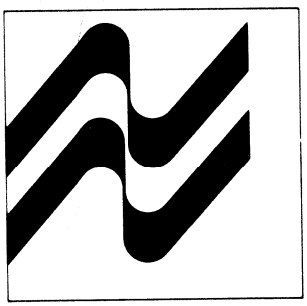
CMOS
DATABOOK

NATIONAL
SEMICONDUCTOR



CMOS INTEGRATED CIRCUITS

Introduction

74C is a CMOS pin for pin, function for function, equivalent to the 7400 TTLP family. This concept in CMOS was designed with the engineer in mind. Strict design rules were adhered to in the input and output characteristics, such as making all outputs capable of sinking 360 μA (one low power Schottky load) and specifying all AC parameters at 50 pF loads. These consistent design rules will simplify system design by giving the engineer realistic and workable parameters. The engineer can take full advantage of his knowledge of the 7400 line and utilize the design tricks he has learned.

For those designs that require 4000 Series, National also manufactures these circuits.

Numerical Index and Table of Contents

(*: Product added to this Data Book since last edition)

74C DATA SHEETS IN NUMERICAL ORDER

Numerical Index and Table of Contents

74C DATA SHEETS IN NUMERICAL ORDER (cont.)

A TO D CONVERTER DATA SHEETS IN NUMERICAL ORDER

Numerical Index and Table of Contents

Numerical Index and Table of Contents

CD4000 DATA SHEETS IN NUMERICAL ORDER (cont.)

Numerical Index and Table of Contents

Numerical Index and Table of Contents

CMOS Guide

GATES

MM54C00/MM74C00 Quad 2-Input NAND Gate

MM54C02/MM74C02 Quad 2-Input NOR Gate

MM54C04/MM74C04 Hex Inverter

MM54C08/MM74C03 Quad 2-Input AND Gate

MM54C10/MM74C10 Triple 3-Input NAND Gate

MM54C20/MM74C20 Dual 4-Input NAND Gate

MM54C30/MM74C30 8-Input NAND Gate

MM54C32/MM74C32 Quad 2-Input OR Gate

MM54C86/MM74C86 Quad 2-Input Exclusive-OR Gate

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

CD4001M/CD4001C Quadruple 2-Input NOR Gate

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate

CD4002M/CD4002C Dual 4-Input NOR Gate

CD4007M/CD4007C Dual Complementary Pair Plus Inverter

CD4011M/CD4011C Quad 2-Input NAND Buffered B Series Gate

CD4012M/CD4012C Dual 4-Input NAND Gate

CD4019BM/CD4019BC Quad AND-OR Select Gate

CD4023M/CD4023C Triple 3-Input NAND Gate

CD4023BM/CD4023BC Triple 3-Input NAND Gate

CD4025M/CD4025C Triple 3-Input NOR Gate

CD4025BM/CD4025BC Triple 3-Input NOR Gate

CD4030M/CD4030C Quad Exclusive-OR Gate

CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

CD4069M/CD4069C Inverter Circuits

CD4070BM/CD4070BC Quad 2-Input Exclusive-OR Gate

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate

CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate

CD4075BM/CD4075BC Double Buffered Triple 3-Input OR Gate

CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

CD45198BM/CD45198BC 4-Bit AND/OR Selector

BUFFERS

MM54C240/MM74C240 Octal TRI-STATE® Buffer

MM54C244/MM74C244 Octal TRI-STATE® Buffer

MM54C901/MM74C901 Hex Inverting TTL Buffer

MM54C902/MM74C902 Hex Non-Inverting TTL Buffer

MM54C903/MM74C903 Hex Inverting PMOS Buffer

MM54C904/MM74C904 Hex Non-Inverting PMOS Buffer

MM54C906/MM74C906 Hex Open Drain N-Channel Buffer

MM54C907/MM74C907 Hex Open Drain P-Channel Buffer

MM74C908 Dual CMOS 30 Volt Driver

MM74C918 Dual CMOS 30 Volt Driver

MM70C95/MM80C95 TRI-STATE® Hex Buffers

MM70C96/MM80C96 TRI-STATE® Hex Inverters

MM70C97/MM80C97 TRI-STATE® Hex Buffers

MM70C98/MM80C98 TRI-STATE® Hex Inverters

MM75250 Octal TRI-STATE® Buffer

MM78C29/MM88C29 Quad Single-Ended Line Driver

CMOS Guide

BUFFERS (cont.)

MM78C30/MM88C30 Dual Differential Line Driver

CD4009M/CD4009C Hex Buffer (Inverting)

CD4010M/CD4010C Hex Buffer (Non-Inverting)

CD4041M/CD4041C Quad True/Complement Buffer

CD4049M/CD4049C Hex Inverting Buffer

CD4050BM/CD4050BC Hex Non-Inverting Buffer

CD4503BM/CD4503BC TRI-STATE® Hex Buffers

DS1630/DS3630 Hex CMOS Compatible Buffer

DS78C20/DS88C20 Dual Compatible Differential Line Receiver

FLIP-FLOPS

MM54C73/MM74C73 Dual J-K Flip-Flops with Clear

MM54C73/MM74C73 Dual D Flip-Flop

MM54C76/MM74C76 Dual J-K Flip-Flops with Clear and Preset

MM54C107/MM74C107 Dual J-K Flip-Flops with Clear

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

MM54C174/MM74C173 Hex D Flip-Flop

MM54C175/MM74C175 Quad D Flip-Flop

MM54C373/MM74C373 TRI-STATE® Octal Latch

MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

CD4013BM/CD4013BC Dual D Flip-Flop

CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

CD4042BM/CD4042BC Quad Clocked D Latch

CD4043M/CD4043C Quad TRI-STATE® NOR R/S Latches

CD4044M/CD4044C Quad TRI-STATE® NAND R/S Latches

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

CD4099BM/CD4099BC 8-Bit Addressable Latches

CD40174BM/CD40174BC Hex D Flip-Flop

CD40175BM/CD40175BC Quad D Flip-Flop

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch

CD4724BM/CD4724BC 8-Bit Addressable Latches

COUNTERS

MM54C90/MM74C90 4-Bit Decade Counter

MM54C93/MM74C93 4-Bit Binary Counter

MM54C160/MM74C106 Decade Counter with Asynchronous Clear

MM54C161/MM74C161 Binary Counter with Asynchronous Clear

MM54C162/MM74C162 Decade Counter with Synchronous Clear

MM54C163/MM74C163 Binary Counter with Synchronous Clear

MM54C192/MM74C192 Synchronous 4-Bit Up/Down Decade Counter

MM54C193/MM74C193 Synchronous 4-Bit Up/Down Binary Counter

MM74C925 4-Digit Counter with Multiplexed 7-Segment Output Driver

MM74C926 4-Digit Counter with Multiplexed 7-Segment Output Driver

MM74C927 4-Digit Counter with Multiplexed 7-Segment Output Driver

MM74C928 4-Digit Counter with Multiplexed 7-Segment Output Driver

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs

CD4018BM/CD4018BC Presettable Divide-by-N Counter

CD4020BM/CD4020BC 14-Stage Ripple-Carry Binary Counter/Divider

CMOS Guide

COUNTERS (cont.)

CD4022BM/CD4022BC Divide-by-8 Counter/ Divider with 8 Decoded Outputs

CD4024BM/CD4024BC 7-Stage Ripple-Carry Binary Counter/Divider

CD4029BM/CD4029BC Presettable Binary/ Decade Up/Down Counter

CD4040BM/CD4040BC 14-Stage Ripple Carry Binary Counters

CD4060BM/CD4060BC 12-Stage Ripple Carry Binary Counters

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear

CD40161BM/CD40161BC Binary Counter with Asynchronous Clear

CD40162BM/CD40162BC Decade Counter with Synchronous Clear

CD40163BM/CD40163BC Binary Counter with Synchronous Clear

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter

CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

CD40195 4-Bit Parallel Shift Register

CD4510BM/CD4510BC BCD Up/Down Counter

CD4516BM/CD4516BC Binary Up/Down Counter

CD4518BM/CD4518BC Dual Synchronous Up Counter

CD4520BM/CD4520BC Dual Synchronous Up Counter

CD4522BM/CD4522BC Programmable Divide-by-N Counter (BCD)

CD4526BM/CD4526BC Programmable Divide-by-N Counter (Binary)

MM5369 Programmable Oscillator Divider

SHIFT REGISTERS

MM54C95/MM74C95 4-Bit Right Shift Left Shift Register

MM54C164/MM74C164 8-Bit Parallel-Out Serial Shift Register

MM54C165/MM74C165 Parallel-Load 8-Bit Shift Register

CD4006M/CD4006C 18-Stage Static Shift Register

CD4014M/CD4014C 8-Stage Static Shift Register

CD4015M/CD4015C Dual 4-Bit Static Register

CD4021M/CD4021C 8-Stage Static Shift Register

CD4031BM/CD4031BC 64-Stage Static Shift Register

CD4034BM/CD4034BC 8-Stage TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

CD4035BM/CD4035BC 4-Bit Parallel-In/ Parallel-Out Shift Register

DECODERS/MULTIPLEXERS

MM54C42/MM74C42 BCD-to-Decimal Decoder

MM54C48/MM74C48 BCD-to-7 Segment Decoder

MM54C150/MM74C150 16-Line to 1-Line Multiplexer

MM54C151/MM74C151 8-Channel Digital Multiplexer

MM54C154/MM74C154 4-Line to 16-Line Decoder/Demultiplexer

MM54C157/MM74C157 Quad 2-Input Multiplexer

MM54C922/MM74C922 16-Key Encoder

MM54C923/MM74C923 20-Key Encoder

MM74C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

CD4016M/CD4016C Quad Bilateral Switch

CD4028BM/CD4028BC BCD-to-Decimal Decoder

CD4051BM/CD4051BC Analog Multiplexers/ Demultiplexers

CD4052BM/CD4052BC Analog Multiplexers/ Demultiplexers

CMOS Guide

DECODERS/MULTIPLEXERS (cont.)

CD4053BM/CD4053BC Analog Multiplexers/ Demultiplexers

CD4066BM/CD4066BC Quad Bilateral Switch

CD4511BM/CD4511BC BCD-to-7 Segment Latch Decoder/Driver

CD4512M/CD4512C 8-Channel Data Selector

CD4514BM/CD4514BC 4-to-16 Line Decoder (High)

CD4515BM/CD4515BC 4-to-16 Line Decoder (Low)

CD4529BM/CD4529BC Dual 4-Channel Analog Data Selector

CD4543BM/CD4543BC BCD-to-7 Segment Decoder (LCD)

MEMORIES

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

MM54C200/MM74C200 256-Bit (256x1) TRI-STATE® Random Access Read/Write Memory

MM54C910/MM74C910 256-Bit (64x4) TRI-STATE® Random Access Read/Write Memory

MM54C920/MM74C920 1024-Bit (256x4) Static Silicon Gate CMOS RAM

MM54C921/MM74C921 1024-Bit (256x4) Static Silicon Gate CMOS RAM

MM54C929/MM74C929 1024-Bit (1024x1) Static Silicon Gate CMOS RAM

MM54C930/MM74C930 1024-Bit (1024x1) Static Silicon Gate CMOS RAM

ARITHMETIC FUNCTIONS

MM54C83/MM74C83 4-Bit Binary Full Adder

MM54C85/MM74C85 4-Bit Magnitude Comparator

CD4008BM/CD4008BC 4-Bit Full Adder

SPECIAL FUNCTIONS

MM54C14/MM74C14 Hex Schmitt Trigger

MM54C221/MM74C221 Dual Monostable Multivibrator

MM54C909/MM74C909 Quad Comparator

MM74C911 Display Controller

MM74C912 Display Controller

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

MM54C915/MM74C915 7-Segment-to-BCD Converter

MM74C932 Phase Detector

CD4046BM/CD4046BC Micropower Phase-Locked Loop

CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator

CD4089BM/CD4089BC Binary Rate Multiplier

CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger

CD40106BM/CD40106BC Hex Schmitt Trigger

CD4527BM/CD4527BC BCD Rate Multiplier

CD4528BM/CD4528BC Dual Retriggerable/Resettable Monostable Multivibrator

DS1631/DS3631 Dual Peripheral Driver

DS1632/DS3632 Dual Peripheral Driver

DS1633/DS3633 Dual Peripheral Driver

DS1634/DS3634 Dual Peripheral Driver

DS1686/DS3686 Positive Voltage Relay Driver

DS1687/DS3687 Negative Voltage Relay Driver

LM146/LM246/LM346 Programmable Quad Operational Amplifier

MM5393 Push Button Telephone Dialer

MM5395 Touch Tone® Generator

MM53100 Programmable TV Timer

MM53104 TV Game Clock Generator

MM53105 Programmable TV Timer

CMOS Guide

SPECIAL FUNCTIONS (cont.)

MM55104 Phase Lock Loop Frequency Synthesizer

MM55106 Phase Lock Loop Frequency Synthesizer

MM55114 Phase Lock Loop Frequency Synthesizer

MM55116 Phase Lock Loop Frequency Synthesizer

MM5840 TV Channel and Time Circuit

MM5841 TV Channel and Time Circuit

MM58106 Digital Clock and TV Display Circuit

A-TO-D CONVERTERS

ADC0816 8-Bit A-to-D Converter (16-Channel MUX)

ADC0817 8-Bit A-to-D Converter (16-Channel MUX)

ADC3501 3½-Digit DVM with 7-Segment Output

ADC3701 3¾-Digit DVM with 7-Segment Output

ADD3511 Microprocessor Compatible A-to-D Converter

ADD3711 Microprocessor Compatible A-to-D Converter

Specifications for "B" Series

National Semiconductor complies with the CMOS "B" Series specification as called out in JEDEC Standard No. 13A. All parts called out as "B" are double buffered and will meet as a minimum the electrical parameters listed in table A. As agreed upon in the JEDEC Spec, products called out as UB are not double buffered but meet table A specifications with the exception of V_{IL} and V_{IH}, which will be 20% and 80%, respectively, of V_{DD}. **The 54C/74C family meets or exceeds the "B"/"UB" specifications as given in table A but are not marked "B"/"UB."**

Table A

Parameter		Temp Range	V_{DD} (Vdc)	Conditions	Limits T_{LOW}* Min	T_{LOW}* Max	+25°C Min	+25°C Typ	+25°C Max	T_{HIGH}* Min	T_{HIGH}* Max	Units
I_{DD}	Quiescent Device Current GATES	Mil	5	$V_I = V_{SS}$ or V_{DD}		0.25			0.25		7.5	μAdc
			10			0.5			0.5		15	
			15			1.0			1.0		30	
		Comm	5	All valid input combinations		1.0			1.0		7.5	μAdc
			10			2.0			2.0		15	
			15			4.0			4.0		30	
	BUFFERS, FLIP-FLOPS	Mil	5	$V_I = V_{SS}$ or V_{DD}		1.0			1.0		30	μAdc
			10			2.0			2.0		60	
			15			4.0			4.0		120	
		Comm	5	All valid input combinations		4.0			4.0		30	μAdc
			10			8.0			8.0		60	
			15			16.0			16.0		120	
	MSI	Mil	5	$V_I = V_{SS}$ or V_{DD}		5			5		150	μAdc
			10			10			10		300	
			15			20			20		600	
		Comm	5	All valid input combinations		20			20		150	μAdc
			10			40			40		300	
			15			80			80		600	
V_{OL}	Low-Level Output Voltage	All	5	$V_I = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\ \mu A$		0.05			0.05		0.05	Vdc
			10			0.05			0.05		0.05	
			15			0.05			0.05		0.05	
V_{OH}	High-Level Output Voltage	All	5	$V_I = V_{SS}$ or V_{DD} $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95			4.95		Vdc
			10		9.95		9.95			9.95		
			15		14.95		14.95			14.95		
V_{IL}	Input Low Voltage	All	5	$V_O = 0.5$ V or 4.5 V, $\lvert I_O \rvert < 1\ \mu A$		1.5			1.5		1.5	Vdc
			10	$V_O = 1.0$ V or 9.0 V, $\lvert I_O \rvert < 1\ \mu A$		3.0			3.0		3.0	
			15	$V_O = 1.5$ V or 13.5 V, $\lvert I_O \rvert < 1\ \mu A$		4.0			4.0		4.0	
V_{IH}	Input High Voltage	All	5	$V_O = 0.5$ V or 4.5 V, $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5			3.5		Vdc
			10	$V_O = 1.0$ V or 9.0 V, $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0			7.0		
			15	$V_O = 1.5$ V or 13.5 V, $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0			11.0		
I_{OL}	Output Low (Sink) Current	Mil	5	$V_O = 0.4$ V, $V_I = 0$ V or 5 V	0.64		0.51			0.36		mAdc
			10	$V_O = 0.5$ V, $V_I = 0$ V or 10 V	1.6		1.3			0.9		
			15	$V_O = 1.5$ V, $V_I = 0$ V or 15 V	4.2		3.4			2.4		
		Comm	5	$V_O = 0.4$ V, $V_I = 0$ V or 5 V	0.52		0.44			0.36		mAdc
			10	$V_O = 0.5$ V, $V_I = 0$ V or 10 V	1.3		1.1			0.9		
			15	$V_O = 1.5$ V, $V_I = 0$ V or 15 V	3.6		3.0			2.4		
I_{OH}	Output High (Source) Current	Mil	5	$V_O = 4.6$ V, $V_I = 0$ V or 5 V	−0.25		−0.2			−0.14		mAdc
			10	$V_O = 9.5$ V, $V_I = 0$ V or 10 V	−0.62		−0.5			−0.35		
			15	$V_O = 13.5$ V, $V_I = 0$ V or 15 V	−1.8		−1.5			−1.1		
		Comm	5	$V_O = 4.6$ V, $V_I = 0$ V or 5 V	−0.2		−0.16			−0.12		mAdc
			10	$V_O = 9.5$ V, $V_I = 0$ V or 10 V	−0.5		−0.4			−0.3		
			15	$V_O = 13.5$ V, $V_I = 0$ V or 15 V	−1.4		−1.2			−1.0		
I_I	Input Current	Mil	15	$V_I = 0$ V or 15 V		±0.1			±0.1		±1.0	μAdc
		Comm	15	$V_I = 0$ V or 15 V		±0.3			±0.3		±1.0	μAdc
C_I	Input Capacitance per Unit Load	All	—	Any Input					7.5			pF

Note: For current flow the convention is positive for current flowing into the device and negative flowing out of the device.

*T_{LOW} = −55°C for Military Temp Range device, −40°C for Commercial Temp Range device.

*T_{HIGH} = +125°C for Military Temp Range device, +85°C for Commercial Temp Range device.

54C/74C Power Consumption Characteristics Guide

Typical characteristics $T_A = 25°C$.

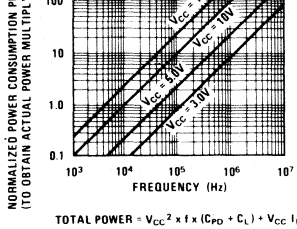
DEVICE TYPE/PRODUCT DESCRIPTION	C_{PD} (pF) (Note 3)	t_{pd} (ns) $C_L = 50$ pF $V_{CC} = 5.0V$	Δt_{pd}/pF CURVE	LTTL (TTL)* FAN OUT
MM54C00/MM74C00 Quad 2-Input NAND Gate	12	50	A	2
MM54C02/MM74C02 Quad 2-Input NOR Gate	12	50	A	2
MM54C04/MM74C04 Hex Inverter	12	50	A	2
MM54C08/MM74C08 Quad 2-Input AND Gate	14	80	A	2
MM54C10/MM74C10 Triple 3-Input NAND Gate	18	60	A	2
MM54C14/MM74C14 Hex Schmitt Trigger	20	220	A	2
MM54C20/MM74C20 Dual 4-Input NAND Gate	30	70	A	2
MM54C30/MM74C30 8-Input NAND Gate	26	125	A	2
MM54C32/MM74C32 Quad 2-Input OR Gate	15	80	A	2
MM54C42/MM74C42 BCD-to-Decimal Decoder	50	200	A	2
MM54C48/MM74C48 BCD-to-7 Segment Decoder	NA	450 (1)	NA	2
MM54C73/MM74C73 Dual J-K Flip-Flop	40	180	A	2
MM54C74/MM74C74 Dual D Flip-Flop	40	180	A	2
MM54C76/MM74C76 Dual J-K Flip-Flop	40	180	A	2
MM54C83/MM74C83 4-Bit Binary Full Adder	120	300	A	2
MM54C85/MM74C85 4-Bit Magnitude Comparator	45	220 (1)	A	2
MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate	20	110	A	2
MM54C89/MM74C89 64-bit TRI-STATE® Random Access Memory	230	270	A	2
MM54C90/MM74C90 4-Bit Decade Counter	45	400	A	2
MM54C93/MM74C93 4-Bit Binary Counter	45	400	A	2
MM54C95/MM74C95 4-Bit R-S/L-S Register	100	200	A	2
MM54C107/MM74C107 Dual J-K Flip-Flop	40	180	A	2
MM54C150/MM74C150 16:1 Multiplexer	100	250	A	1*
MM54C151/MM74C151 8-Channel Digital Multiplexer	50	200 (1)	A	2
MM54C154/MM74C154 4:16 Decoder/Demultiplexer	60	275 (1)	A	2
MM54C157/MM74C157 Quad 2-Input Multiplexer	20	150 (1)	A	2
MM54C160/MM74C160 Sync Decade Counter	95	250 (2)	A	2
MM54C161/MM74C161 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C162/MM74C162 Sync Decade Counter	95	250 (2)	A	2
MM54C163/MM74C163 Sync 4-Bit Binary Counter	95	250 (2)	A	2
MM54C164/MM74C164 8-Bit SI/PO S/R	140	230 (2)	A	2
MM54C165/MM74C165 8-Bit PI/SO S/R	55	210 (2)	A	2
MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop	100	220 (2)	A	2
MM54C174/MM74C174 Hex D Flip-Flop	95	150 (2)	A	2
MM54C175/MM74C175 Quad D Flip-Flop	130	190 (2)	A	2
MM54C192/MM74C192 Sync Up/Down Decade Counter	100	250 (2)	A	2
MM54C193/MM74C193 Sync Up/Down Binary Counter	100	250 (2)	A	2
MM54C195/MM74C195 4-Bit Parallel S/R	130	200 (2)	A	2
MM54C200/MM74C200 256-Bit RAM	400	850	A	1*
MM54C221/MM74C221 Dual Monostable Multivibrators	NA	250 (2)	A	2
MM54C373/MM74C373 TRI-STATE® Octal Flow-through Latch	200	165	A	1*
MM54C374/MM74C374 TRI-STATE® Octal D Flip-Flop	250	165	A	1*
MM54C901/MM74C901 Hex Inverting TTL Buffer	30	38	B	2*
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM54C902/MM74C903 Hex Inverting TTL Buffer	30	38	B	2*
MM54C904/MM74C904 Hex Non-Inverting TTL Buffer	50	57	B	2*
MM54C905/MM74C905 12-Bit Successive Approximation Register	100	200	A	2
MM54C906/MM74C906 Hex Open Drain N-Channel Buffers	30	NA	NA	2*
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers	30	NA	NA	2*
MM54C908/MM74C908 Dual High Voltage CMOS Driver	NA	150 (1)	NA	NA
MM54C914/MM74C914 Hex Schmitt Trigger	20	220	A	2
MM54C918/MM74C918 Dual High Voltage CMOS Driver	NA	150 (1)	NA	NA
MM70C95/MM80C95 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*
MM70C96/MM80C96 TRI-STATE® Hex Inverting Buffer	60	70	B	1*
MM70C97/MM80C97 TRI-STATE® Hex Non-Inverting Buffer	60	60	B	1*
MM70C98/MM80C98 TRI-STATE® Hex Inverting Buffer	60	70	B	1*
MM72C19/MM82C19 TRI-STATE® 16:1 Multiplexer	100	250	A	1*
MM78C29/MM88C29 Quad Single Ended Line Driver	150	200	NA	5*
MM78C30/MM88C30 Dual Differential Line Driver	200	350	NA	5*

Note 1: t_{pd} shown is from data input to output. For more detailed specifications see individual data sheet.

Note 2: t_{pd} shown is from clock to output. For more detailed specifications see individual data sheet.

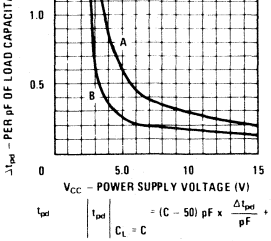
Note 3: C_{PD} numbers shown are for independent identical functions within a package. For instance the total C_{PD} for a MM74C157 is 4 x 20 pF = 80 pF while the total C_{PD} for the MM74C173 is 100 pF because all flip-flops have a common clock.

Normalized Typical Power Consumption vs Frequency



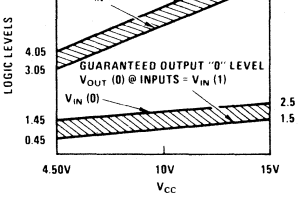
TOTAL POWER = $V_{CC}^2 \times f \times (C_{PD} + C_L) + V_{CC} \times I_{LEAKAGE}$

Typical Propagation Delay per pF of Load Capacitance vs Power Supply



$$t_{pd}\Big|_{C_L = C} = (C - 50)\text{ pF} \times \frac{\Delta t_{pd}}{\text{pF}} + t_{pd}\Big|_{C_L = 50\text{ pF}}$$

Guaranteed Noise Margin Over Temperature vs V_{CC}



For complete explanation on use of curves see application note AN-90, 54C/74C Family Characteristics.

National Semiconductor

MM74C911/12/13 Display Controller

Features

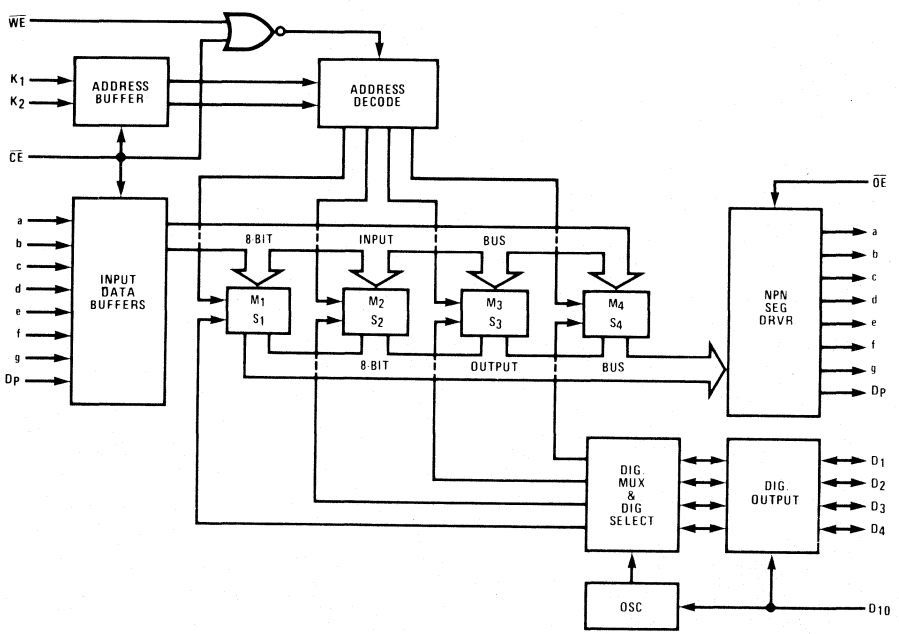
- Drives 7-Segment Display Directly
- Handles All Housekeeping Chores of Driving and Refreshing Display
- Single 5-Volt Supply
- Options

  MM74C911 (28-Pin):
  - 4 Digits, 8 Segments, Expandable in Digits and Segments
  - Direct Input Control on Each of the 8 Segments

  MM74C912 (28-Pin):
  - 4-Bit BCD Plus a Decimal Input
  - 6 Digits, 8 Segments with Decoder on Chip
  - Digit Expansion Capability

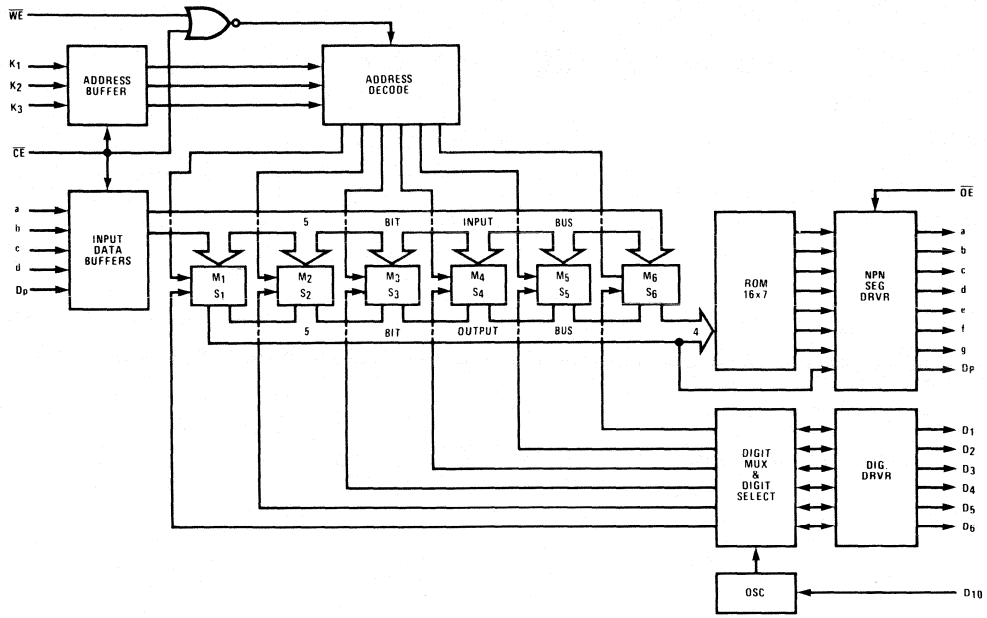
  MM74C917 (24-pin)
  - Same as MM74C917 Except Hexadecimal

Block Diagram



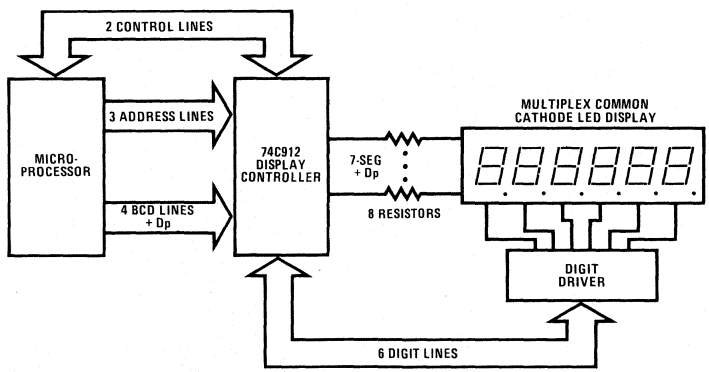
MM74C911

Block Diagram (cont.)



MM74C912/MM74C917

Application



Display Controller Interfacing with a Microprocessor

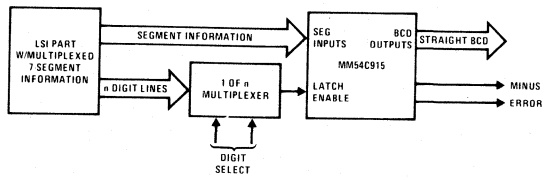
National Semiconductor

MM74C915 7-Segment to BCD Converter

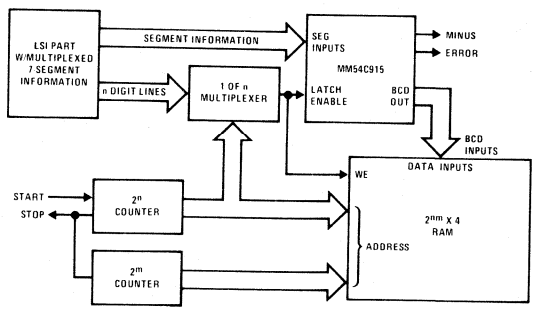
Features

- Single Supply 3V – 15V
- Polarity Input Control (active high or low on segment inputs)
- Output Latch
- Minus Sign Output
- Error Output for Non-BCD Characters
- TTL Compatible TRI-STATE Output
- Decodes Blank into "1" "1" "1" "1"
- Will Accept 6 or 9 With or Without Top or Bottom Bar
- Will Accept Right- or Left-Justified Ones

Application

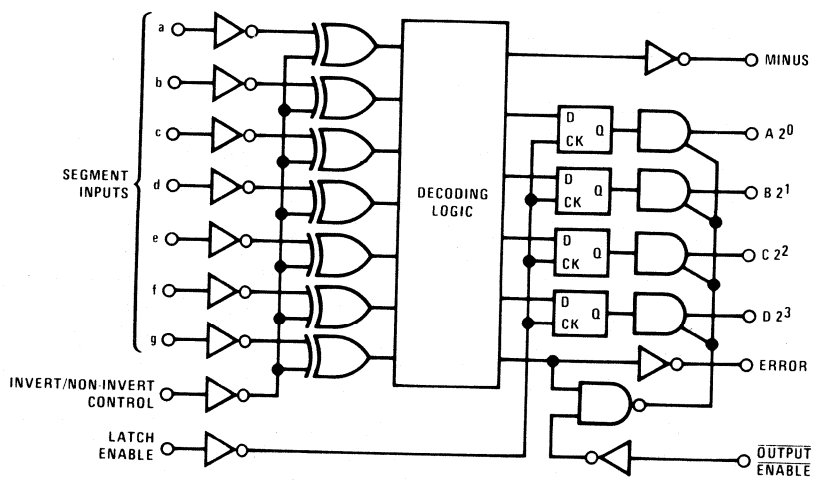


Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs

Block Diagram



MM74C915 7-Segment to BCD Converter

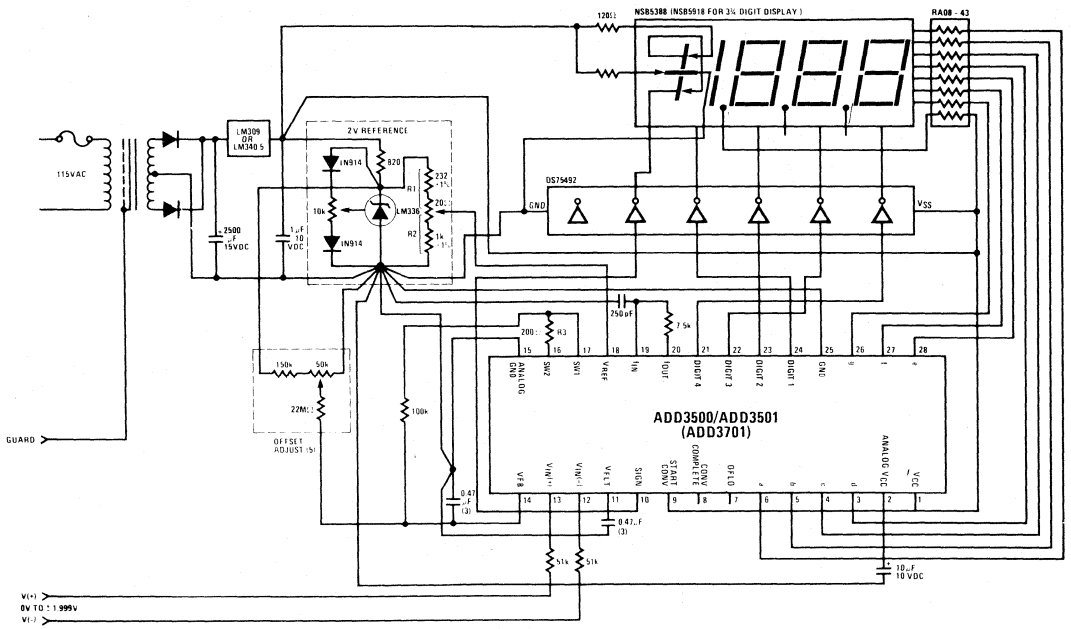
National Semiconductor

ADD3501/ADD3701 3½/3¾-Digit DVMs

Features

- Single Chip
- Single 5-Volt Supply
- ADD3501 Converts 0 to ±1999 Counts
- ADD3701 Converts 0 to ±3999 Counts
- Drives Multiplexed 7-Segment Directly
- No External Precision Components Required
- Overrange Indicated by +OFL, −OFL Display
- Auto Polarity
- On-Chip Clock/External Clock
- Conversion Time 200 ms

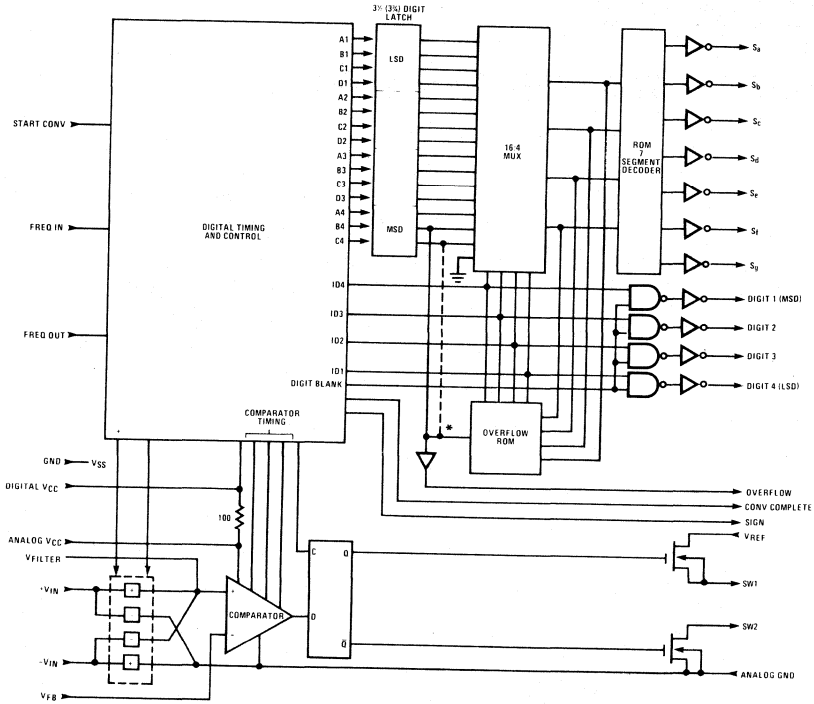
Application



NOTES:
1. ALL RESISTORS ¼ WATT ±5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\Omega$
5. OFFSET ADJUST REQUIRED FOR MM74C935-1 (ADD3501) ONLY.

ADD3500/ADD3501 3½-Digit DPM, ±1.999 Volts Full Scale
(ADD3701 3¾-Digit DPM, ±3.999 Counts Full Scale)

Block Diagram



ADD3501/ADD3701 3½/3¾ DVM Chip

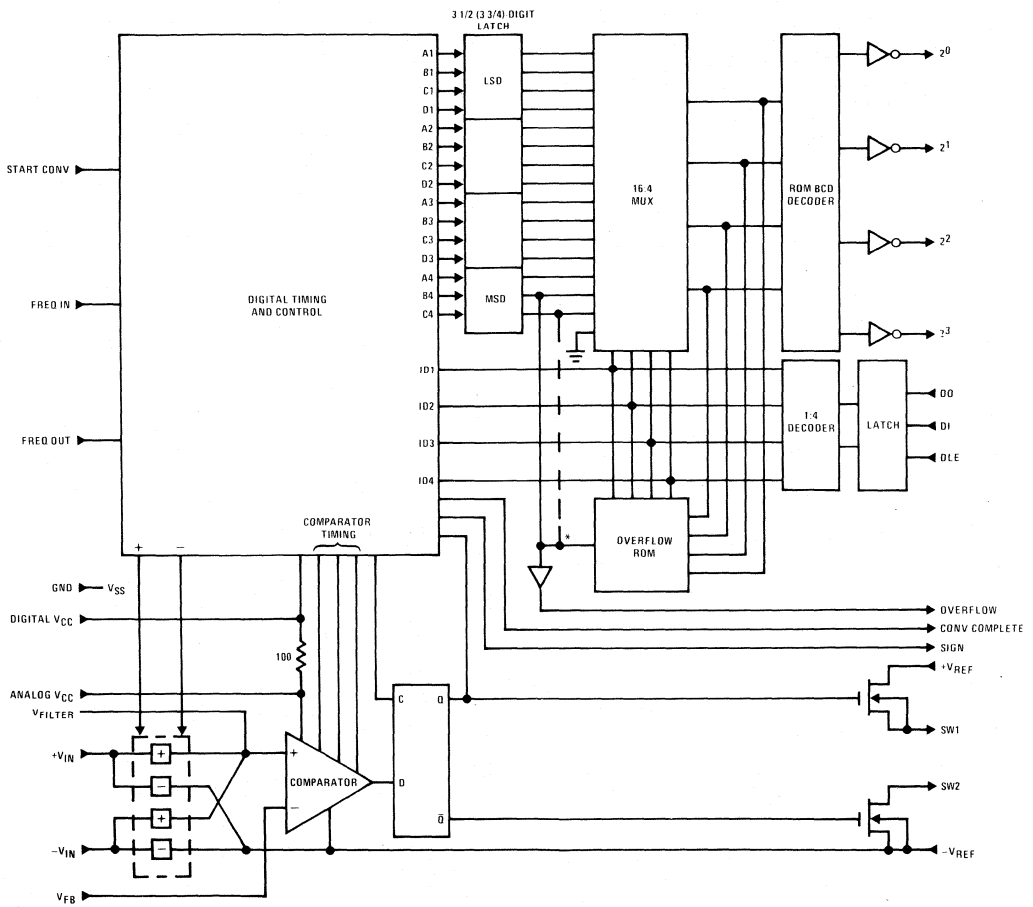
National Semiconductor

ADC3511/ADC3711 3½/3¾-Digit Microprocessor Compatible A/D Converter

Features

- Single Chip
- Single 5-Volt Supply
- ADC3511 Converts 0 to ±1999 Counts
- ADC3711 Converts 0 to ±3999 Counts
- Uses Single 2-Volt Reference
- Addressable BCD Outputs (provide simple microprocessor interfacing)
- No External Precision Components Required
- Overrange Indicated by Hex "EEEE" and Overflow Output
- On-Chip or External Clock
- Conversion Time 200 ms
- See AN-200 for Interfacing to μ Processors

Block Diagram



ADC3711 A/D Converter

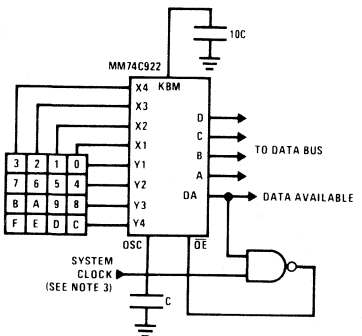
National Semiconductor

MM74C922/MM74C923 16/20 Key Keyboard Encoder

Features

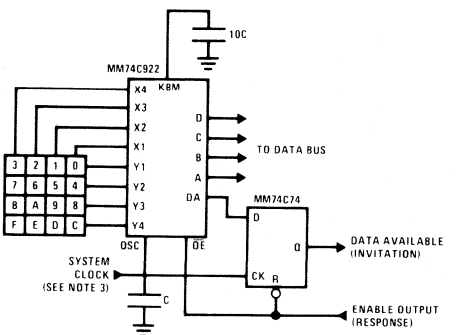
- Keybounce Elimination
- TRI-STATE Output
- Two-Key Rollover
- Internal Latch (last key register at outputs)
- On-Chip Pullup Devices
- 50 kΩ Maximum Switch On Resistance

Application

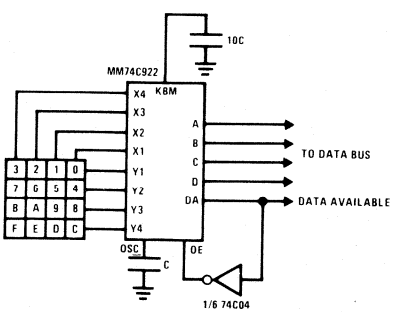


Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Synchronous Handshake (MM74C922)



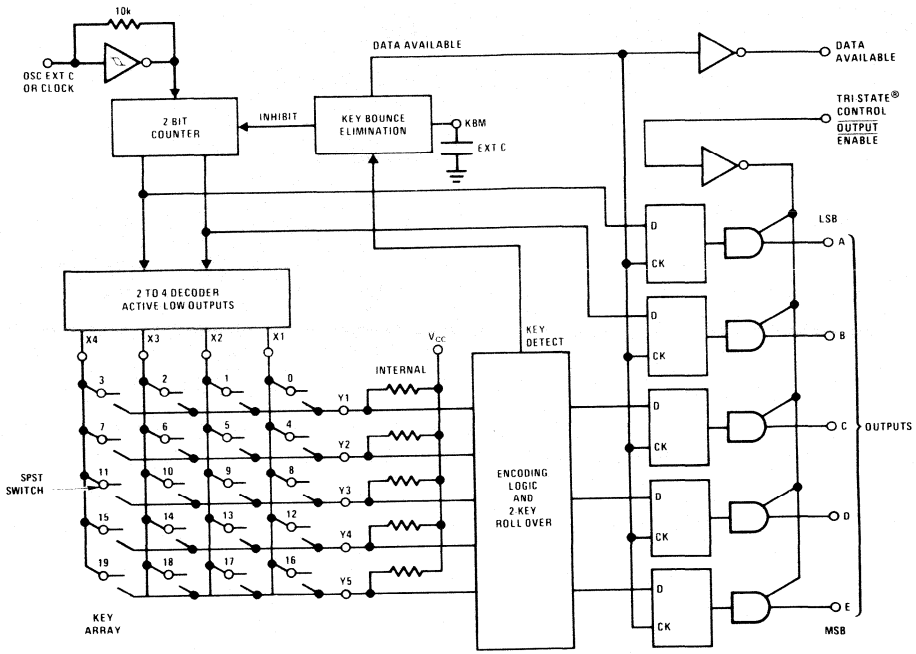
Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Synchronous Data Entry Onto Bus (MM74C922)

Block Diagram



MM74C923 20-Key Keyboard Encoder

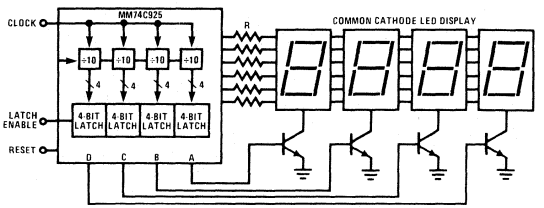
National Semiconductor

MM74C925/26/27/28 4-Digit Counters with Multiplexed 7-Segment Output Drivers

Features

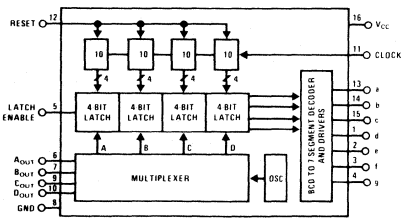
- 4-Digit Counter
- Multiplexed 7-Segment Output Driver
- Output Latch
- Counter Expansion Capability
- Display Select (Counter or Latch)

Application

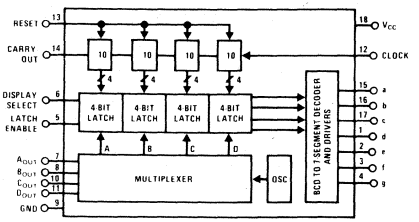


MM74C925 Count and Display Application

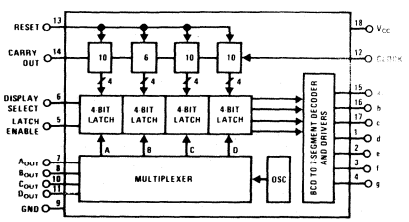
Block Diagrams



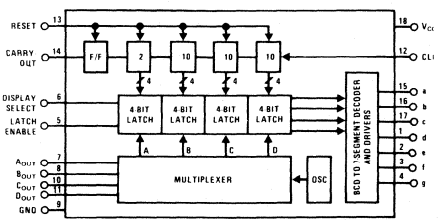
MM74C925



MM74C926



MM74C927



MM74C928

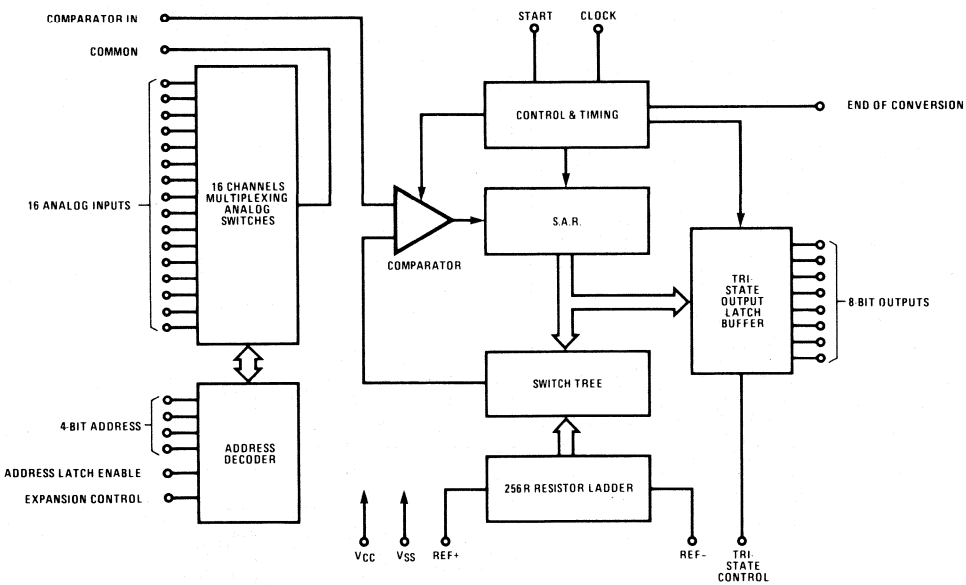
National Semiconductor

ADC0816/ADC0817 8-Bit A-D Converter with 16 Channel Analog Multiplexer

Features

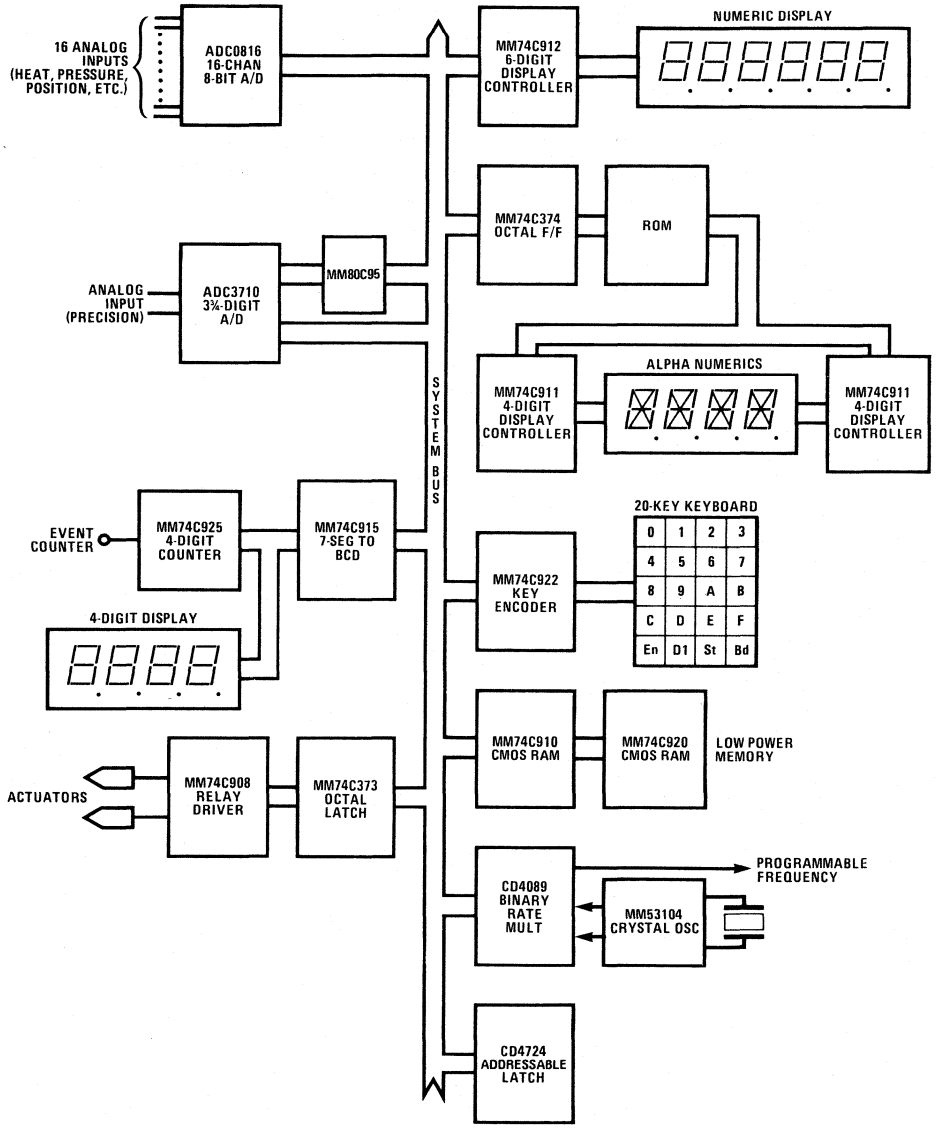
- Single 5-Volt Supply
- Single 5-Volt Reference
- 256 R Ladder On Chip
- Guaranteed Monotonicity
- Latched TRI-STATE Output
- Linearity ±½ LSB (10 mV)
- Drives 1 TTL Load
- 16-Channel Multiplexer On Chip
- Sample and Hold Capability
- Conversion Time 100 μs

Block Diagram



National Semiconductor

Microprocessor Applications



Cross Reference Guide

National	RCA	Harris	Motorola	TI	Fairchild
MM74C00		HD74C00			
MM74C02		HD74C02			
MM74C04	CD4069	HD74C04	MC14069		
MM74C08		HD74C08			
MM74C10		HD74C10			
MM74C14	CD40106	HD74C14	MC14584		340014
MM74C20		HD74C20			
MM74C30		HD74C30			
MM74C32		HD74C32			
MM74C42		HD74C42			
MM74C48		HD74C48			
MM74C73		HD74C73			
MM74C74		HD74C74			
MM74C76		HD74C76			
MM74C83		HD74C83			
MM74C85	CD4030	HD74C85			
MM74C86	CD4070B	HD74C86	MC14507		
MM74C89		HD74C89			
MM74C90					
MM74C93					
MM74C95		HD74C95			
MM74C107		HD74C107			
MM74C151		HD74C151			
MM74C154		HD74C154			
MM74C157		HD74C157			
MM74C160	CD40160	HD74C160	MC14160	TP4360	F340160
MM74C161	CD40161	HD74C161	MC14161	TP4361	F340161
MM74C162	CD40162	HD74C162	MC14162	TP4362	F340162
MM74C163	CD40163	HD74C163	MC14163	TP4363	F340163
MM74C164		HD74C164			
MM74C165		HD74C165			
MM74C173	CD4076	HD74C173	MC14076		
MM74C174	CD40174	HD74C174	MC14174		F340174
MM74C175		HD74C175	MC14175		F340175
MM74C192	CD40192	HD74C192	MC14192		F340192
MM74C193	CD40193	HD74C193	MC14193		F340193
MM74C195	CD40195	HD74C195	MC14195	F340195	
MM74C200		HD74C200			
MM74C221		HD74C221			
MM74C901		HD74C901			
MM74C902		HD74C902			
MM74C903		HD74C903			
MM74C904		HD74C904			
MM74C905					
MM74C906		HD74C906			
MM74C907		HD74C907			
MM74C908					
MM74C918					
MM80C95		HD80C95			
MM80C97			MC14503		F340097
MM80C98		HD80C98			F340098
MM88C29					
MM88C30					

54C/74C Series

National Semiconductor

MM54C00/MM74C00 Quad 2-Input NAND Gate
MM54C02/MM74C02 Quad 2-Input NOR Gate
MM54C04/MM74C04 Hex Inverter
MM54C10/MM74C10 Triple 3-Input NAND Gate
MM54C20/MM74C20 Dual 4-Input NAND Gate

general description

These logic gates employ complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times. With features such as this the 54C/74C logic family is close to ideal for use in digital systems. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers already familiar with the standard 54/74 logic family.

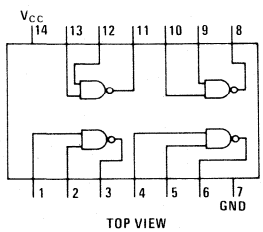
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ.
■ Low power consumption	10 nW/package typ.
■ Low power TTL compatibility	fan out of 2 driving 74L

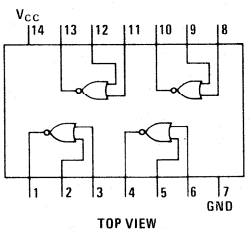
connection diagrams

MM54C00/MM74C00



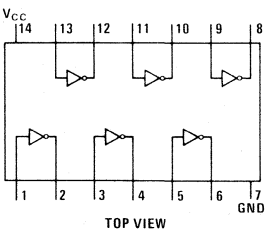
TOP VIEW

MM54C02/MM74C02



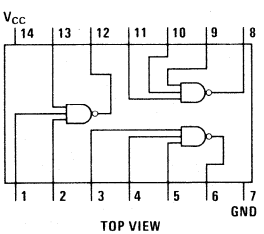
TOP VIEW

MM54C04/MM74C04



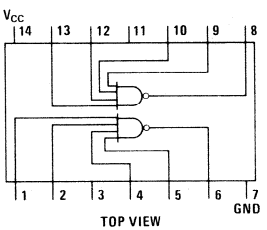
TOP VIEW

MM54C10/MM74C10



TOP VIEW

MM54C20/MM74C20



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
54C	−55°C to +125°C
74C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Operating V_{CC} Range	3.0V to 15V
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across the guaranteed temperature range unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
LOW POWER TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −10μA 74C, V_{CC} = 4.75V, I_O = −10μA	4.4 4.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +10μA 74C, V_{CC} = 4.75V, I_O = +10μA			0.4 0.4	V V
CMOS TO LOW POWER					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	4.0 4.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			1.0 1.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		50	90	ns
	V_{CC} = 10V		30	60	ns
Input Capacitance (C_{IN})	(Note 2)		6.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate or Inverter		12		pF
MM54C10/MM74C10					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		60	100	ns
	V_{CC} = 10V		35	70	ns
Input Capacitance (C_{IN})	(Note 2)		7.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		18		pF
MM54C20/MM74C20					
Propagation Delay Time to Logical "1" or "0" (t_{pd})	V_{CC} = 5.0V		70	115	ns
	V_{CC} = 10V		40	80	ns
Input Capacitance (C_{IN})	(Note 2)		9		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		30		pF

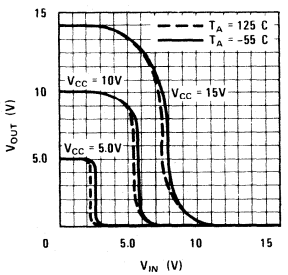
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

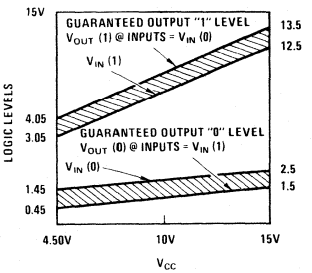
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note — AN-90

typical performance characteristics

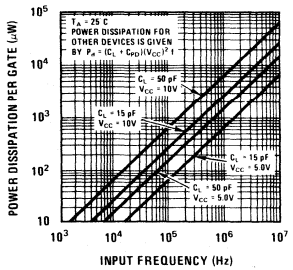
Gate Transfer Characteristics



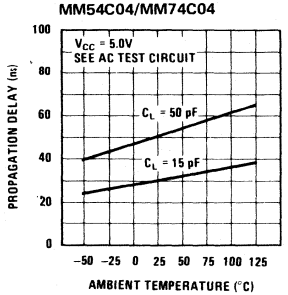
Guaranteed Noise Margin Over Temperature vs V_{CC}



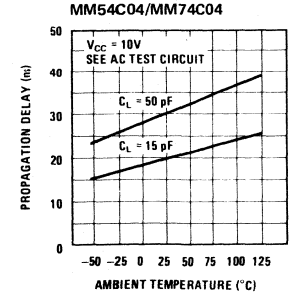
Power Dissipation vs Frequency MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



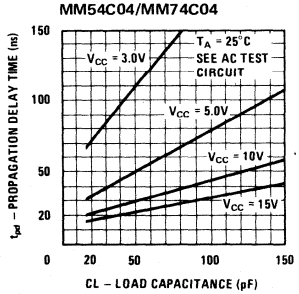
Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04



Propagation Delay vs Ambient Temperature MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

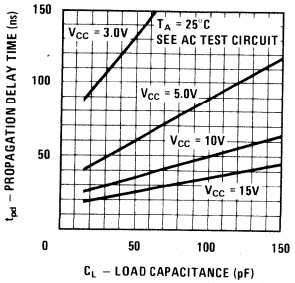


Propagation Delay Time vs Load Capacitance MM54C00/MM74C00, MM54C02/MM74C02, MM54C04/MM74C04

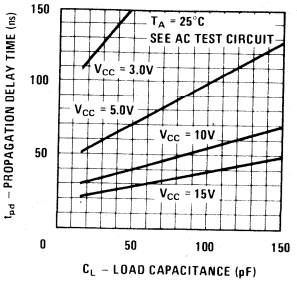


typical performance characteristics (con't)

Propagation Delay Time vs
Load Capacitance
MM54C10/MM74C10

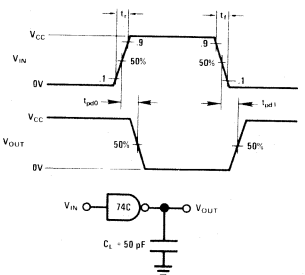


Propagation Delay Time vs
Load Capacitance
MM54C20/MM74C20



switching time waveforms and ac test circuits

CMOS to CMOS



NOTE: DELAYS MEASURED WITH INPUT t_r, $t_f \leq 20$ ns.

National Semiconductor

MM54C08/MM74C08 Quad 2-Input AND Gate
MM54C86/MM74C86 Quad 2-Input EXCLUSIVE-OR Gate

general description

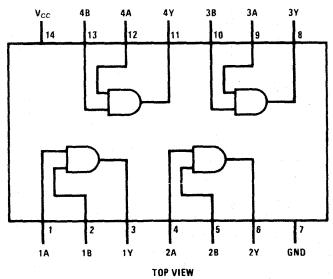
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin these gates provide basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Low power consumption — 10 nW/package typ
- The MM54C86/MM74C86 follows the MM54L86/MM74L86 pinout

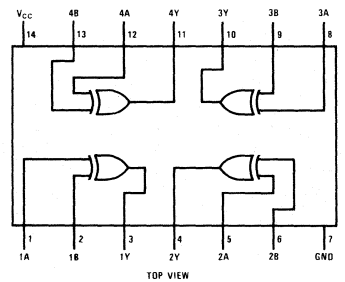
connection diagrams

MM54C08/MM74C08



TOP VIEW

MM54C86/MM74C86



TOP VIEW

truth tables

MM54C08/MM74C08

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	L
H	L	L
H	H	H

H = High Level L= Low Level

MM54C86/MM74C86

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C08, MM54C86	−55°C to +125°C
MM74C08, MM74C86	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA 74C, V_{CC} = 4.75V, I_O = +360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics

(MM54C08/MM74C08) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$		80	140	ns
	$V_{CC} = 10V$		40	70	ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3 Per Gate		14		pF

ac electrical characteristics

(MM54C86/MM74C86) $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$		110	185	ns
	$V_{CC} = 10V$		50	90	ns
Input Capacitance (C_{IN})	Note 2		5.0		pF
Power Dissipation Capacitance (C_{pd})	Note 3 Per Gate		20		pF

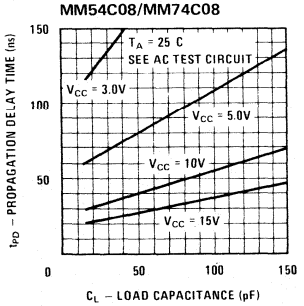
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

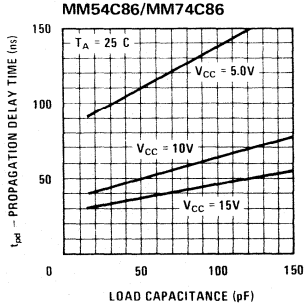
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

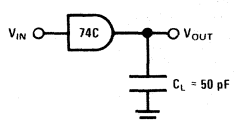
Propagation Delay Time vs Load Capacitance MM54C08/MM74C08



Propagation Delay Time vs Load Capacitance MM54C86/MM74C86

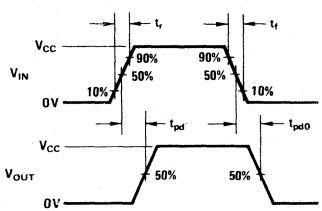


ac test circuit



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns

switching time waveforms



National Semiconductor

MM54C14/MM74C14 Hex Schmitt Trigger

general description

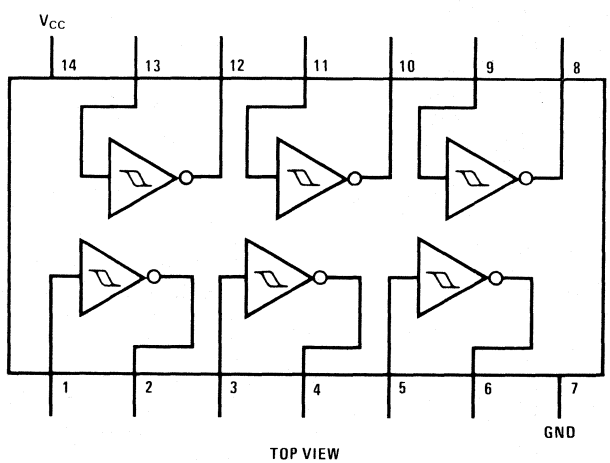
The MM54C14/MM74C14 Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Hysteresis	0.4 V_{CC} typ 0.2 V_{CC} guaranteed

connection diagram



TOP VIEW

absolute maximum ratings

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C14	$-55°C$ to $+125°C$	Absolute Maximum V_{CC}	18V
MM74C14	$-40°C$ to $+85°C$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$		

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage	$V_{CC} = 5V$	3.0	3.6	4.3	V
	$V_{CC} = 10V$	6.0	6.8	8.6	V
	$V_{CC} = 15V$	9.0	10.0	12.9	
V_{T-} Negative Going Threshold Voltage	$V_{CC} = 5V$	0.7	1.4	2.0	V
	$V_{CC} = 10V$	1.4	3.2	4.0	V
	$V_{CC} = 15V$	2.1	5.0	6.0	
Hysteresis ($V_{T+} - V_{T-}$)	$V_{CC} = 5V$	1.0	2.2	3.6	V
	$V_{CC} = 10V$	2.0	3.6	7.2	V
	$V_{CC} = 15V$	3.0	5.0	10.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	$V_{CC} = 5V$, $I_O = -10\mu A$	4.5			V
	$V_{CC} = 10V$, $I_O = -10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	$V_{CC} = 5V$, $I_O = +10\mu A$			0.5	V
	$V_{CC} = 10V$, $I_O = +10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	$V_{CC} = 15V$, $V_{IN} = 15V$		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	$V_{CC} = 15V$, $V_{IN} = 0V$	-1.0	-0.005		μA
Supply Current (I_{CC})	$V_{CC} = 15V$, $V_{IN} = 0V/15V$		0.05	15	μA
	$V_{CC} = 5V$, $V_{IN} = 2.5V$ (Note 4)		20		μA
	$V_{CC} = 10V$, $V_{IN} = 5V$ (Note 4)		200		μA
	$V_{CC} = 15V$, $V_{IN} = 7.5V$ (Note 4)		600		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	$V_{CC} = 5V$	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$)	$V_{CC} = 5V$			0.7	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, $V_{CC} = 4.5V$, $I_O = -360\mu A$	2.4			V
	74C, $V_{CC} = 4.75V$, $I_O = -360\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, $V_{CC} = 4.5V$, $I_O = 360\mu A$			0.4	V
	74C, $V_{CC} = 4.75V$, $I_O = 360\mu A$			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 5V$, $V_{OUT} = 0V$, $T_A = 25°C$	-1.75	-3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	$V_{CC} = 10V$, $V_{OUT} = 0V$, $T_A = 25°C$	-8.0	-15		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 5V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	$V_{CC} = 10V$, $V_{OUT} = V_{CC}$, $T_A = 25°C$	8.0	16		mA

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Input to Output (t_{pd0} or t_{pd1})	V_{CC} = 5V		220	400	ns
	V_{CC} = 10		80	200	ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

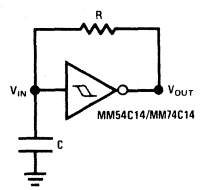
Note 2: Capacitance is guaranteed by periodic testing.

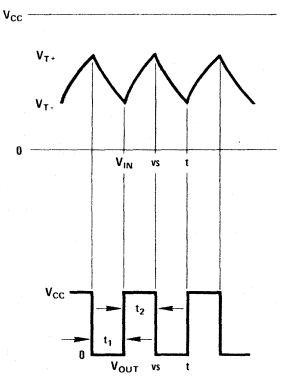
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: Only one of the six inputs is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

typical application

Low Power Oscillator





$$t_1 \approx RC \ln \frac{V_{T+}}{V_{T-}}$$

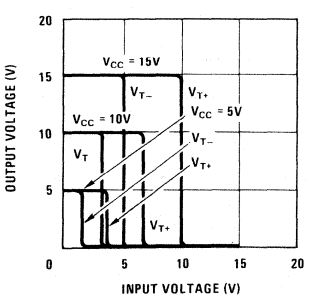
$$t_2 \approx RC \ln \frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}$$

$$f \approx \frac{1}{RC \ln \frac{V_{T+}(V_{CC} - V_{T-})}{V_{T-}(V_{CC} - V_{T+})}} \approx \frac{1}{1.7\,RC}$$

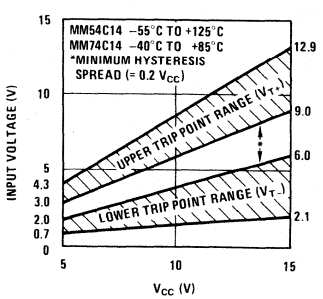
Note: The equations assume $t_1 + t_2 >> t_{pd0} + t_{pd1}$

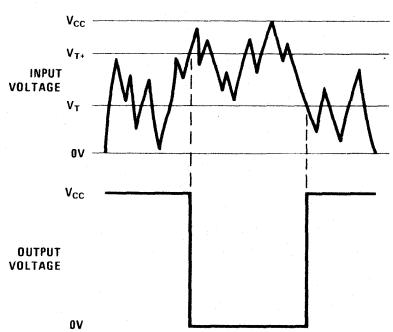
typical performance characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





Note: For more information on output drive characteristics, power dissipation, and propagation delays, see AN-90.

National Semiconductor

MM54C30/MM74C30 8-Input NAND Gate

general description

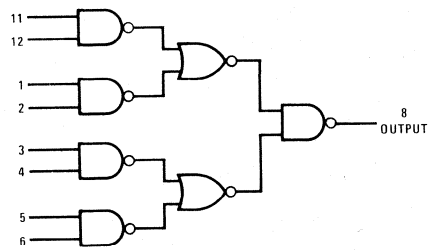
The logic gate employs complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption and high noise immunity. Function and pin out compatibility with series 54/74 devices minimizes design time for those designers familiar with the standard 54/74 logic family.

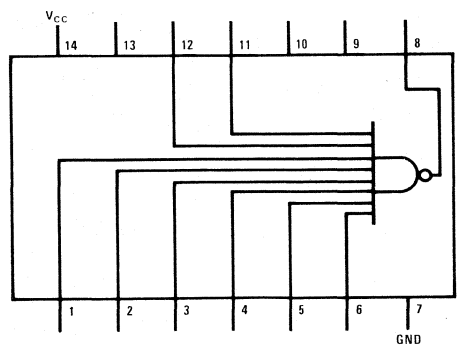
All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic and connection diagrams





TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C30	−55°C to +125°C
MM74C30	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.01	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} −1.5 V_{CC} −1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	$V_{CC} = 5.0V$ $V_{CC} = 10V$		125 55	180 90	ns ns
Input Capacitance (C_{IN})	(Note 2)		4.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Gate		26		pF

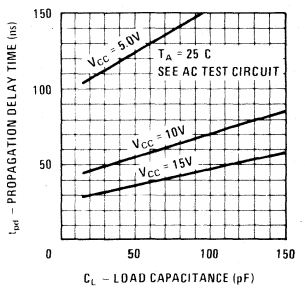
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

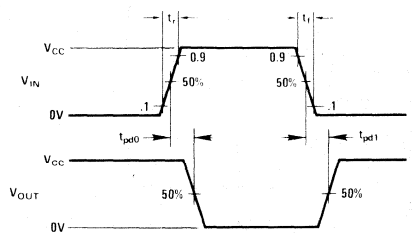
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

Propagation Delay Time vs Load Capacitance

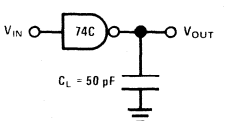


switching time waveforms



NOTE: DELAYS MEASURED WITH INPUT t_r, t_f = 20 ns.

ac test circuit



National Semiconductor

MM54C32/MM74C32 Quad 2-Input OR Gate

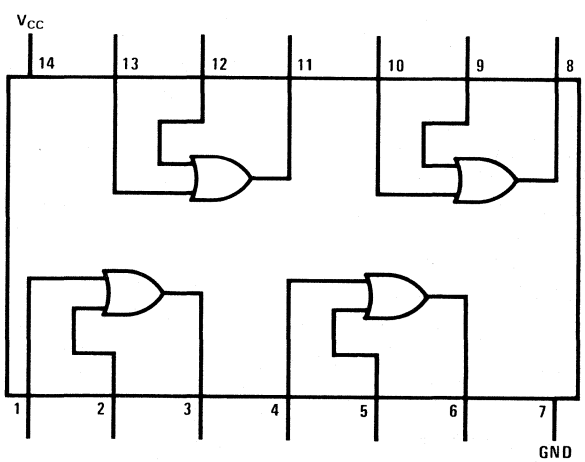
general description

Employing complementary MOS (CMOS) transistors to achieve low power and high noise margin, these gates provide the basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge damage.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagram



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C32	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C32	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	15	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C32	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C32	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C32	V_{CC} = 4.5V			0.8	V
MM74C32	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C32	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C32	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C32	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C32	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" (t_{pd1}) or "0" (t_{pd0})	V_{CC} = 5V		80	150	ns
	V_{CC} = 10V		35	70	ns
Input Capacitance (C_{IN})	Any Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{pd})	Per Gate (Note 3)		15		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

MM54C42/MM74C42 BCD-to-Decimal Decoder

general description

The MM54C42/MM74C42 one-of-ten decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. This decoder produces a logical "0" at the output corresponding to a four bit binary input from zero to nine, and a logical "1" at the other outputs. For binary inputs from ten to fifteen all outputs are logical "1".

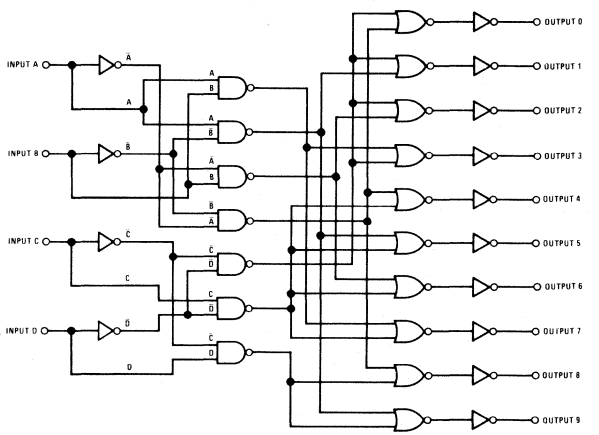
features

- Supply voltage range — 3V to 15V
- Tenth power TTL compatible — drive 2 LPTTL loads
- High noise immunity — 0.45 V_{CC} (typ.)
- Low power — 50 nW (typ.)
- Medium speed operation — 10 MHz (typ.) with 10V V_{CC}

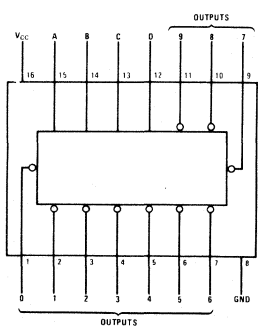
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

schematic diagram



connection diagram



truth table

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V	Storage Temperature	−65°C to +150°C
Operating Temperature MM54C42	−55°C to +125°C	Package Dissipation	500 mW
MM74C42	−40°C to +85°C	Operating V_{CC} Range	3V to 15V
Maximum V_{CC} Voltage	18V	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics Min/Max limits apply across temperature range unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage	$V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10.0V	8			V
Logical "0" Input Voltage	$V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10.0V			2	V
Logical "1" Output Voltage	$V_{OUT(1)}$	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
		V_{CC} = 10.0V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage	$V_{OUT(0)}$	V_{CC} = 5.0V, I_O = +10 μA			0.5	V
		V_{CC} = 10.0V, I_O = +10 μA			1	V
Logical "1" Input Current	$I_{IN(1)}$	V_{CC} = 15.0V, V_{IN} = 15V			1	μA
Logical "0" Input Current	$I_{IN(0)}$	V_{CC} = 15.0V, V_{IN} = 0V	−1			μA
Supply Current	I_{CC}	V_{CC} = 15.0V		0.05	300	μA
Input Capacitance		Any Input		5		pF
Propogation Delay Time to a		V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	300	ns
Logical "0" or Logical "1"		V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	140	ns
CMOS TO TENTH POWER INTERFACE						
Logical "1" Input Voltage	$V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
		74C, V_{CC} = 4.75V				
Logical "0" Input Voltage	$V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V				
Logical "1" Output Voltage	$V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360 μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −360 μA				
Logical "0" Output Voltage	$V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
Output Source Current (I_{SOURCE})		V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	−1.75			mA
		T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})		V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
		T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})		V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
		T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})		V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
		T_A = 25°C, V_{OUT} = V_{CC}				

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

National Semiconductor

MM54C48/MM74C48 BCD-to-7 Segment Decoder

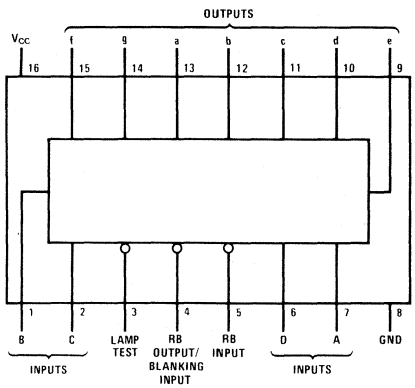
general description

The MM54C48/MM74C48 BCD-to-7 segment decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Seven NAND gates and one driver are connected in pairs to make binary-coded decimal (BCD) data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide test blanking input/ripple-blanking output, and ripple-blanking inputs.

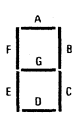
features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power fan out of 2
  TTL compatibility driving 74L
- High current sourcing output (up to 50 mA)
- Ripple blanking for leading or trailing zeros (optional)
- Lamp test provision

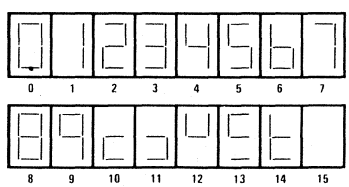
connection diagram



TOP VIEW



Segment Identification



Numerical Designations and Resultant Displays

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C48	−55°C to +125°C
MM74C48	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (RB Output Only)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$) (RB Output Only)	54C, V_{CC} = 4.5V, I_O = −50μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −50μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel) (RB Output Only)	V_{CC} = 4.75V, V_{OUT} = 0.4V			−0.80	mA
	V_{CC} = 10V, V_{OUT} = 0.5V			-4.0	mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA
Output Source Current (NPN Bipolar)	V_{CC} = 5.0V, V_{OUT} = 3.4	-20	-50		mA
	V_{CC} = 5.0V, V_{OUT} = 3.0		-65		mA
	V_{CC} = 10V, V_{OUT} = 8.4	-20	-50		mA
	V_{CC} = 10V, V_{OUT} = 8.0		-65		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

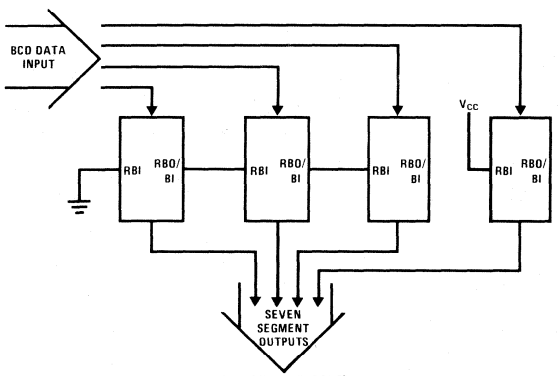
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a "1" or "0" on Segment Outputs from Data Inputs	$V_{CC} = 5.0V$		450	1500	ns
	$V_{CC} = 10V$		160	500	ns
Propagation Delay to a "0" on Segment Outputs from RB Input	$V_{CC} = 5.0V$		500	1600	ns
	$V_{CC} = 10V$		180	550	ns
Propagation Delay to a "0" on Segment Outputs from Blanking Input	$V_{CC} = 5.0V$		350	1200	ns
	$V_{CC} = 10V$		140	450	ns
Propagation Delay to a "1" on Segment Outputs from Lamp Test	$V_{CC} = 5.0V$		450	1500	ns
	$V_{CC} = 10V$		160	500	ns
Propagation Delay to a "1" on RB Output from RB Input	$V_{CC} = 5.0V$		600	2000	ns
	$V_{CC} = 10V$		250	800	ns
Propagation Delay to a "0" on RB Output from RB Input	$V_{CC} = 5.0V$		140	450	ns
	$V_{CC} = 10V$		50	150	ns

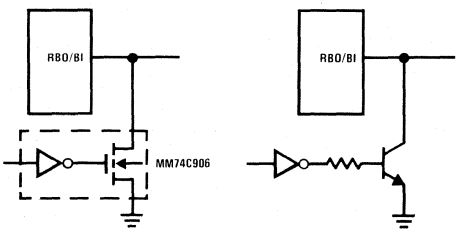
typical applications

Typical Connection Utilizing the Ripple-Blanking Feature



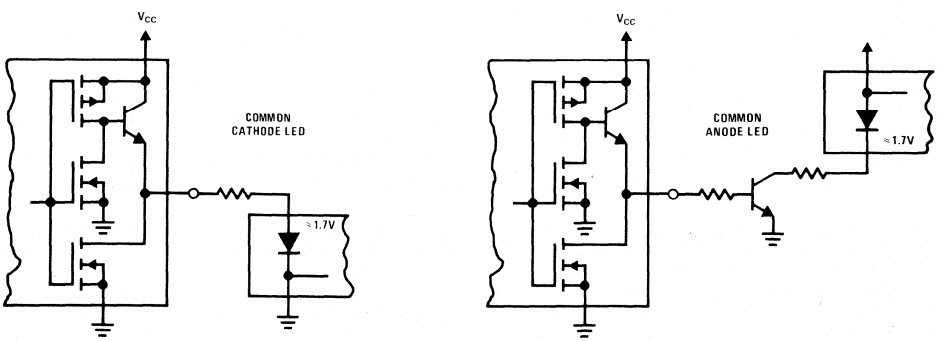
(First three stages will blank leading zeros, the fourth stage will not blank zeros)

Blanking Input Connection Diagram



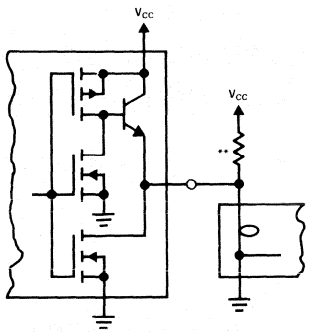
(When RBO/BI is forced low, all segment outputs are off regardless of the state of any other input condition)

Light Emitting Diode (LED) Readout



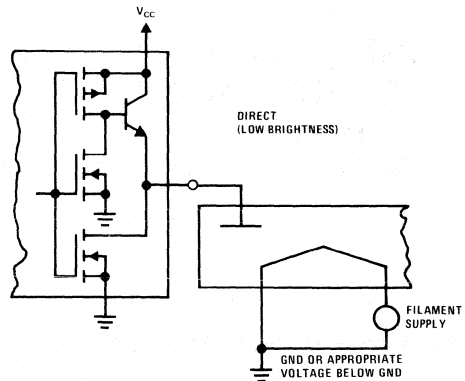
typical applications (con't)

Incandescent Readout

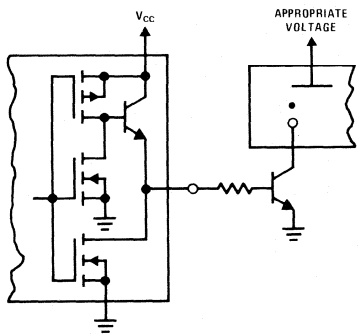


**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

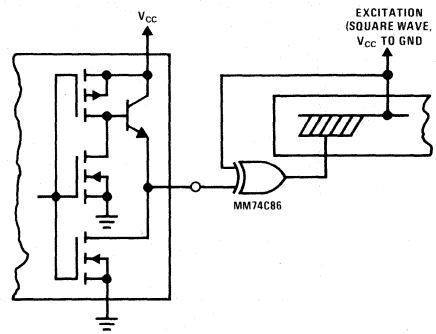
Fluorescent Readout



Gas Discharge Readout



Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

truth table

DECIMAL OR FUNCTION	INPUTS						BI/RBO†	OUTPUTS							NOTE
	LT	RBI	D	C	B	A		a	b	c	d	e	f	g	
0	H	H	L	L	L	L	H	H	H	H	H	H	H	L	1
1	H	X	L	L	L	H	H	L	H	H	L	L	L	L	1
2	H	X	L	L	H	L	H	H	H	L	H	H	L	H	
3	H	X	L	L	H	H	H	H	H	H	H	L	L	H	
4	H	X	L	H	L	L	H	L	H	H	L	L	H	H	
5	H	X	L	H	L	H	H	H	L	H	H	L	H	H	
6	H	X	L	H	H	L	H	L	L	H	H	H	H	H	
7	H	X	L	H	H	H	H	H	H	H	L	L	L	L	
8	H	X	H	L	L	L	H	H	H	H	H	H	H	H	
9	H	X	H	L	L	H	H	H	H	H	L	L	H	H	
10	H	X	H	L	H	L	H	L	L	L	H	H	L	H	
11	H	X	H	L	H	H	H	L	L	H	H	L	L	H	
12	H	X	H	H	L	L	H	L	H	L	L	L	H	H	
13	H	X	H	H	L	H	H	H	L	L	H	L	H	H	
14	H	X	H	H	H	L	H	L	L	L	H	H	H	H	
15	H	X	H	H	H	H	H	L	L	L	L	L	L	L	
BI	X	X	X	X	X	X	L	L	L	L	L	L	L	L	2
RBI	H	L	L	L	L	L	L	L	L	L	L	L	L	L	3
LT	L	X	X	X	X	X	H	H	H	H	H	H	H	H	4

H = high level, L = low level, X = irrelevant

Note 1: The blanking input (BI) must be open when output functions 0–15 are desired. The ripple-blanking input (RBI) must be high, if blanking of a decimal zero is not desired.

Note 2: When a low logic level is applied directly to the blanking input (BI), all segment outputs are low regardless of the level of any other input.

Note 3: When ripple-blanking input (RBI) and inputs A, B, C, and D are at a low level with the lamp-test input high, all segment outputs go low and the ripple-blanking output (RBO) goes to a low level (response condition).

Note 4: When the blanking input/ripple-blanking output (BI/RBO) is open and a low is applied to the lamp-test input, all segment outputs are high.

† One BI/RBO is wire-AND logic serving as blanking input (BI) and/or ripple-blanking output (RBO).

National Semiconductor

MM54C73/MM74C73 Dual J-K Flip-Flops with Clear
MM54C76/MM74C76 Dual J-K Flip-Flops with Clear and Preset
MM54C107/MM74C107 Dual J-K Flip-Flops with Clear

general description

These dual J-K flip - flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement transistors. Each flip-flop has independent J, K, clock and clear inputs and Q and $\overline{Q}$ outputs. The MM54C76/MM74C76 flip flops also include preset inputs and are supplied in 16 pin packages. These flip flops are edge sensitive to the clock input and change state on the negative going transition of the clock pulses. Clear or preset is independent of the clock and is accomplished by a low level on the respective input.

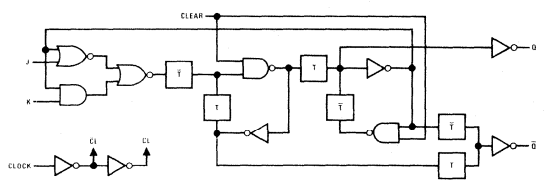
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

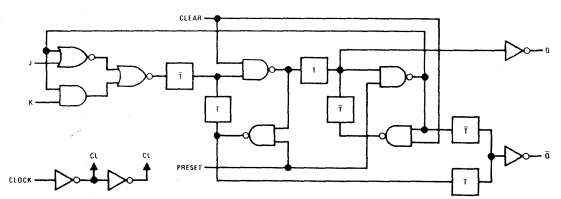
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams

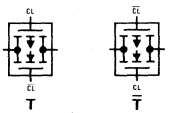


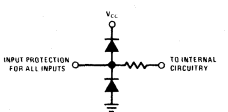
MM54C73/MM74C73 and MM54C107/MM74C107

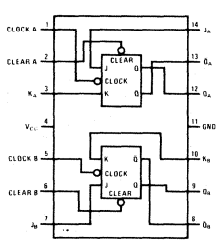


MM54C76/MM74C76

Transmission Gate

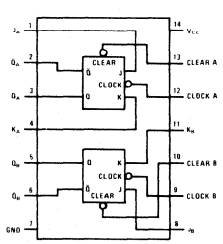






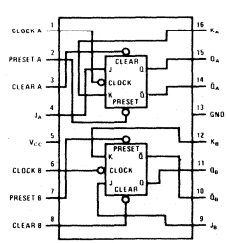
Note: A logic "0" on clear sets Q to logic "0."

MM54C73/MM74C73



Note: A logic "0" on clear sets Q to logic "0."

MM54C107/MM74C107



Note 1: A logic "0" on clear sets Q to a logic "0."
Note 2: A logic "0" on preset sets Q to a logic "1."

MM54C76/MM74C76

absolute maximum ratings

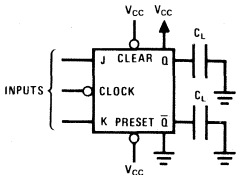
Voltage at any pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature MM54CXX	−55°C to 125°C
MM74CXX	−40°C to +85°C
Storage Temperature	−65°C to 150°C
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 sec)	300°C
Operating V_{CC} Range	+3V to 15V

electrical characteristics

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	3.5 8			V V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			1.5 2.0	V V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V V_{CC} = 10.0V	4.5 9.0			V V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V V_{CC} = 10.0V			0.5 1.0	V V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	60	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		180 70	300 110	ns ns
Propagation Delay Time to a Logical "0" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Propagation Delay Time to a Logical "1" From Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.V, C_L = 50 pF, T_A = 25°C		200 80	300 130	ns ns
Time Prior to Clock Pulse That Data Must be Present, t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		110 45	175 70	ns ns
Time After Clock Pulse That J and K Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−40 −20	0 0	ns ns
Minimum Clock Pulse Width t_{WL} = t_{WH}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		120 50	190 80	ns ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90 40	130 60	ns ns
Maximum Toggle Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	2.5 7.0	4.0 11.0		MHz MHz
Clock Pulse Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C			15 5	μs μs
LOW POWER TTL TO CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Votlage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_0 = −360μA 74C, V_{CC} = 4.75V, I_0 = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_0 = 360μA 74C, V_{CC} = 4.75V, I_0 = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	-1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	-8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac test circuit



truth table

t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

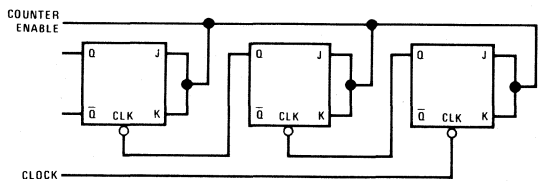
t_n = bit time before clock pulse.
t_{n+1} = bit time after clock pulse.

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	*Q_n	*$\overline{Q}_n$

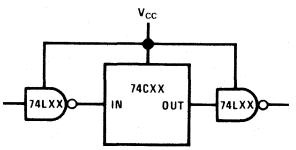
*No change in output from previous state.

typical applications

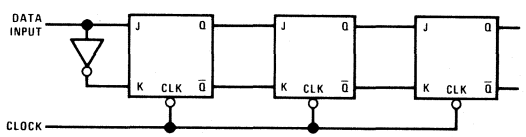
Ripple Binary Counters



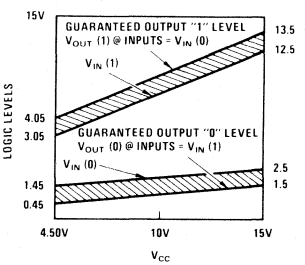
74C Compatibility



Shift Registers

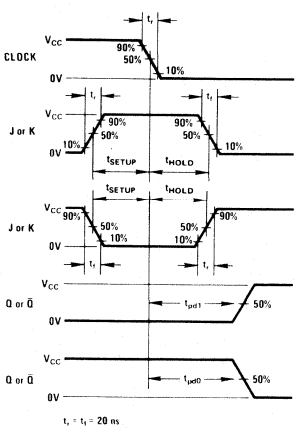


Guaranteed Noise Margin as a Function of V_{CC}



switching time waveforms

CMOS to CMOS



$t_r = t_f = 20$ ns

National Semiconductor

MM54C74/MM74C74 Dual D Flip-Flop

general description

The MM54C74/MM74C74 dual D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. Each flip flop has independent data, preset, clear and clock inputs and Q and $\overline{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive going transition of the clock pulse. Preset or clear is independent of the clock and accomplished by a low level at the preset or clear input.

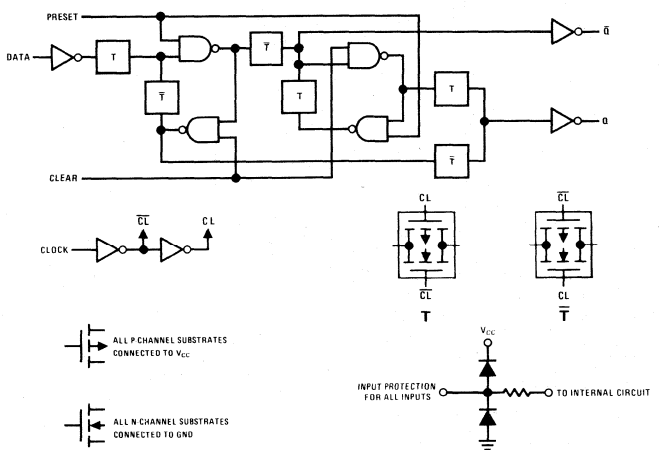
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2LPT^{2}L loads
■ High noise immunity	0.45 V_{CC} (typ)
■ Low power	50 nW (typ)
■ Medium speed operation	10 MHz (typ) with 10V supply

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

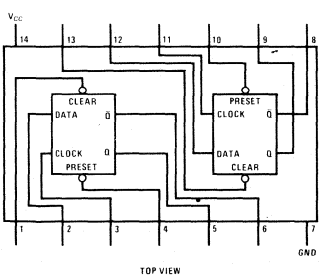
logic and connection diagrams



truth table

Preset	Clear	Q_n	$\overline{Q}_n$
0	0	0	0
0	1	1	0
1	0	0	1
1	1	$^*Q_n$	$^*\overline{Q}_n$

*No change in output from previous state.



TOP VIEW

Note: A logic "0" on clear sets Q to logic "0."
A logic "0" on preset sets Q to logic "1."

absolute maximum ratings

Voltage at any pin (Note 1)	−0.3V to V_{CC} + 0.3V
Operating temperature MM54C74	−55°C to 125°C
MM74C74	−40°C to +85°C
Storage temperature	−65°C to 150°C
Maximum V_{CC} Voltage	18V
Package dissipation	500 mW
Lead temperature (Soldering, 10 sec)	300°C
Operating V_{CC} range	+3V to +15V

electrical characteristics

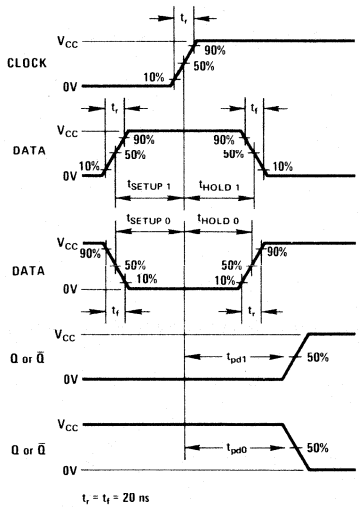
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	60	μA
Input Capacitance	Any Input		5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "0" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay Time to a Logical "1" from Preset or Clear	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		250	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		100	150	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	100	50		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	40	20		ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		−20	0	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		−8.0	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	250	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40	100	ns
Minimum Preset and Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	160	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		40	70	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	15.0			μs
	V_{CC} = 10.0V, C_L = 50 pF	5.0			μs
Maximum Clock Frequency	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	2.0	3.5		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	5.0	8.0		MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.75V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = − 360 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = − 360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.50V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	−1.75			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

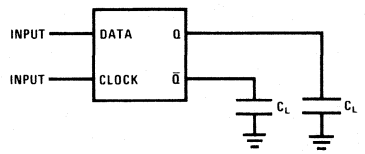
Note 1: These devices should not be connected under power on conditions.

switching time waveforms

CMOS to CMOS

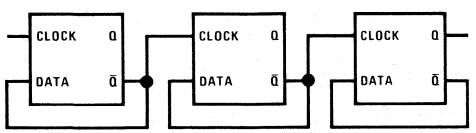


ac test circuit

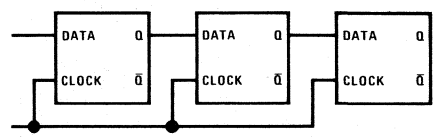


typical applications

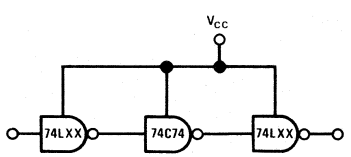
Ripple Counter (Divide by 2^n)



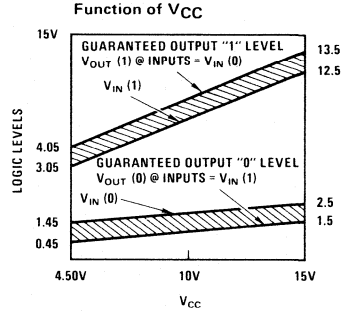
Shift Register



74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



National Semiconductor

MM54C83/MM74C83 4-Bit Binary Full Adder

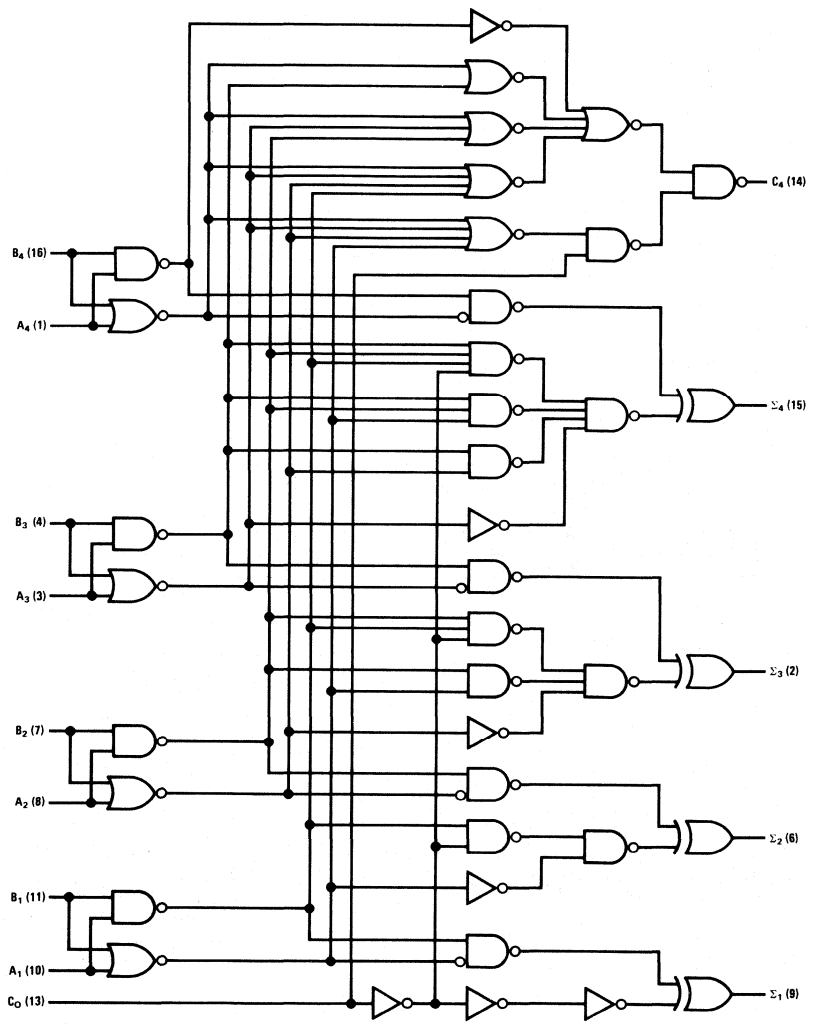
general description

The MM54C83/MM74C83 4-bit binary full adder performs the addition of two 4-bit binary numbers, A carry input (C_0) is included and the sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Since the carry-ripple-time is the limiting delay in the addition of a long word length, carry look-ahead circuitry has been included in the design to minimize this delay. Also, the logic levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

features

■ Wide supply voltage range	3V to 15V
■ Guaranteed noise margin	1V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L
■ Fast carry ripple (C_0 to C_4)	50 ns typ @ V_{CC} = 10V and C_L = 50 pF
■ Fast summing (Σ_{IN} to Σ_{OUT})	125 ns typ @ V_{CC} = 10V and C_L = 50 pF

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C83	−55°C to +125°C
MM74C83	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

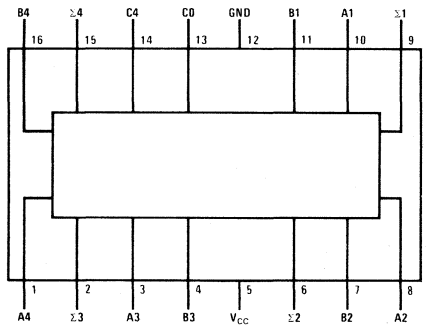
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

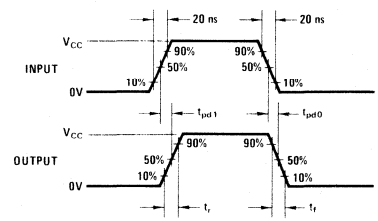
ac electrical characteristics $T_A = 25^\circ C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from C_0 to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		120	200	ns
	$V_{CC} = 10V$		50	80	ns
Propagation Delay from Sum Inputs to C_4 (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		250	450	ns
	$V_{CC} = 10V$		90	150	ns
Propagation Delay from C_0 to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		350	550	ns
	$V_{CC} = 10V$		125	200	ns
Propagation Delay from Sum Inputs to Sum Outputs (t_{PD0} or t_{PD1})	$V_{CC} = 5.0V$		300	550	ns
	$V_{CC} = 10V$		110	180	ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	Per Package (Note 3)		120		pF

connection diagram



switching time waveforms



Inputs must be tied to appropriate logic level.

truth table

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	L	H	H	H	H	H	L

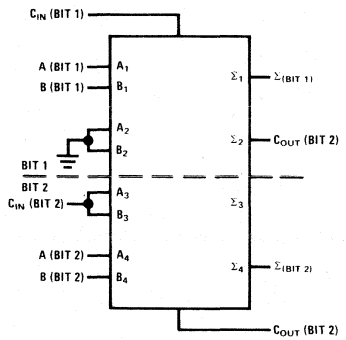
H = high level, L = low level

Note: Input conditions at A3, A2, B2 and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

typical applications

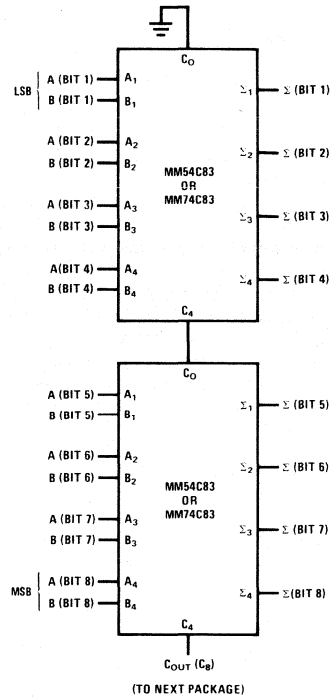
APPLICATION

Connect the MM54C83/MM74C83 in the following manner to implement a dual single bit full adder.



CASCADING

Connect the MM54C83/MM74C83 in the following manner to implement full adders with more than 4 bits.



National Semiconductor

MM54C85/MM74C85 4-Bit Magnitude Comparator

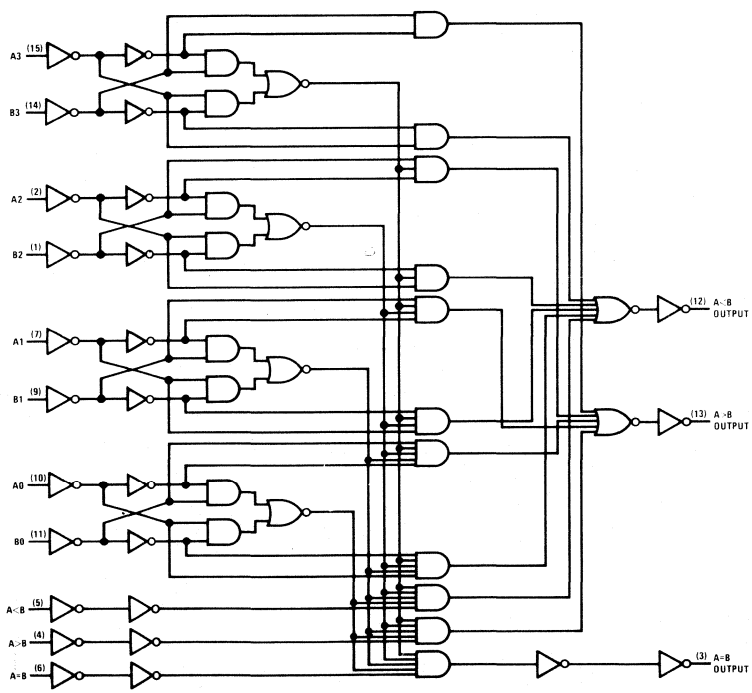
general description

The MM54C85/MM74C85 is a four-bit magnitude comparator which will perform comparison of straight binary or BCD codes. The circuit consists of eight comparing inputs (A0, A1, A2, A3, B0, B1, B2, B3), three cascading inputs (A>B, A<B and A=B), and three outputs (A>B, A<B and A=B). This device compares two four-bit words (A and B) and determines whether they are "greater than," "less than," or "equal to" each other by a high level on the appropriate output. For words greater than four-bits, units can be cascaded by connecting the outputs (A>B, A<B, and A=B) of the least-significant stage to the cascade inputs (A>B, A<B and A=B) of the next-significant stage. In addition the least significant stage must have a high level voltage ($V_{IN(1)}$) applied to the A=B input and low level voltages ($V_{IN(0)}$) applied to A>B and A<B inputs.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Expandable to 'N' stages
- Applicable to binary or BCD
- The MM54C85/MM74C85 follows the MM54L85/MM74L85 Pinout.

logic diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C85	−55°C to +125°C
MM74C85	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC} − 1.5 V_{CC} − 1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time from any A or B Data Input to any Data Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V V_{CC} = 10V		250 100	600 300	ns ns
Propagation Delay Time from any Cascade Input to any Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V V_{CC} = 10V		200 100	500 250	ns ns
Input Capacitance	Any Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3) Per Package		45		pF

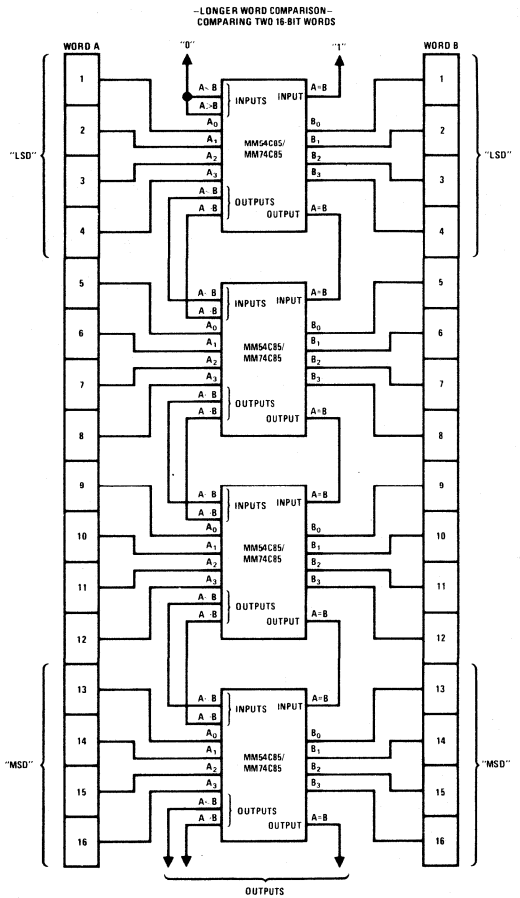
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

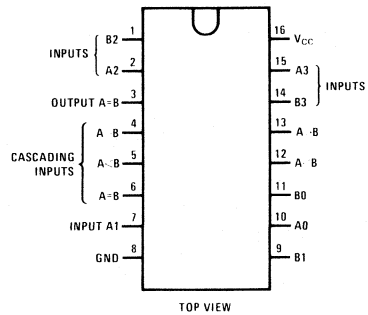
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical application

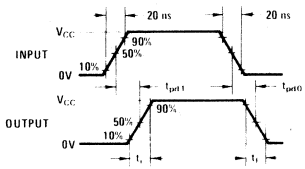
Four Digit Comparator



connection diagram



switching time waveform



Unused inputs must be tied to an appropriate logic level.

truth table

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	H	L	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	H	H	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	H	H	H	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	H	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L

H = high level, L = low level, X = irrelevant

National Semiconductor

MM54C89/MM74C89 64-Bit TRI-STATE® Random Access Read/Write Memory

general description

The MM54C89/MM74C89 is a 16-word by 4-bit random access read/write memory. Inputs to the memory consist of four address lines, four data input lines, a write enable line and a memory enable line. The four binary address inputs are decoded internally to select each of the 16 possible word locations. An internal address register, latches the address information on the positive to negative transition of the memory enable input. The four TRI-STATE® data output lines working in conjunction with the memory enable input provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of memory enable. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition of memory enable).

Note: The timing is different than the DM7489 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

Write Operation: Information present at the data inputs is written into the memory at the selected address by bringing write enable and memory enable low.

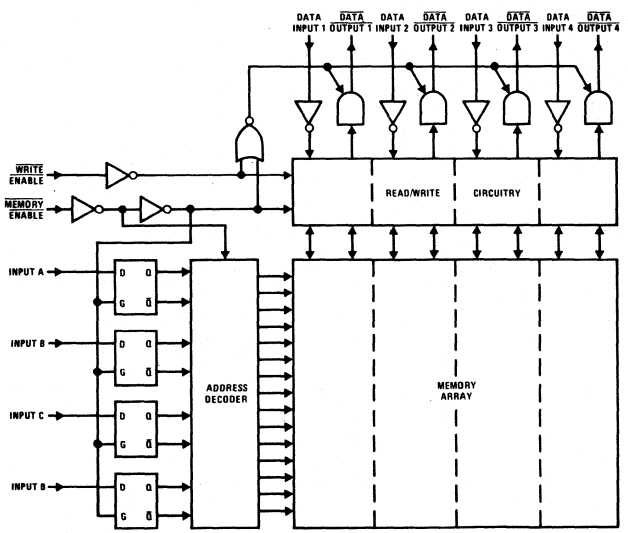
Read Operation: The complement of the information which was written into the memory is non-destructively read out at the four outputs. This is accomplished by selecting the desired address and bringing memory enable low and write enable high.

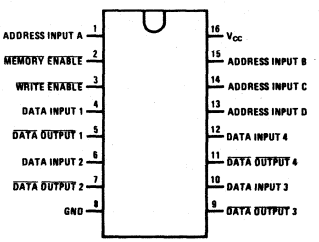
When the device is writing or disabled the output assumes a TRI-STATE (Hi-z) condition.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Input address register
- Low power consumption — 100 nW/package typ @ V_{CC} = 5V
- Fast access time — 130 ns typ at V_{CC} = 10V
- TRI-STATE output

logic and connection diagrams





TOP VIEW

Order Number MM54C89D or MM74C89D
See Package 3
Order Number MM74C89N
See Package 15

absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C89	−55°C to +125°C
MM74C89	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
	V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = +360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics (T_A = 25°C, C_L = 50 pF, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from $\overline{\text{Memory Enable}}$ (t_{pd})	V_{CC} = 5.0V		270	500	ns
	V_{CC} = 10V		100	220	ns
Access Time from Address Input (t_{acc})	V_{CC} = 5.0V		350	650	ns
	V_{CC} = 10V		130	280	ns
Address Input Setup Time (t_{SA})	V_{CC} = 5.0V	150			ns
	V_{CC} = 10V	60			ns
Address Input Hold Time (t_{HA})	V_{CC} = 5.0V	60			ns
	V_{CC} = 10V	40			ns
$\overline{\text{Memory Enable}}$ Pulse Width (t_{ME})	V_{CC} = 5.0V	400	250		ns
	V_{CC} = 10V	150	90		ns
$\overline{\text{Memory Enable}}$ Pulse Width ($t_{\overline{ME}}$)	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	150	70		ns

ac electrical characteristics (cont.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Read (t_{SR})	V_{CC} = 5.0V	0			ns
	V_{CC} = 10V	0			ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Setup Time for a Write (t_{WS})	V_{CC} = 5.0V			t_{ME}	ns
	V_{CC} = 10V			t_{ME}	ns
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V, t_{WS} = 0	300	160		ns
	V_{CC} = 10V, t_{WS} = 0	100	60		ns
Data Input Hold Time (t_{HD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Data Input Setup (t_{SD})	V_{CC} = 5.0V	50			ns
	V_{CC} = 10V	25			ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Memory}}$ $\overline{\text{Enable}}$ (t_{IH}, t_{OH})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Propagation Delay from a Logical "1" or Logical "0" to the High Impedance State from $\overline{\text{Write}}$ $\overline{\text{Enable}}$ (t_{IH}, t_{OH})	V_{CC} = 5.0V, C_L = 5.0 pF, R_L = 10k		180	300	ns
	V_{CC} = 10V, C_L = 5.0 pF, R_L = 10k		85	120	ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity (C_{OUT})	Any Output (Note 2)		6.5		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		230		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics (con't)

(Guaranteed across the specified temperature range, C_L = 50 pF)

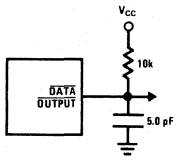
PARAMETER	CONDITIONS	MM54C89 T_A = −55°C to +125°C		MM74C89 T_A = −40°C to +85°C		UNITS
		MIN	MAX	MIN	MAX	
t_{PD}	V_{CC} = 5 V		700		600	ns
	V_{CC} = 10 V		310		265	ns
	V_{CC} = 15 V		250		210	ns
t_{ACC}	V_{CC} = 5 V		910		780	ns
	V_{CC} = 10 V		400		345	ns
	V_{CC} = 15 V		320		270	ns
t_{SA}	V_{CC} = 5 V	210		180		ns
	V_{CC} = 10 V	90		80		ns
	V_{CC} = 15 V	70		60		ns
t_{HA}	V_{CC} = 5 V	80		70		ns
	V_{CC} = 10 V	55		50		ns
	V_{CC} = 15 V	45		40		ns
t_{ME}	V_{CC} = 5 V	560		480		ns
	V_{CC} = 10 V	210		180		ns
	V_{CC} = 15 V	170		150		ns
$t_{\overline{ME}}$	V_{CC} = 5 V	560		480		ns
	V_{CC} = 10 V	210		180		ns
	V_{CC} = 15 V	170		150		ns
$t_{\overline{WE}}$	V_{CC} = 5 V	420		360		ns
	V_{CC} = 10 V	140		120		ns
	V_{CC} = 15 V	110		100		ns
t_{HD}	V_{CC} = 5 V	70		60		ns
	V_{CC} = 10 V	35		30		ns
	V_{CC} = 15 V	30		25		ns
t_{SA}	V_{CC} = 5 V	70		60		ns
	V_{CC} = 10 V	35		30		ns
	V_{CC} = 15 V	30		25		ns
t_{IH}, t_{OH}	V_{CC} = 5 V, C_L = 5 pF		420		360	ns
	V_{CC} = 10 V, R_L = 10 kΩ		170		145	ns
	V_{CC} = 15 V		135		115	ns

truth table

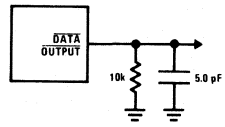
ME	WE	OPERATION	CONDITION OF OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Complement of Selected Word
H	L	Inhibit, Storage	TRI-STATE
H	H	Inhibit, Storage	TRI-STATE

ac test circuits

t_{0H}

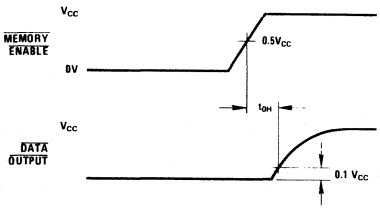


t_{1H}

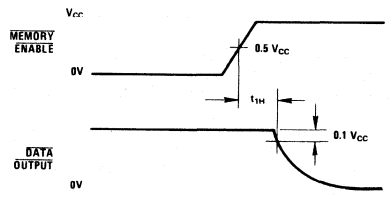


switching time waveforms

t_{0H}

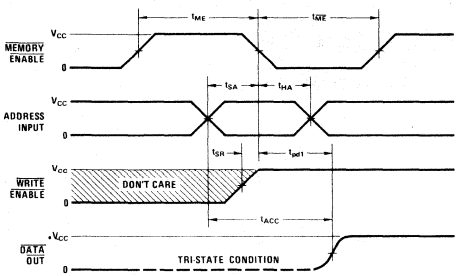


t_{1H}

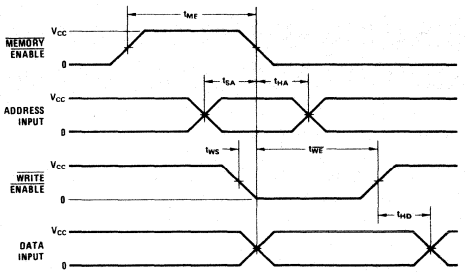


switching time waveforms (con't)

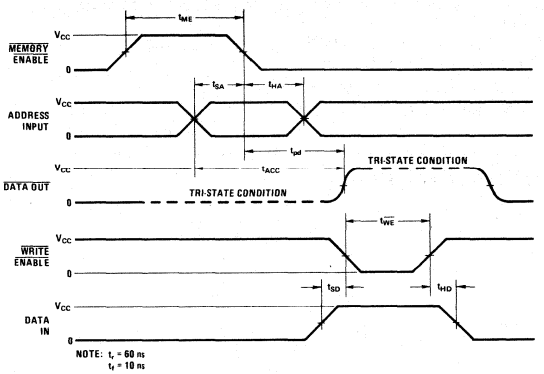
Read Cycle



Write Cycle



Read Modify Write Cycle



National Semiconductor

MM54C90/MM74C90 4-Bit Decade Counter
MM54C93/MM74C93 4-Bit Binary Counter

general description

The MM54C90/MM74C90 decade counter and the MM54C93/MM74C93 binary counter are complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The 4-bit decade counter can be reset to zero or preset to nine by applying appropriate logic level on the R_{01}, R_{02}, R_{91} and R_{92} inputs, also a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, 5 or 10 frequency counter. The 4-bit binary counter can be reset to zero by applying high logic level on inputs R_{01} and R_{02}, also a separate flip-flop on the A-bit enables the user to operate it as a divide-by-2, -8, or -16 divider. Counting occurs on the negative-going edge of the input pulse.

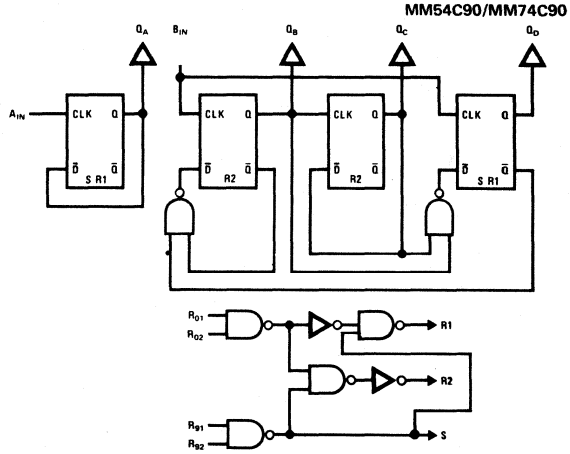
All inputs are protected against static discharge damage.

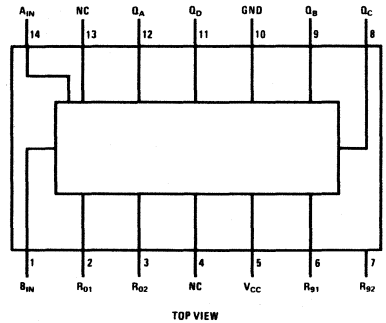
features

- Wide supply voltage range — 3V to 15V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — fan out of 2
  TTL compatibility — driving 74L
- The MM54C93/MM74C93 follows the MM54L93/MM74L93 Pinout

logic and connection diagrams

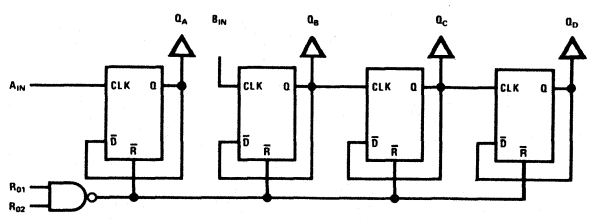
MM54C90/MM74C90

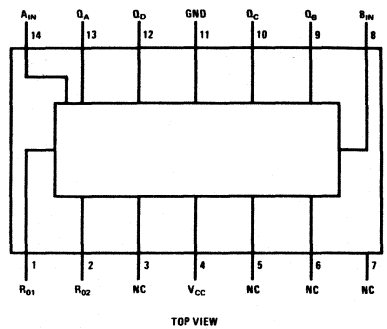




TOP VIEW

MM54C93/MM74C93





TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V	Operating V_{CC} Range	3V to 15V
Operating Temperature Range		Absolute Maximum V_{CC}	18V
MM54C90, MM54C93	−55°C to +125°C	Storage Temperature Range	−65°C to +150°C
MM74C90, MM74C93	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	500 mW		

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Volage ($V_{IN(1)}$)					
MM54C90, MM54C93	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C90, MM74C93	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C90, MM54C93	V_{CC} = 4.5V			0.8	V
MM74C90, MM74C93	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C90, MM54C93	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C90, MM74C93	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C90, MM54C93	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C90, MM74C93	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		200	400	ns
Q_A (t_{pd0} or t_{pd1})	V_{CC} = 10V		80	150	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		450	850	ns
Q_B (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 10V		160	300	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		450	800	ns
Q_B (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 10V		160	300	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		500	1050	ns
Q_C (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 10V		200	400	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		500	1000	ns
Q_C (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 10V		200	400	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		600	1200	ns
Q_D (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 10V		250	500	ns
Propagation Delay Time From A_{IN} to	V_{CC} = 5V		450	800	ns
Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 10V		160	300	ns

ac electrical characteristics (con't)

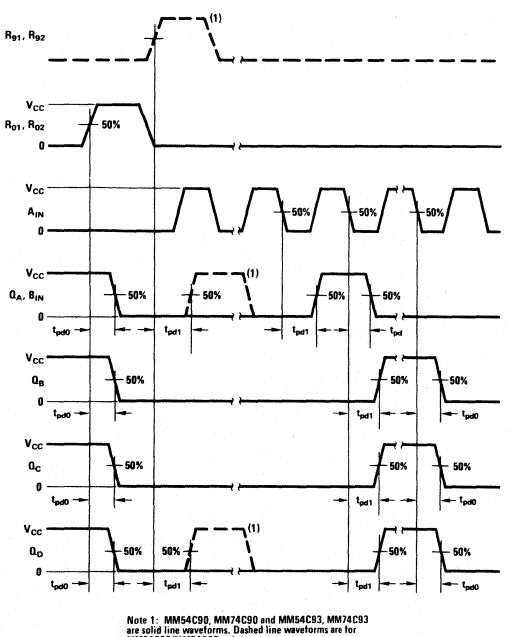
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (t_{pd0} or t_{pd1}) (MM54C93/MM74C93)	V_{CC} = 5V V_{CC} = 10V		150 75	300 150	ns ns
Propagation Delay Time From R_{01} or R_{02} to Q_A, Q_B, Q_C or Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		200 75	400 150	ns ns
Propagation Delay Time From R_{91} or R_{92} to Q_A or Q_D (t_{pd0} or t_{pd1}) (MM54C90/MM74C90)	V_{CC} = 5V V_{CC} = 10V		250 100	500 200	ns ns
Min R_{01} or R_{02} Pulse Width (MM54C93/MM74C93)	V_{CC} = 5 V V_{CC} = 10 V	600 300	250 125		ns ns
Min R_{01} or R_{02} Pulse Width (MM54C90/MM74C90)	V_{CC} = 5 V V_{CC} = 10 V	600 300	250 125		ns ns
Min R_{91} or R_{92} Pulse Width (MM54C90/MM74C90)	V_{CC} = 5 V V_{CC} = 10 V	500 250	200 100		ns ns
Maximum Clock Rise and Fall Time	V_{CC} = 5V V_{CC} = 10V			15 5	μs μs
Minimum Clock Pulse Width (t_W)	V_{CC} = 5V V_{CC} = 10V	250 100	100 50		ns ns
Maximum Clock Frequency	V_{CC} = 5V V_{CC} = 10V	2 5			MHz MHz
Input Capacitance	Any Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	Per Package (Note 3)		45		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

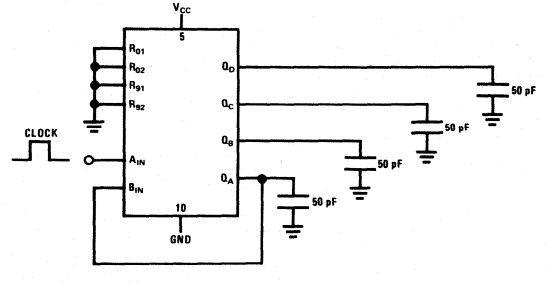
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms and ac test circuits

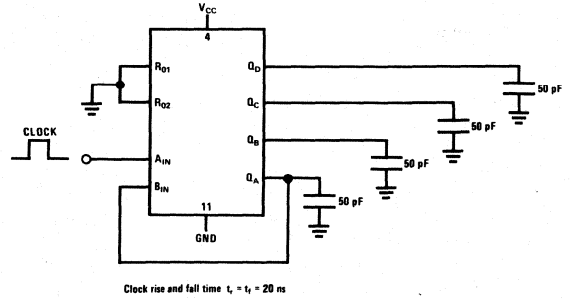


Note 1: MM54C90, MM74C90 and MM54C93, MM74C93 are solid line waveforms. Dashed line waveforms are for MM54C90/MM74C90 only.



Clock rise and fall time $t_r = t_f$ = 20 ns

MM54C90/MM74C90



Clock rise and fall time $t_r = t_f$ = 20 ns

MM54C93/MM74C93

truth tables

MM54C90/MM74C90 4-Bit Decade Counter

BCD Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Output Q_A is connected to input B for BCD count.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS				OUTPUT			
R_{01}	R_{02}	R_{91}	R_{92}	Q_D	Q_C	Q_B	Q_A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

MM54C93/MM74C93 4-Bit Binary Counter

Binary Count Sequence

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Output Q_A is connected to input B for binary count sequence.

H = High level
L = Low level
X = Irrelevant

Reset/Count Function Table

RESET INPUTS		OUTPUT			
R_{01}	R_{02}	Q_D	Q_C	Q_B	Q_A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

National Semiconductor

MM54C95/MM74C95 4-Bit Right-Shift Left-Shift Register

general description

This 4-bit shift register is a monolithic complementary MOS (CMOS) integrated circuit composed of four D flip flops. This register will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an N-bit right shift or left shift register.

When a logical "0" level is applied to the mode control input, the output of each flip flop is coupled to the D input of the succeeding flip flop. Right-shift operation is performed by clocking at the clock 1 input, and serial data entered at the serial input, clock 2 and parallel inputs A through D are inhibited. With a logical "1" level applied to the mode control, outputs to succeeding stages are decoupled and parallel loading is possible, or with external interconnection, shift-left operation can be accomplished by connecting the output of each flip flop to the parallel input of the previous flip flop and serial data is entered at input D.

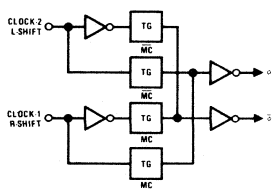
features

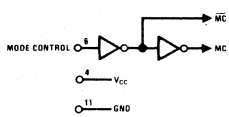
- Medium speed operation — 10 MHz typ (V_{CC} = 10V, C_L = 50 pF
- High noise immunity — 0.45 V_{CC} typ
- Low power — 100 nW typ
- Tenth power TTL compatible — Drive 2 LTTL loads
- Wide supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip flop
- Negative edge triggered clocking
- The MM54C95/MM74C95 follows the MM54L95/MM74L95 Pinout.

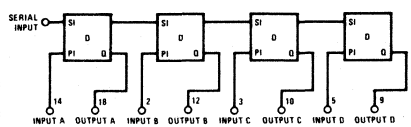
applications

- Data terminals
- Instrumentation
- Automotive
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

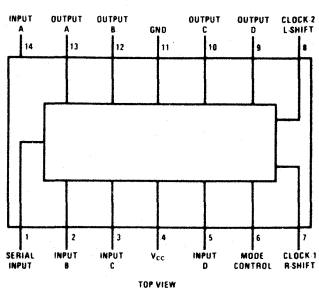
block and connection diagrams







Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V	Maximum V_{CC} Voltage	18V
Operating Temperature	MM54C95	−55°C to +125°C	Package Dissipation	500 mW
	MM74C95	−40°C to +85°C	Operating V_{CC} Range	+3V to +15V
Storage Temperature		−65°C to +150°C	Lead Temperature (Soldering, 10 sec)	300°C

electrical characteristics

Max/min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} From Clock to Q or $\overline{Q}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	160	ns
Time Prior to Clock Pulse That Data Must be Preset t_{SETUP}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	60	30		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	25	10		ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	25	10		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	10	50		ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		50		ns
Time Prior to Clock Pulse that Mode Control must be Present	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	200	100		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	100	50		ns
Maximum Input Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	3	5		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	6.5	10		MHz
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_D = 360 μA	2.4			V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_D = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_D = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	−1.75			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

Note 1: These devices should not be connected under "Power On" conditions.

function table

INPUTS								OUTPUTS			
MODE CONTROL	CLOCKS		SERIAL	PARALLEL							
	2 (L)	1 (R)		A	B	C	D	Q_A	Q_B	Q_C	Q_D
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B†	Q_C†	Q_D†	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	L	H	X	X	X	X	X	Undefined			
↓	H	L	X	X	X	X	X	Operating Conditions			

†Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C or D, respectively.

Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the most-recent ↓ transition of the clock.

National Semiconductor

MM54C150/MM74C150 16-Line to 1-Line Multiplexer MM72C19/MM82C19 TRI-STATE® 16-Line to 1-Line Multiplexer

general description

The MM54C150/MM74C150 and MM72C19/MM82C19 multiplex 16 digital lines to 1 output. A 4-bit address code determines the particular 1-of-16 inputs which is routed to the output. The data is inverted from input to output.

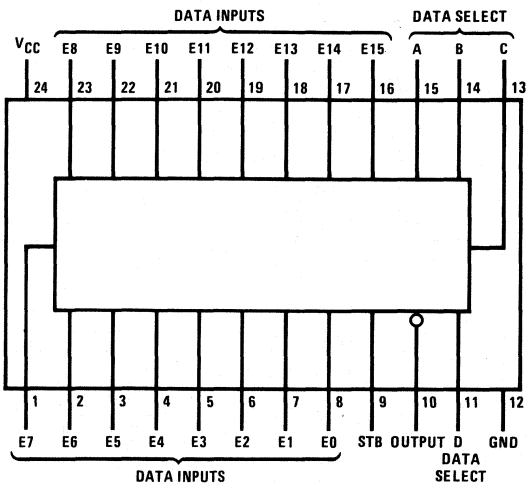
A strobe override places the output of MM54C150/MM74C150 in the logical "1" state and the output of MM72C19/MM82C19 in the high-impedance state.

All inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	Drive 1 TTL Load

connection diagram



absolute maximum ratings

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C150, MM72C19	−55°C to +125°C
MM74C150, MM82C19	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V, I_O = −10μA	4.5			V
		V_{CC} = 10V, I_O = −10μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = +10μA			0.5	V
		V_{CC} = 10V, I_O = +10μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	Output Current in High Impedance State					
	MM72C19/MM82C19	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C,72C V_{CC} = 4.5V	V_{CC}−1.5			V
		74C,82C V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C,72C V_{CC} = 4.5V			0.8	V
		74C,82C V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C,72C V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
		74C,82C V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C,72C V_{CC} = 4.5V I_O = 1.6 mA			0.4	V
		74C,82C V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−4.35		−8	mA
I_{SOURCE}	Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−20		−40	mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	4.35		8	mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	20		40	mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	Any Input, (Note 2)		5.0		pF
C_{OUT}	Output Capacitance					
	MM72C19/MM82C19	(Note 2)		11.0		pF
C_{pd}	Power Dissipation Capacitance	(Note 3)		100		pF
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Inputs to Output	$V_{CC} = 5.0V$		250	600	ns
		$V_{CC} = 10V$		110	300	ns
		$V_{CC} = 5.0V$, $C_L = 150$ pF		290	650	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Data Select Inputs to Output	$V_{CC} = 5.0V$		290	650	ns
		$V_{CC} = 10V$		120	330	ns
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" from Strobe to Output					
	MM54C150/MM74C150	$V_{CC} = 5.0V$		120	300	ns
		$V_{CC} = 10V$		55	150	ns
t_{1H}, t_{0H}	Delay from Strobe to High Impedance State					
	MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$, $C_L = 5$ pF		80	200	ns
		$V_{CC} = 10V$, $R_L = 10k$, $C_L = 5$ pF		60	150	ns
t_{H1}, t_{H0}	Delay from Strobe to Logical "1" Level or to Logical "0" Level (from High Impedance State)					
	MM72C19/MM82C19	$V_{CC} = 5.0V$, $R_L = 10k$		80	250	ns
		$V_{CC} = 10V$, $R_L = 10k$		30	120	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Charactersitcs" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

truth table

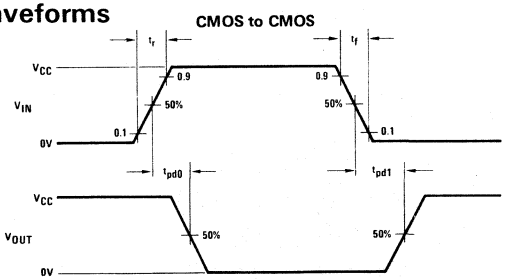
MM54C150/MM74C150

INPUTS																			OUTPUT
D	C	B	A	STROBE	E0	E1	E2	E3	E4	E5	E6	E7	E8	E9	E10	E11	E12	E13	E14	E15	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1 *
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

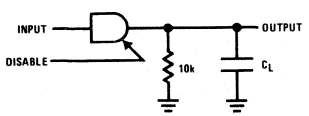
*For MM72C19/MM82C19 this would be Hi-Z, everything else is the same.

switching time waveforms

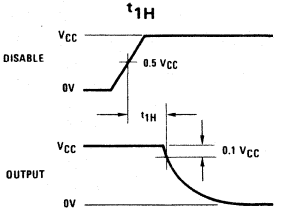
CMOS to CMOS



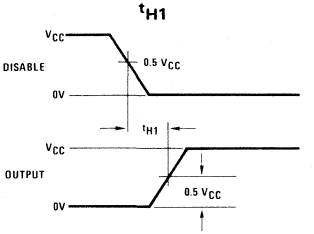
t_{1H} and t_{H1}



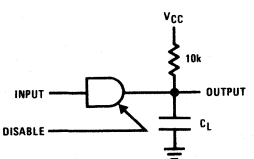
t_{1H}



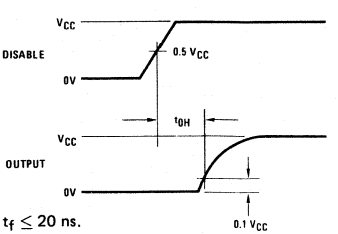
t_{H1}



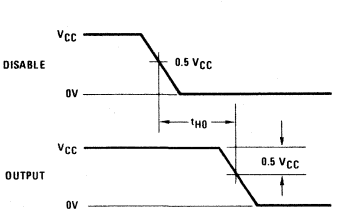
t_{0H} and t_{H0}



t_{0H}



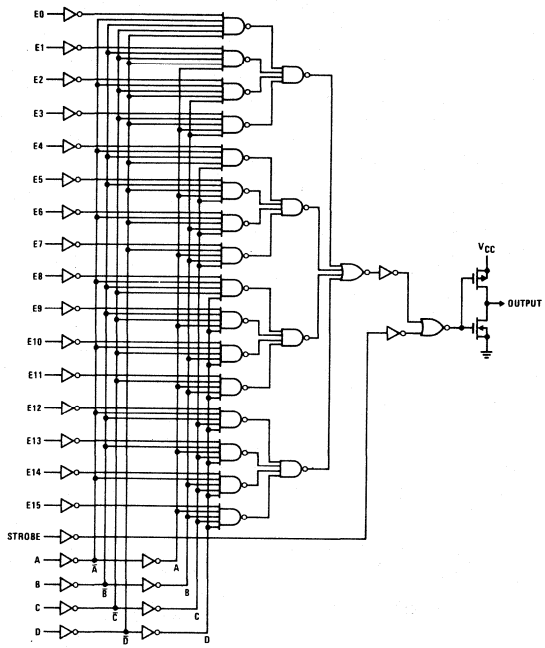
t_{H0}



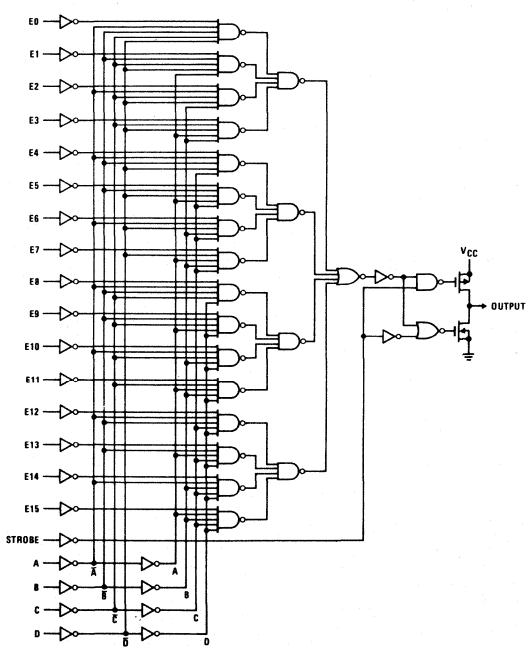
Note: Delays measured with input t_r, $t_f \leq 20$ ns.

logic diagrams

MM54C150/MM74C150



MM72C19/MM82C19



National Semiconductor

MM54C151/MM74C151 8-Channel Digital Multiplexer

general description

The MM54C151/MM74C151 multiplexer is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors.

This data selector/multiplexer contains on-chip binary decoding. Two outputs provide true (output Y) and complement (output W) data. A logical "1" on the strobe input forces W to a logical "1" and Y to a logical "0."

All inputs are protected against electrostatic effects.

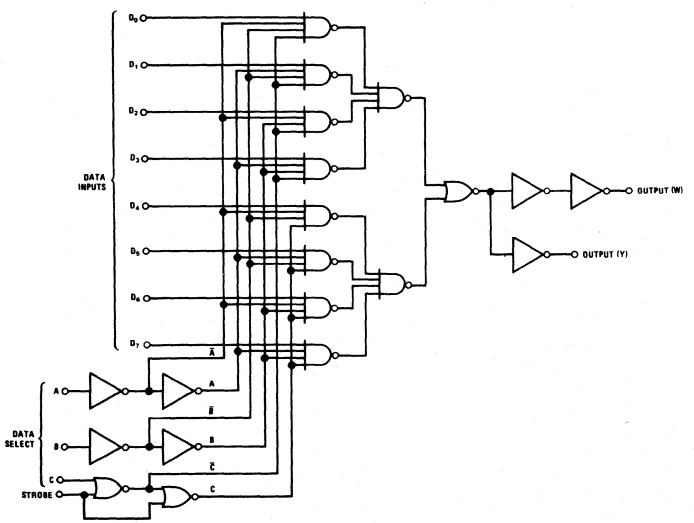
features

- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} typ
- Low power 50 nW typ

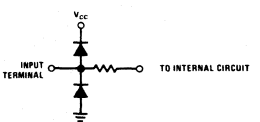
applications

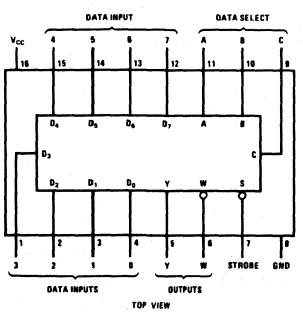
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams



Input Protection For All Inputs





absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C151	−55°C to +125°C
	MM74C151	−40°C to +85°C
Storage Temperature		−65°C to +150°C
Maximum V_{CC} Voltage		18V
Package Dissipation		500 mW
Operating V_{CC} Range		3V to 15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

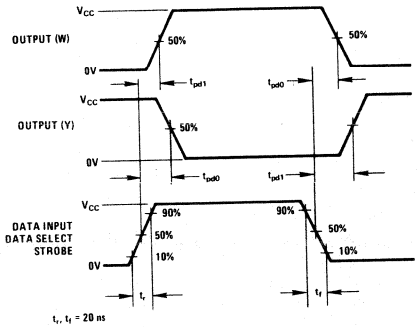
Min/Max limits apply across temperature range across otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
	V_{CC} = 10.0V, I_O = − 10 μA	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V, I_O = +10 μA			0.5	V
	V_{CC} = 10.0V, I_O = +10 μA			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V, V_{IN} = 15V			1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V, V_{IN} = 0V	-1			μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or Logical "1" from Data to Y	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	270	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	130	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Data to W	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		200	300	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	140	ns
Propagation Delay Time to a Logical "0" or Logical "1" from Strobe or Data Select to Y	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	360	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		110	170	ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360 μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	-1.75			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V	-8.0			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

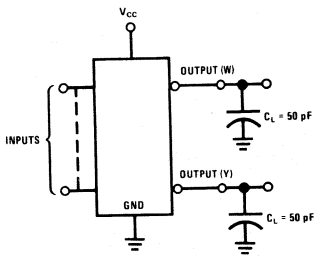
Note 1: This device should not be connected under power on conditions.

switching time waveforms

CMOS to CMOS (t_{pd1} & t_{pd0})



ac test circuit



truth table

INPUTS												OUTPUTS	
C	B	A	STROBE	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

National Semiconductor

MM54C154/MM74C154 4-Line to 16-Line Decoder/ Demultiplexer

general description

The MM54C154/MM74C154 one of sixteen decoder is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The device is provided with two strobe inputs, both of which must be in the logical "0" state for normal operation. If either strobe input is in the logical "1" state, all 16 outputs will go to the logical "1" state.

To use the product as a demultiplexer, one of the strobe inputs serves as a data input terminal, while the other strobe input must be maintained in the logical "0" state. The information will then be transmitted to the selected output as determined by the 4-line input address.

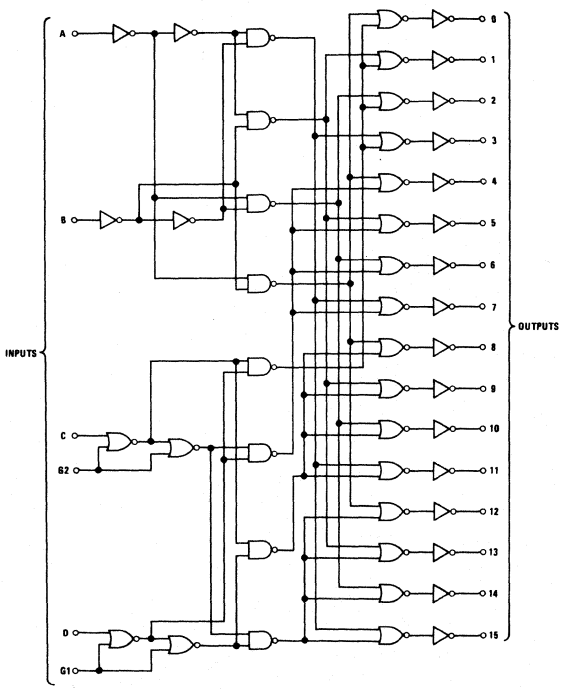
features

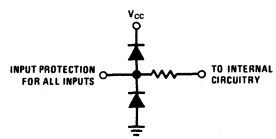
- Supply voltage range 3V to 15V
- Tenth power TTL compatible drive 2 LPTTL loads
- High noise margin 1V guaranteed
- High noise immunity 0.45 V_{CC} typ

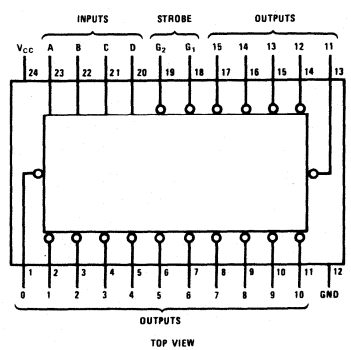
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams







absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C154	−55°C to +125°C
MM74C154	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum V_{CC} Voltage	18V
Package Dissipation	500 mW
Operating Range, V_{CC}	+3V to +15V
Lead Temperature (Soldering, 10 sec)	300°C

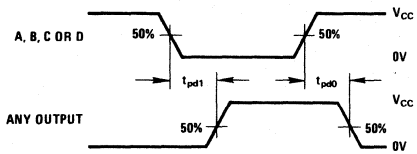
electrical characteristics

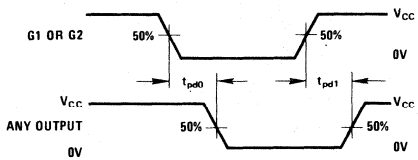
(Min/max limits apply across temperature range unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10 V			1.5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay to a Logical "0" From Any Input to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "0" From G1 or G2 to Any Output (t_{pd0})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		275 100	400 200	ns ns
Propagation Delay to a Logical "1" From Any Input to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
Propagation Delay to a Logical "1" From G1 or G2 to Any Output (t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		265 100	400 200	ns ns
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4.5 74C V_{CC} = 4.75			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4.5V, I_O = −100μA 74C V_{CC} = 4.75V, I_O = −100μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

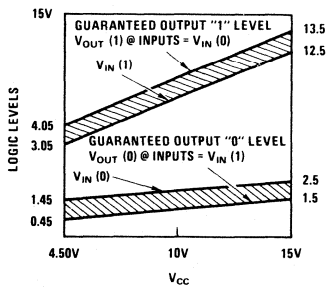
switching time waveforms





$t_r = t_f = 20$ ns

Guaranteed Noise Margin as a Function of V_{CC}



truth table

INPUTS						OUTPUTS														
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

X = "Don't Care" Condition

National Semiconductor

MM54C157/MM74C157 Quad 2-Input Multiplexers

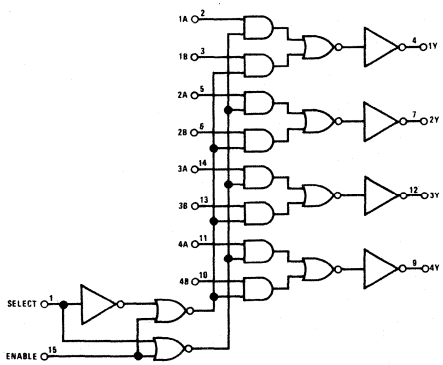
general description

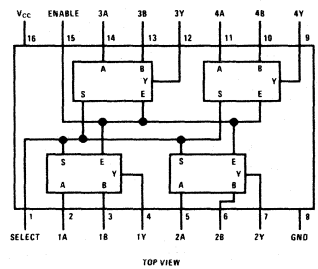
These multiplexers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement transistors. They consist of four 2-input multiplexers with a common select and enable inputs. When the enable input is at logical "0" the four outputs assume the values as selected from the inputs. When the enable input is at logical "1" the outputs assume logical "0." Select decoding is done internally resulting in a single select input only.

features

- Supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power — 50 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads

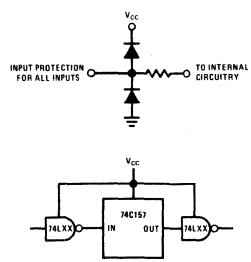
schematic and connection diagrams





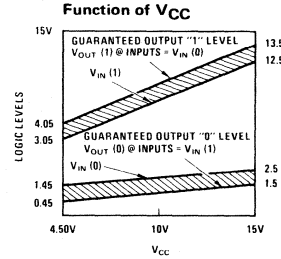
truth table

ENABLE	SELECT	A	B	OUTPUT Y
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1



74L Compatibility

Guaranteed Noise Margin as a Function of V_{CC}



absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3V to V_{CC} to 0.3V	Storage Temperature	−65°C to 150°C
Operating Temperature	MM54C157	−55°C to 125°C	Package Dissipation	500 nW
	MM74C157	−40°C to +85°C	Lead Temperature (Soldering, 10 sec)	300°C
Maximum V_{CC} Voltage		18V	Operating V_{CC} Range	+3V to 15V

electrical characteristics

Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V	−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0V		0.050	60	μA
Input Capacitance	Any Input		5		pF
Propagation Delay from Data to Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		150	250	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		70	110	ns
Propagation Delay from Select to Output (t_{pd0} or t_{pd1})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		80	130	ns
Propagation Delay from Enable to Output (t_{pd0})	V_{CC} = 5.0V C_L = 50 pF, T_A = 25°C		180	300	ns
	V_{CC} = 10.0V C_L = 50 pF, T_A = 25°C		80	130	ns
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C V_{CC} = 4.5V			0.8	V
	74C V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C V_{CC} = 4.75V, I_O = −360μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C V_{CC} = 4.5V, I_O = 360 μA			0.4	V
	74C V_{CC} = 4.75V, I_O = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V	−1.75			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V	−8.0			mA
	T_A = 25°C, V_{OUT} = 0V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

National Semiconductor

MM54C160/MM74C160 Decade Counter with Asynchronous Clear
MM54C161/MM74C161 Binary Counter with Asynchronous Clear
MM54C162/MM74C162 Decade Counter with Synchronous Clear
MM54C163/MM74C163 Binary Counter with Synchronous Clear

general description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P channel enhancement mode transistors. They feature an internal carry lookahead for fast counting schemes and for cascading packages without additional gating.

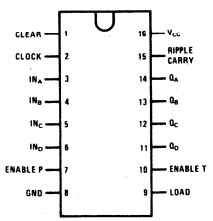
A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the C162 and C163 is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the C160 and C161 is asynchronous and a low level at the clear input sets all four outputs low regardless of the state of the clock.

Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

features

- High noise margin — 1V guaranteed
- High noise immunity — 0.45 V_{CC} typ
- Tenth power TTL compatible — drives 2 LPTTL loads
- Wide supply voltage range — 3V to 15V
- Internal look-ahead for fast counting scemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable

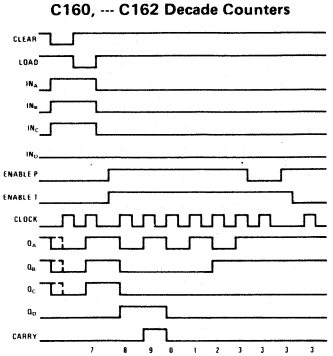
connection diagram



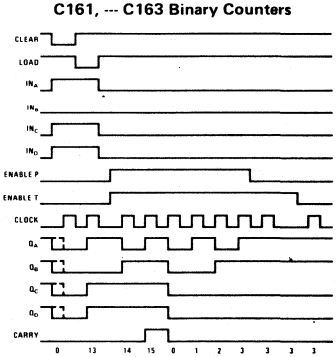
TOP VIEW

logic waveforms

C160, --- C162 Decade Counters



C161, --- C163 Binary Counters



absolute maximum ratings

Voltage At Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	18V
Operating Temperature MM54C160/1/2/3	−55°C to +125°C	Package Dissipation	500mW
MM74C160/1/2/3	−40°C to +85°C	Operating V_{CC} Range	+3V to +15V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 sec.)	300°C

electrical characteristics

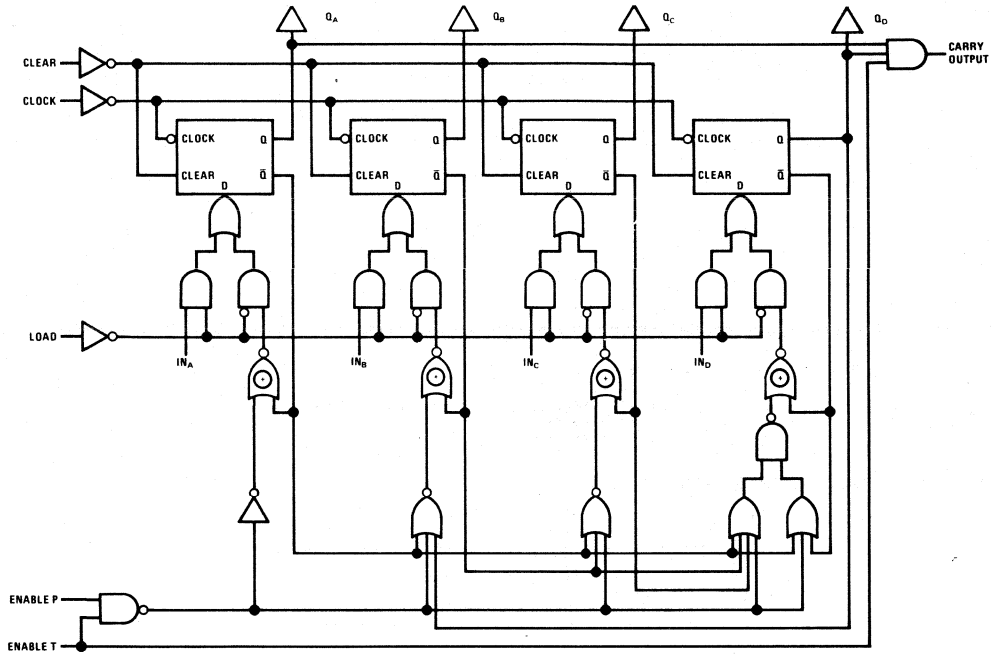
Min/Max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS to CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time from Clock to Q t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		250	400	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		100	160	ns
Propagation Delay Time from Clock to Carry Out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		290	450	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		120	190	ns
Propagation Delay Time from T Enable to Carry Out t_{pd0} or t_{pd1}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		180	290	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		70	120	ns
Propagation Time from Clear to Q t_{pd0} (C160 and C161 only)	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		190	300	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		80	150	ns
Time Prior to Clock that Data or Load Must be Present t_{SETUP}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		120		ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		30		ns
Time Prior to Clock that Enable P or T Must be Present t_{SETUP}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		170	280	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		70	120	ns
Time Prior to Clock that Clear Must be Present t_{SETUP} (162, 163 only)	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		120	190	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		50	80	ns
Minimum Clock Pulses Width t_{WL} or t_{WH}	V_{CC} = 5V, C_L = 50pF, T_A = 25°C		90	170	ns
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C		35	70	ns
Maximum Clock Rise or Fall Time	V_{CC} = 5V, C_L = 50pF, T_A = 25°C			15	μs
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C			5.0	μs
Maximum Clock Frequency	V_{CC} = 5V, C_L = 50pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10V, C_L = 50pF, T_A = 25°C	5.5	8.5		MHz
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage 54C	V_{CC} = 4.5V	V_{CC}−1.5			V
74C	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage 54C	V_{CC} = 4.5V			0.8	V
74C	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage 54C	V_{CC} = 4.5V, I_O = −360μA	2.4			V
74C	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage 54C	V_{CC} = 4.5V, I_O = +360μA			0.4	V
74C	V_{CC} = 4.75V, I_O = +360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current I_{SOURCE}	V_{CC} = 5V, $V_{IN(0)}$ = 0V, V_{OUT} = 0V, T_A = 25°C	1.75			mA
Output Source Current I_{SOURCE}	V_{CC} = 10V, $V_{IN(0)}$ = 0V, V_{OUT} = 0V, T_A = 25°C	8.0			mA
Output Sink Current I_{SINK}	V_{CC} = 5V, $V_{IN(1)}$ = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75			mA
Output Sink Current I_{SINK}	V_{CC} = 10V, $V_{IN(1)}$ = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0			mA

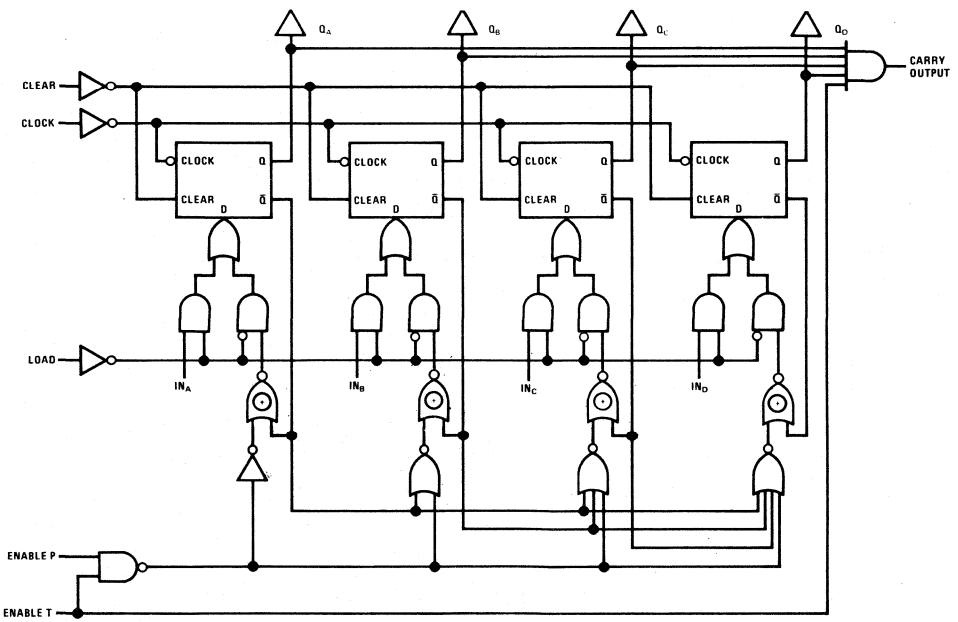
Note 1: This device should not be connected during power on conditions.

logic diagrams

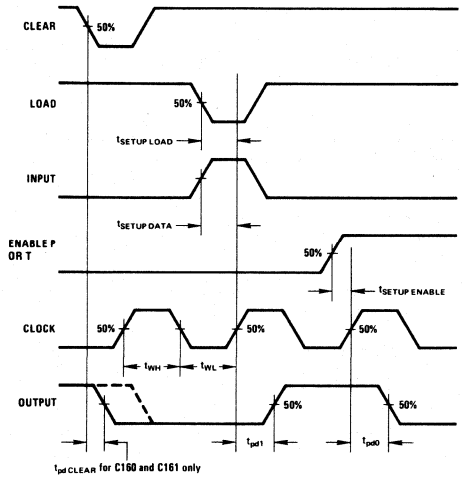
MM74C160, MM74C162; Clear is Synchronous for the MM74C162



MM74C161, MM74C163; Clear is Synchronous for the MM74C163



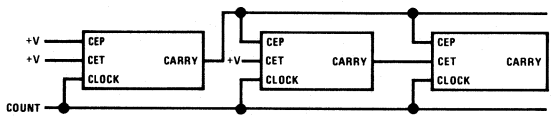
switching time waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f =$ 20 ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

cascading packages



National Semiconductor

MM54C164/MM74C164 8-Bit Parallel-Out Serial Shift Register

general description

The MM54C164/MM74C164 shift registers are a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. These 8-bit shift registers have gated serial inputs and clear. Each register bit is a D-type master/slave flip flop. A high-level input enables the other input which will then determine the state of the flip flop.

Data is serially shifted in and out of the 8-bit register during the positive going transition of clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input. All inputs are protected against electrostatic effects.

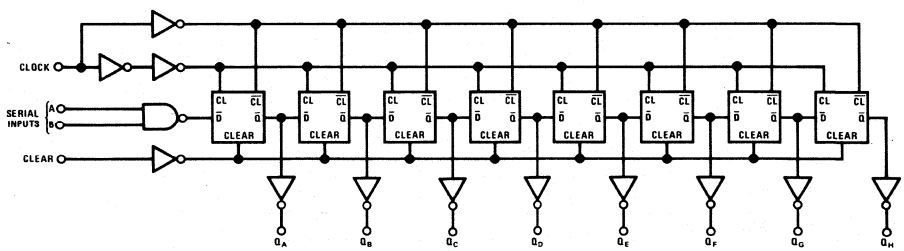
features

■ Supply voltage range	3V to 15V
■ Tenth power TTL compatible	drive 2 LPTTL loads
■ High noise immunity	0.45 V_{CC} typ
■ Low power	50 nW typ
■ Medium speed operation	8.0 MHz typ with 10V supply

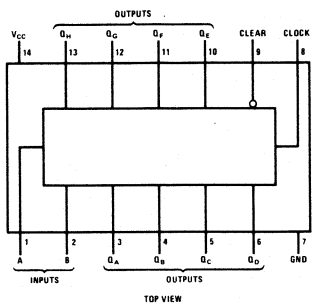
applications

- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

block diagram



connection diagram



truth table

Serial Inputs A and B

INPUTS t_n		OUTPUT t_{n+1}
A	B	Q_A
1	1	1
0	1	0
1	0	0
0	0	0

absolute maximum ratings

Voltage at Any Pin (Note 1)	−0.3 V to V_{CC} + 0.3 V	Maximum V_{CC} Voltage	18 V
Operating Temperature MM54C164	−55°C to +125°C	Package Dissipation	500 mW
MM74C164	−40°C to +85°C	Operating V_{CC} Range	+3 V to +15 V
Storage Temperature	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

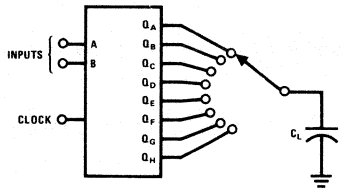
electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

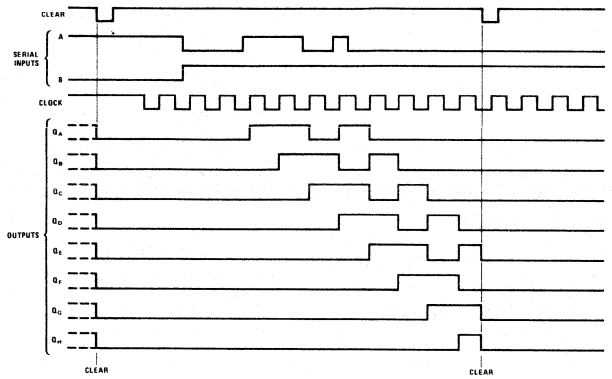
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0 V	3.5			V
	V_{CC} = 10.0 V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0 V			1.5	V
	V_{CC} = 10.0 V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0 V, I_O = −10 μA	4.5			V
	V_{CC} = 10.0 V, I_O = −10 μA	9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0 V, I_O = −10 μA			0.5	V
	V_{CC} = 10.0 V, I_O = −10 μA			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0 V, V_{IN} = 15 V		0.005	1	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0 V, V_{IN} = 0 V	−1	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0 V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" or a Logical "1" from Clock to Q	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C		230	310	ns
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C		90	120	ns
Propagation Delay Time to a Logical "0" from Clear to Q	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C		280	380	ns
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C	200	110	150	ns
Time Prior to Clock Pulse that Data Must be Present t_{SETUP}	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	80	110		ns
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C		30		ns
Time After Clock Pulse that Data Must be Held	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	0	0		ns
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C	0	0		ns
Maximum Clock Frequency	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	2	3		MHz
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C	5.5	8		MHz
Minimum Clear Pulse Width	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C		150	250	ns
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C		55	90	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0 V, C_L = 50 pF, T_A = 25°C	15			μs
	V_{CC} = 10.0 V, C_L = 50 pF, T_A = 25°C	5			μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C: V_{CC} = 4.5 V	V_{CC} − 1.5			V
	74C: V_{CC} = 4.75 V				
Logical "0" Input Voltage $V_{IN(0)}$	54C: V_{CC} = 4.5 V			0.8	V
	74C: V_{CC} = 4.75 V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C: V_{CC} = 4.5 V, I_O = −360 μA	2.4			V
	74C: V_{CC} = 4.75 V, I_O = −360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C: V_{CC} = 4.5 V, I_O = 360 μA			0.4	V
	74C: V_{CC} = 4.75 V, I_O = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0 V, $V_{IN(0)}$ = 0 V	−1.75			mA
	T_A = 25°C, V_{OUT} = 0 V				
Output Source Current (I_{SOURCE})	V_{CC} = 10 V, $V_{IN(0)}$ = 0 V	−8.0			mA
	T_A = 25°C, V_{OUT} = 0 V				
Output Sink Current (I_{SINK})	V_{CC} = 5.0 V, $V_{IN(1)}$ = 5.0 V	1.75			mA
	T_A = 25°C, V_{OUT} = V_{CC}				
Output Sink Current (I_{SINK})	V_{CC} = 10 V, $V_{IN(1)}$ = 10 V	8.0			mA
	T_A = 25°C, V_{OUT} = V_{CC}				

Note 1: These devices should not be connected under power on conditions.

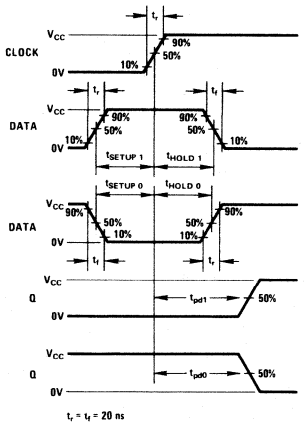
ac test circuit



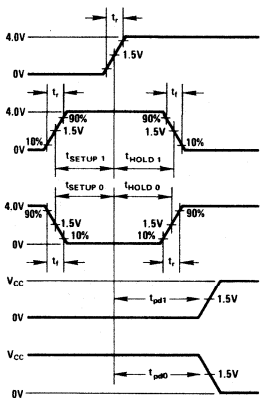
switching time waveforms



CMOS to CMOS

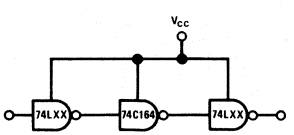


TTL to CMOS

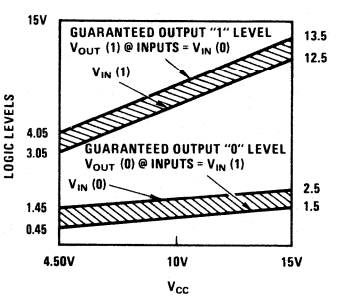


typical applications

74C Compatibility



Guaranteed Noise Margin as a Function of V_{CC}



National Semiconductor

MM54C165/MM74C165 Parallel-Load 8-Bit Shift Register

general description

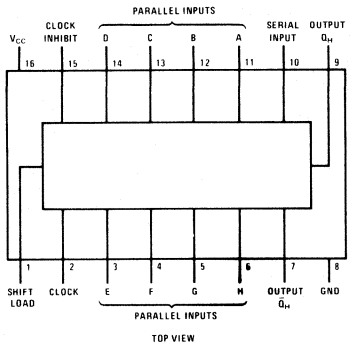
The MM54C165/MM74C165 is an 8-bit serial shift register which shifts data from Q_A to Q_H when clocked. Parallel inputs to each stage are enabled by a low level at the shift/load input. Also included is a gated clock input and a complementary output from the eighth-bit.

Clocking is accomplished through a 2-input NOR-gate permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the shift/load input high enables the other clock input. Data transfer occurs on the positive edge of the clock. The clock inhibit input should be changed to a high level only while the clock input is high. Parallel loading is inhibited as long as the shift/load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

features

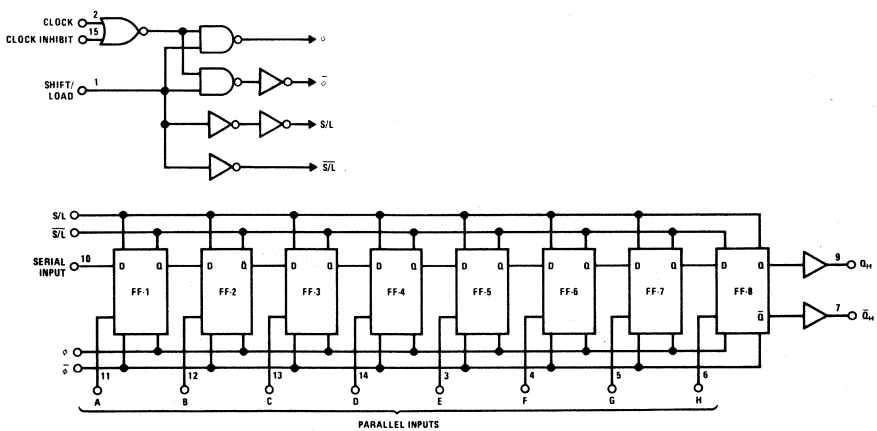
- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Direct overriding load
- Gated clock inputs
- Fully static operation

connection diagram



TOP VIEW

block diagram



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C165	−55°C to +125°C
MM74C165	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V V_{CC} = 10V	3.5 8.0			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V V_{CC} = 10V			1.5 2.0	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9.0			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1.0	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5 V_{CC}−1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

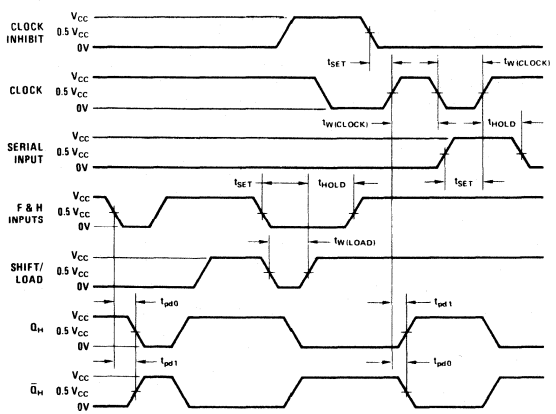
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from Clock or Load to Q or $\overline{Q}$	V_{CC} = 5.0V		200	400	ns
	V_{CC} = 10V		80	200	ns
Propagation Delay Time to a Logical "0" (t_{pd0}), or Logical "1" (t_{pd1}), from H to Q or $\overline{Q}$	V_{CC} = 5.0V		200	400	ns
	V_{CC} = 10V		80	200	ns
Clock Inhibit Set-up Time	V_{CC} = 5.0V	150	75		ns
	V_{CC} = 10V	60	30		ns
Serial Input Set-up Time	V_{CC} = 5.0V	50	25		ns
	V_{CC} = 10V	30	15		ns
Serial Input Hold Time	V_{CC} = 5.0V	50	0		ns
	V_{CC} = 10V	30	0		ns
Parallel Input Set-up Time	V_{CC} = 5.0V	150	75		ns
	V_{CC} = 10V	60	30		ns
Parallel Input Hold Time	V_{CC} = 5.0V	50	0		ns
	V_{CC} = 10V	30	0		ns
Minimum Clock Pulse Width	V_{CC} = 5.0V		70	200	ns
	V_{CC} = 10V		30	100	ns
Minimum Load Pulse Width	V_{CC} = 5.0V		85	180	ns
	V_{CC} = 10V		30	90	ns
Maximum Clock Frequency	V_{CC} = 5.0V		6.0	2.5	MHz
	V_{CC} = 10V		12	5.0	MHz
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	10			μs
	V_{CC} = 10V	5.0			μs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF
Power Dissipation Capacitance (C_{pd})	(Note 3)		65		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms



Note A: The remaining six data and the serial input are low.

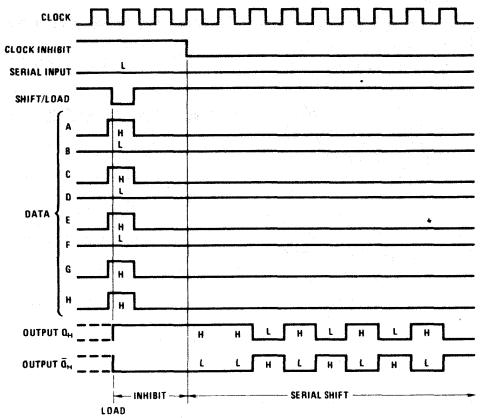
Note B: Prior to test, high level data is loaded into H input.

truth table

INPUTS					INTERNAL OUTPUTS		OUTPUT Q_H
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	
L	X	X	X	a . . . h	a	b	h
H	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = $V_{IN(1)}$, L = $V_{IN(0)}$
X = irrelevant
↑ = transition from $V_{IN(0)}$ to $V_{IN(1)}$
a . . . h = the level at data inputs A thru H
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B or Q_H, before the indicated input conditions were established
Q_{An}, Q_{6n} = the level of Q_A or Q_6 before the most recent ↑ transition of the clock

logic waveforms



National Semiconductor

MM54C173/MM74C173 TRI-STATE® Quad D Flip-Flop

general description

The MM54C173/MM74C173 TRI-STATE quad D flip flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The four D type flip flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disable allows the flip flop to remain in their present states without disrupting the clock. If either of the two input disables are taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip flops do not change state.

Clearing is enabled by taking the input to a logic "1" level. Clocking occurs on the positive going transition.

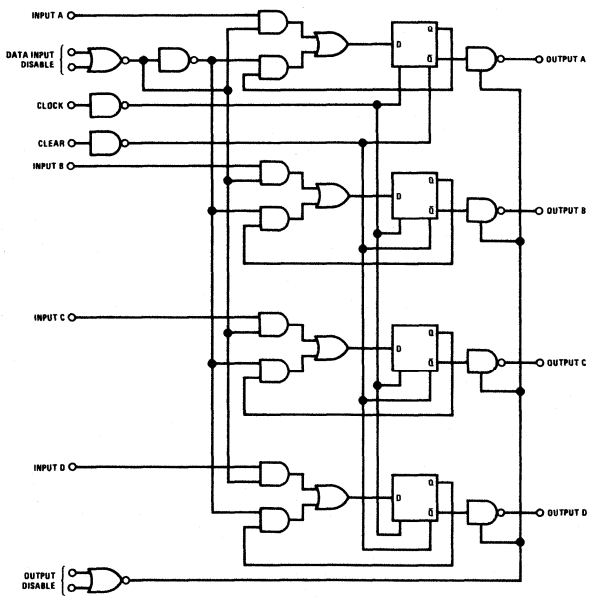
features

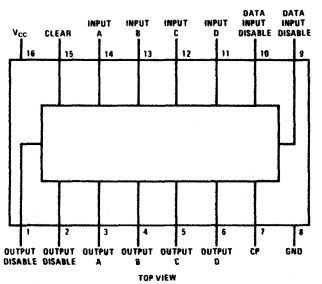
- Supply voltage range 3V to 15V
- Tenth power TTL compatible Drive 2 LPTTL loads
- High noise immunity 0.45 V_{CC} typ
- Low power
- Medium speed operation
- High impedance TRI-STATE
- Input disabled without gating the clock

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering
- Computers

logic and connection diagrams





absolute maximum ratings

Voltage at Any Pin (Note 1)		−0.3 to V_{CC} +0.3V
Operating Temperature	MM54C173	−55°C to +125°C
	MM74C173	−40°C to +85°C
Storage Temperature		−65°C to +150°C
Maximum V_{CC} Voltage		18V
Package Dissipation		500 mW
Operating V_{CC} Range		+3V to +15V
Lead Temperature (Soldering, 10 sec)		300°C

electrical characteristics

Min/max limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10.0V	8			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10.0V			2	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V	4.5			V
	V_{CC} = 10.0V	9			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V			0.5	V
	V_{CC} = 10.0V			1	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V		0.005	1	μA
Logical "0" Input Current $I_{IN(0)}$		−1	−0.005		μA
Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.001		μA
	V_{CC} = 15V, V_O = 0V		0.001		μA
Supply Current I_{CC}	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) From Clock to Output	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		220	400	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		80	200	ns
Input Data Setup Time, $t_{S\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		40	80	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		15	30	ns
Input Data Hold Time, $t_{H\ DATA}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0	0	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0	0	ns
Input Disable Setup Time, $t_{S\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		35	70	ns
Input Disable Hold Time, $t_{H\ DISS}$	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		0	0	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		0	0	ns
Delay From Output Disable to High Impedance State (From Logical "1" or Logical "0" Level), t_{1H}, t_{0H}	V_{CC} = 5.0V, C_L = 5 pF, T_A = 25°C, R_L = 10k		170	340	ns
	V_{CC} = 10.0V, C_L = 5 pF, T_A = 25°C, R_L = 10k		70	140	ns
Delay From Output Disable to Logical "1" Level, t_{H1} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Delay From Output Disable to Logical "0" Level, t_{HO} (From High Impedance State)	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		170	340	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70	140	ns
Propagation Delay From Clear to Output t_{pdR}	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		240	490	ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		90	180	
Maximum Clock Frequency	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C	3.0	4.0		MHz
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C	7	12		
Minimum Clear Pulse Width	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		150		ns
	V_{CC} = 10.0V, C_L = 50 pF, T_A = 25°C		70		
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V, C_L = 50 pF	10			μs
	V_{CC} = 10.0V, C_L = 50 pF	5			μs

Note 1: These devices should not be connected under "Power On" conditions.

electrical characteristics (con't)

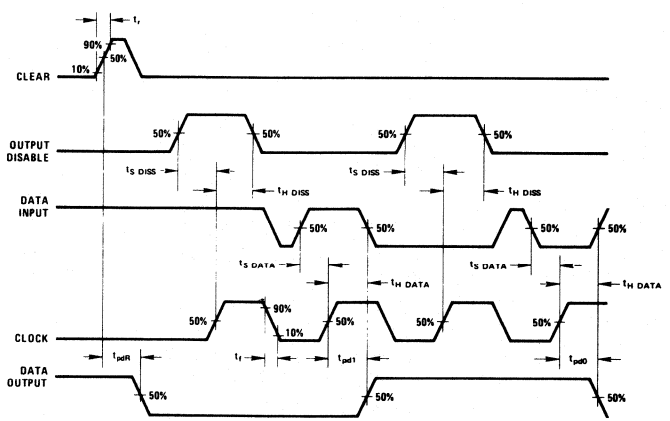
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOW POWER TTL/CMOS INTERFACE					
Logical "1" Input Voltage $V_{IN(1)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage $V_{IN(0)}$	54C, V_{CC} = 4.5V 74C, V_{CC} = 4.75V			.8	V
Logical "1" Output Voltage $V_{OUT(1)}$	54C, V_{CC} = 4.5V, I_O = −360μA 74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage $V_{OUT(0)}$	54C, V_{CC} = 4.5V, I_O = 360μA 74C, V_{CC} = 4.75V, I_O = 360μA			.4	V
Propagation Delay Time to a Logical "0", t_{pd0} or Logical "1" t_{pd1} From Clock	V_{CC} = 5.0V, C_L = 50 pF, T_A = 25°C		500		ns
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	-1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	-8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

truth table

Truth Table (Both Output Disables Low)

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

switching time waveforms



National Semiconductor

MM54C174/MM74C174 Hex D Flip-Flop

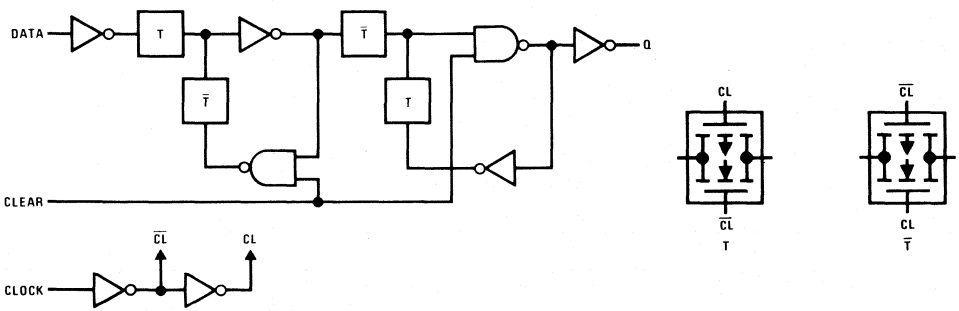
general description

The MM54C174/MM74C174 hex D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N- and P-channel enhancement transistors. All have a direct clear input. Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clear is independent of clock and accomplished by a low level at the clear input. All inputs are protected by diodes to V_{CC} and GND.

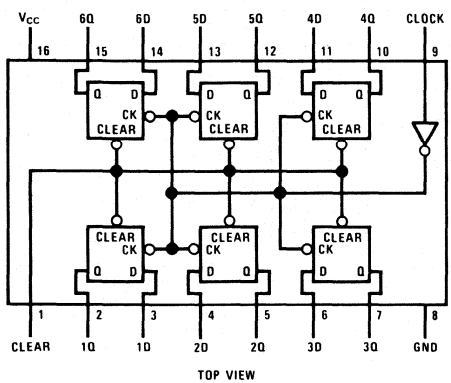
features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

logic diagram



connection diagram



TOP VIEW

truth table

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C174	−55°C to +125°C
MM74C174	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q	V_{CC} = 5.0V		150	300	ns
	V_{CC} = 10V		70	110	ns
Propagation Delay Time to a Logical "0" from Clear	V_{CC} = 5.0V		110	300	ns
	V_{CC} = 10V		50	110	ns
Time Prior to Clock Pulse that Data Must be Present (t_{SETUP})	V_{CC} = 5.0V	75			ns
	V_{CC} = 10V	25			ns
Time After Clock Pulse that Data Must be Held (t_{HOLD})	V_{CC} = 5.0V	75	-10	0	ns
	V_{CC} = 10V	25	-5	0	ns
Minimum Clock Pulse Width	V_{CC} = 5.0V		50	250	ns
	V_{CC} = 10V		35	100	ns
Minimum Clear Pulse Width	V_{CC} = 5.0V		65	140	ns
	V_{CC} = 10V		35	70	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	15	>1200		μs
	V_{CC} = 10V	5.0	>1200		μs
Maximum Clock Frequency	V_{CC} = 5.0V	2.0	6.5		MHz
	V_{CC} = 10V	5.0	12		MHz
Input Capacitance (C_{IN})	Clear Input (Note 2)		11		pF
	Any Other Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		95		pF

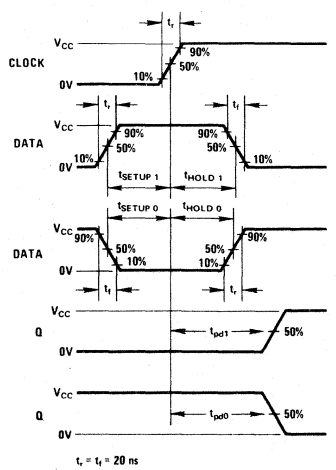
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

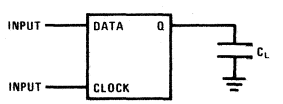
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

CMOS to CMOS



ac test circuit



National Semiconductor

MM54C175/MM74C175 Quad D Flip-Flop

general description

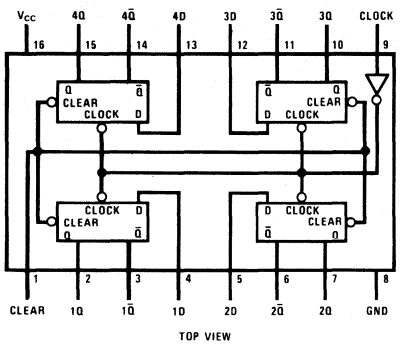
The MM54C175/MM74C175 consists of four positive-edge-triggered D-type flip-flops implemented with monolithic CMOS technology. Both true and complemented outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all four Q outputs to logical "0" and $\overline{Q}$'s to logical "1."

All inputs are protected from static discharge by diode clamps to V_{CC} and GND.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power	fan out of 2
TTL compatibility	driving 74L

connection diagram and truth table



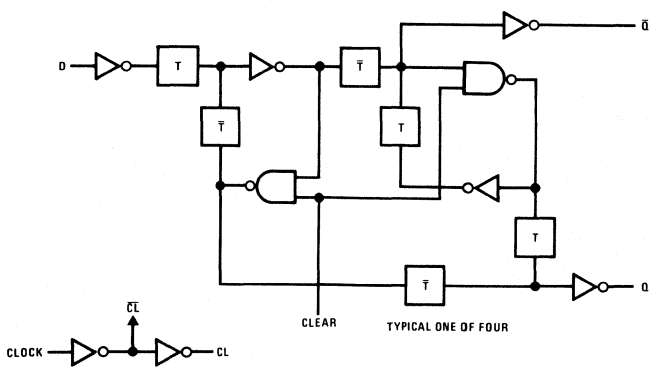
TOP VIEW

Each Flip-Flop

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change

logic diagrams



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C175	−55°C to +125°C
MM74C175	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C175	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C175	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C175	V_{CC} = 4.5V			0.8	V
MM74C175	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C175	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C175	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C175	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C175	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC} T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to a Logical "0" (t_{pd0}) or Logical "1" (t_{pd1}) from Clock to Q or $\overline{Q}$	V_{CC} = 5.0V		190	300	ns
	V_{CC} = 10V		75	110	ns
Propagation Delay Time to a Logical "0" from Clear to Q	V_{CC} = 5.0V		180	300	ns
	V_{CC} = 10V		70	110	ns
Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$	V_{CC} = 5.0V		230	400	ns
	V_{CC} = 10V		90	150	ns
Time Prior to Clock Pulse that Data must be Present (t_{SET-UP})	V_{CC} = 5.0V	100	45		ns
	V_{CC} = 10V	40	16		ns
Time after Clock Pulse that Data must be Held (t_{HOLD})	V_{CC} = 5.0V		−11	0	ns
	V_{CC} = 10V		−4	0	ns
Minimum Clock Pulse Width	V_{CC} = 5.0V		130	250	ns
	V_{CC} = 10V		45	100	ns
Minimum Clear Pulse Width	V_{CC} = 5.0V		120	250	ns
	V_{CC} = 10V		45	100	ns
Maximum Clock Rise Time	V_{CC} = 5.0V	15	450		μs
	V_{CC} = 10V	5.0	125		μs
Maximum Clock Fall Time	V_{CC} = 5.0V	15	50		μs
	V_{CC} = 10V	5.0	50		μs
Maximum Clock Frequency	V_{CC} = 5.0V	2.0	3.5		MHz
	V_{CC} = 10V	5.0	10		MHz
Input Capacitance (C_{IN})	Clear Input (Note 2)		10		pF
	Other Input		5.0		pF
Power Dissipation Capacitance (C_{pd})	Per Package (Note 3)		130		pF

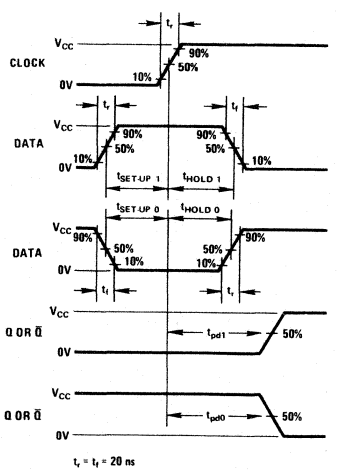
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

CMOS to CMOS



National Semiconductor

MM54C192/MM74C192 Synchronous 4-Bit Up/Down Decade Counter
MM54C193/MM74C193 Synchronous 4-Bit Up/Down Binary Counter

general description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The MM54C192 and MM74C192 are BCD counters. While the MM54C193 and MM74C193 are binary counters.

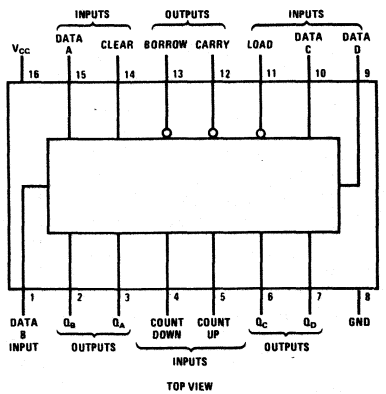
Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive going transition of this clock.

These counters feature preset inputs that are set when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1." The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

features

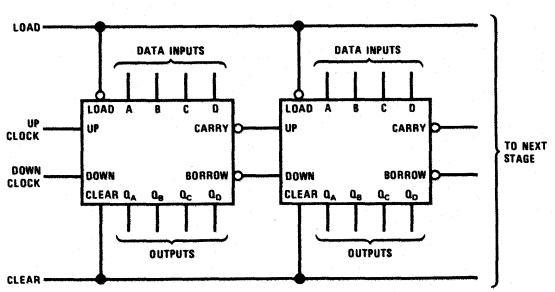
- High noise margin — 1V guaranteed
- Tenth power TTL compatible — drive 2 LPTTL loads
- Wide supply range — 3V to 15V
- Carry and borrow outputs for N-bit cascading
- Asynchronous clear
- High noise immunity — 0.45 V_{CC} typ

connection diagram

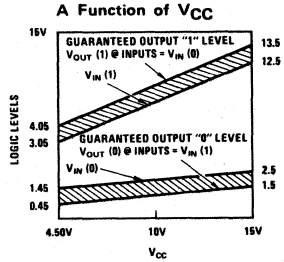


TOP VIEW

cascading packages



Guaranteed Noise Margin as A Function of V_{CC}



absolute maximum ratings

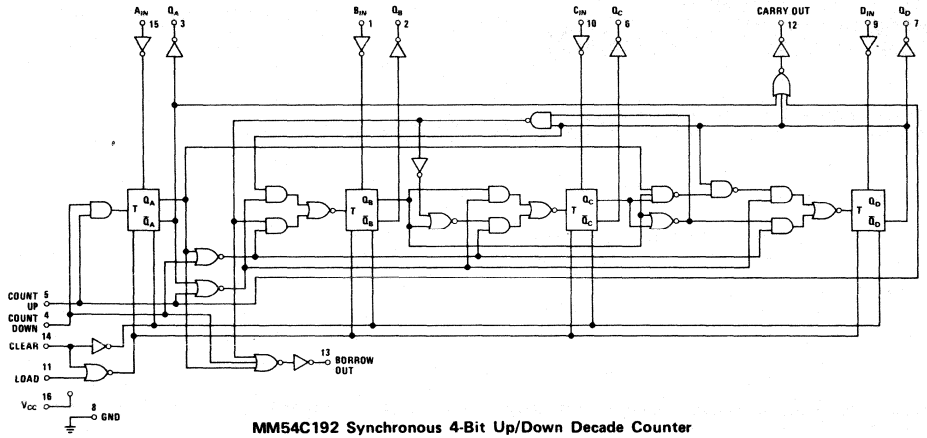
Voltage at Any Pin (Note 1)	−0.3V to V_{CC} + 0.3V	Maximum V_{CC} Voltage	18V
Operating Temperature Range		Package Dissipation	500 mW
MM54C192, MM54C193	−55°C to +125°C	Operating V_{CC} Range	+3V to +15V
MM74C192, MM74C193	−40°C to +85°C	Lead Temperature (Soldering, 10 sec)	300°C
Storage Temperature Range	−65°C to +150°C		

electrical characteristics (Min/max limits apply across temperature range unless otherwise specified.)

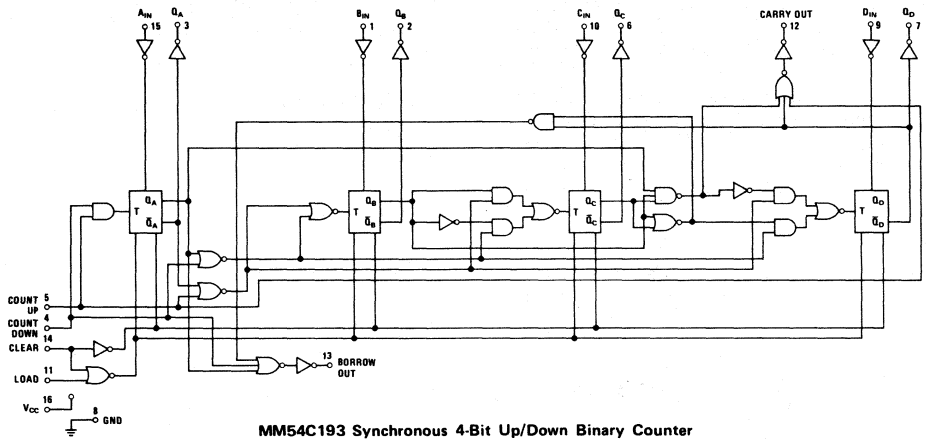
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO MOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA V_{CC} = 10V, I_O = −10μA	4.5 9			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA V_{CC} = 10V, I_O = +10μA			0.5 1	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	1.0	0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
Input Capacitance	Any Input		5		pF
Propagation Delay Time to Q From Count Up or Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		250 100	400 160	ns ns
Propagation Delay Time to Borrow From Count Down (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 50	200 80	ns ns
Propagation Delay Time to Carry From Count Up (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 50	200 80	ns ns
Time Prior to Load That Data Must be Present (t_{SETUP})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100 30	160 50	ns ns
Minimum Clear Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		300 120	480 190	ns ns
Minimum Load Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		100 40	160 65	ns ns
Propagation Delay Time to Q From Load (t_{pd0} or t_{pd1})	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		300 120	480 190	ns ns
Minimum Count Pulse Width	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C		120 35	200 80	ns ns
Maximum Count Frequency	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C	2.5 6	4 10		MHz MHz
Count Rise and Fall Time	V_{CC} = 5V, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, C_L = 50 pF, T_A = 25°C			15 5	μs μs
CMOS TO TENTH POWER INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V	V_{CC}−1.5 V_{CC}−1.5			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C V_{CC} = 4.5V 74C V_{CC} = 4.75V			0.8 0.8	V V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C V_{CC} = 4.5V, I_O = −360μA 74C V_{CC} = 4.75V, I_O = −360μA	2.4 2.4			V V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C V_{CC} = 4.5V, I_O = 360μA 74C V_{CC} = 4.75V, I_O = 360μA			0.4 0.4	V V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V T_A = 25°C, V_{OUT} = 0V	−8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = V_{CC}	1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = V_{CC}	8.0			mA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

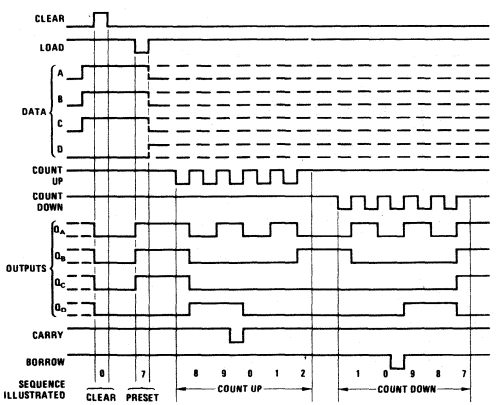
schematic diagrams



MM54C192 Synchronous 4-Bit Up/Down Decade Counter

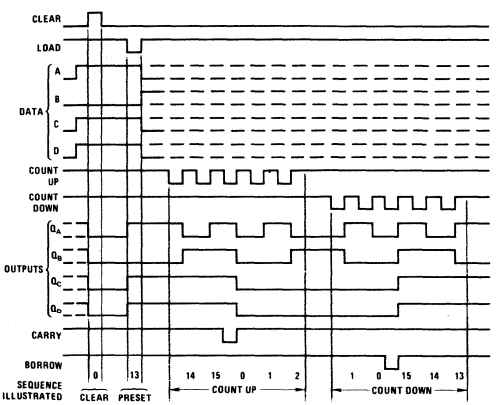


MM54C193 Synchronous 4-Bit Up/Down Binary Counter



Note 1: Clear outputs to zero.
Note 2: Load (preset) to BCD seven.
Note 3: Count up to eight, nine, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, nine, eight, and seven.

MM54C192/MM74C192



Note 1: Clear outputs to zero.
Note 2: Load (preset) to binary thirteen.
Note 3: Count up to fourteen, fifteen, carry, zero, one, and two.
Note 4: Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

MM54C193/MM74C193

NOTE A: CLEAR OVERRIDES LOAD, DATA, AND COUNT INPUTS.

NOTE B: WHEN COUNTING UP, COUNT DOWN INPUT MUST BE HIGH; WHEN COUNTING DOWN, COUNT-UP INPUT MUST BE HIGH.

National Semiconductor

MM54C195/MM74C195 4-Bit Registers

general description

The MM54C195/MM74C195 CMOS 4-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input and a direct overriding clear. The following two modes of operation are possible.

Parallel Load
Shift in direction Q_A towards Q_D

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited.

Serial shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$, D or T-type flip flop as shown in the truth table.

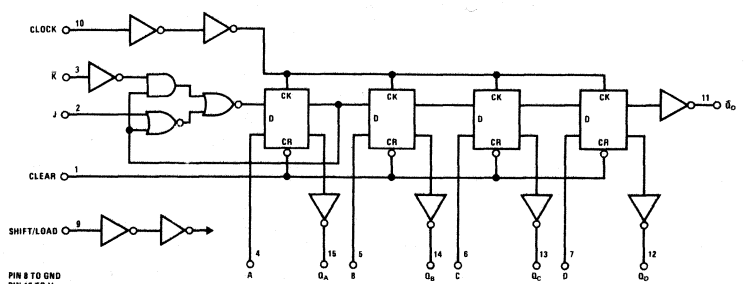
features

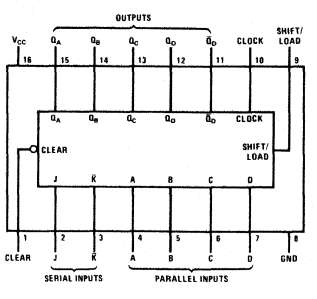
- Medium speed operation — 8.5 MHz (typ) with 10V supply and 50 pF load
- High noise immunity — 0.45 V_{CC} (typ)
- Low power — 100 nW (typ)
- Tenth power TTL compatible — drive 2 LPTTL loads
- Supply voltage range — 3V to 15V
- Synchronous parallel load
- Parallel inputs and outputs from each flip-flop
- Direct overriding clear
- J and $\overline{K}$ inputs to first stage
- Complementary outputs from last stage
- Positive edge triggered clocking
- Diode clamped inputs to protect against static charge

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Remote metering
- Industrial electronics
- Computers

schematic and connection diagrams





absolute maximum ratings

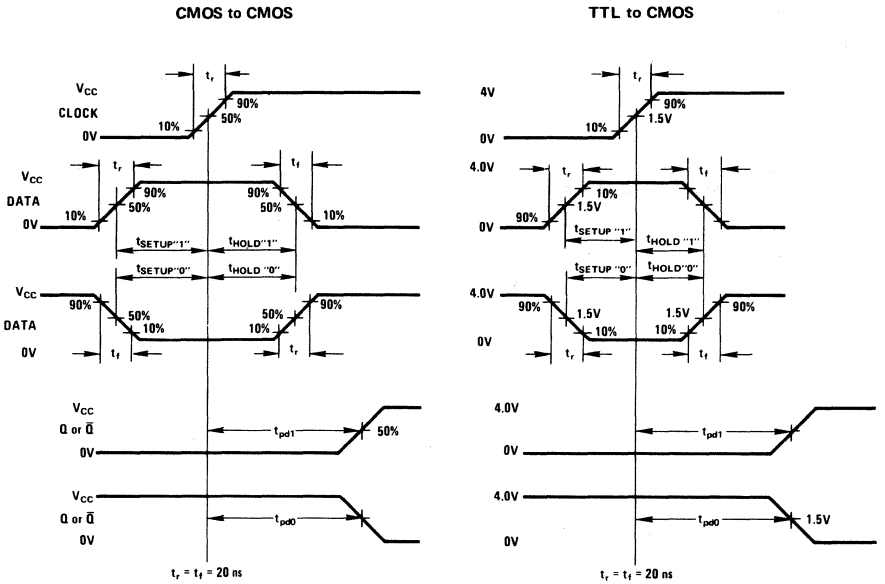
Voltage at Any Pin (Note 1)		−0.3V to V_{CC} +0.3V
Operating Temperature	MM54C195	−55°C to +125°C
	MM74C195	−40°C to +85°C
Storage Temperature		−65°C to 150°C
Maximum V_{CC} Voltage		18V
Package Dissipation		500 mW
Lead Temperature (Soldering, 10 sec)		300°C
Operating V_{CC} Range		+3V to +15V

electrical characteristics Max/Min limits apply across temperature range unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMOS TO CMOS						
Logical "1" Input Voltage $V_{IN(1)}$	V_{CC} = 5.0V		3.5			V
	V_{CC} = 10.0V		8.0			V
Logical "0" Input Voltage $V_{IN(0)}$	V_{CC} = 5.0V				1.5	V
	V_{CC} = 10.0V				2.0	V
Logical "1" Output Voltage $V_{OUT(1)}$	V_{CC} = 5.0V		4.5			V
	V_{CC} = 10.0V		9.0			V
Logical "0" Output Voltage $V_{OUT(0)}$	V_{CC} = 5.0V				0.5	V
	V_{CC} = 10.0V				1.0	V
Logical "1" Input Current $I_{IN(1)}$	V_{CC} = 15.0V			0.005	1.0	μA
Logical "0" Input Current $I_{IN(0)}$	V_{CC} = 15.0V		−1.0	−0.005		μA
Supply Current I_{CC}	V_{CC} = 15.0V			0.050	300	μA
Input Capacitance	Any Input			5.0		pF
Propagation Delay Time to a Logical "0" t_{pd0} or Logical "1" t_{pd1} from Clock to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		150	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		75	130	ns
Propagation Delay Time to a Logical "0" or Logical "1" From Clear to Q or $\overline{Q}$	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		150	300	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	130	ns
Time Prior to Clock Pulse That Data Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		80	200	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		35	70	ns
Time Prior to Clock Pulse That Shift/Load Must be Present t_{SETUP}	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		110	150	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		60	90	ns
Time After Clock Pulse That Data Must be Held	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		−10	0	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		−5	0	ns
Minimum Clock Pulse Width (t_{WL} = t_{WH})	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		100	200	ns
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C		50	100	ns
Minimum Clear Pulse Width	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C		90	130	ns
	V_{CC} = 10V	C_L = 50 pF, T_A = 25°C		40	60	ns
Maximum Clock Rise and Fall Time	V_{CC} = 5.0V	C_L = 50 pF	5.0			μs
	V_{CC} = 10.0V	C_L = 50 pF	2.0			μs
Maximum Input Clock Frequency	V_{CC} = 5.0V	C_L = 50 pF, T_A = 25°C	2.0	3.0		MHz
	V_{CC} = 10.0V	C_L = 50 pF, T_A = 25°C	5.5	8.5		MHz
LOW POWER TTL/CMOS INTERFACE						
Logical "1" Input Voltage $V_{IN(1)}$	54C	V_{CC} = 4.5V	V_{CC}−1.5			V
	74C	V_{CC} = 4.75V				
Logical "0" Input Voltage $V_{IN(0)}$	54C	V_{CC} = 4.5V			0.8	V
	74C	V_{CC} = 4.75V				
Logical "1" Output Voltage $V_{OUT(1)}$	54C	V_{CC} = 4.5V, I_D = −360 μA	2.4			V
	74C	V_{CC} = 4.75V, I_D = −360 μA				
Logical "0" Output Voltage $V_{OUT(0)}$	54C	V_{CC} = 4.5V, I_D = 360 μA			0.4	V
	74C	V_{CC} = 4.75V, I_D = 360 μA				
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)						
Output Source Current (I_{SOURCE})	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V, T_A = 25°C, V_{OUT} = 0V		−1.75			mA
Output Source Current (I_{SOURCE})	V_{CC} = 10V, $V_{IN(0)}$ = 0V, T_A = 25°C, V_{OUT} = 0V		−8.0			mA
Output Sink Current (I_{SINK})	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V, T_A = 25°C, V_{OUT} = V_{CC}		1.75			mA
Output Sink Current (I_{SINK})	V_{CC} = 10V, $V_{IN(1)}$ = 10V, T_A = 25°C, V_{OUT} = V_{CC}		8.0			mA

Note: These devices should not be connected under power on condition.

switching time waveforms

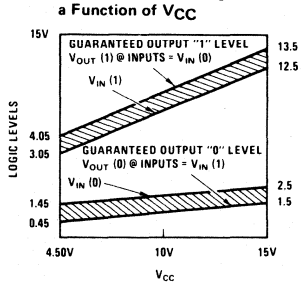


truth table

INPUTS AT t_n		OUTPUTS AT t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

Note: H = HIGH LEVEL, L = LOW LEVEL
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
Q_{An} = State of Q_A at t_n

Guaranteed noise Margin as a Function of V_{CC}



National Semiconductor

MM54C200/MM74C200 256-Bit TRI-STATE® Random Access Read/Write Memory

general description

The MM54C200/MM74C200 is a 256-bit random access read/write memory. Inputs consist of eight address lines, a data input line, a write enable line, and three chip enables. The eight binary address inputs are decoded internally to select each of the 256 locations. An internal address register, latches and address information on the positive to negative edge of $\overline{CE}_3$. The TRI-STATE data output line working in conjunction with $\overline{CE}_1$ or $\overline{CE}_2$ inputs provides for easy memory expansion.

Address Operation: Address inputs must be stable t_{SA} prior to the positive to negative transition of $\overline{CE}_3$. It is thus not necessary to hold address information stable for more than t_{HA} after the memory is enabled (positive to negative transition).

Note: The timing is different than the DM74200 in that a positive to negative transition of the memory enable must occur for the memory to be selected.

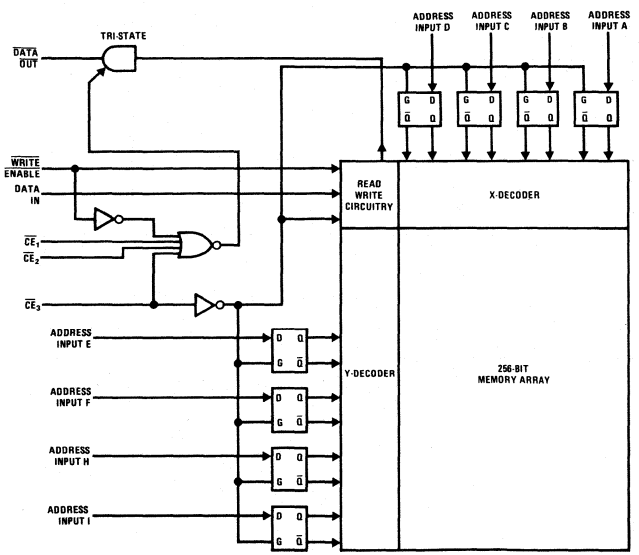
Read Operation: The data is read out by selecting the proper address and bringing $\overline{CE}_3$ low and write enable high. Holding $\overline{CE}_1$ or $\overline{CE}_2$ or $\overline{CE}_3$ at a high level forces the output into TRI-STATE. When used in bus organized systems, $\overline{CE}_1$, or $\overline{CE}_2$, a TRI-STATE control, provides for fast access times by not totally disabling the chip.

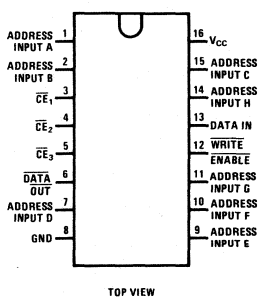
Write Operation: Data is written into the memory with $\overline{CE}_3$ low and write enable low. The state of $\overline{CE}_1$ or $\overline{CE}_2$ has no effect on the write cycle. The output assumes TRI-STATE with write enable low.

features

■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatibility	fan out of 1 driving standard TTL
■ Low power	500 nW typ
■ Internal address register	

logic and connection diagrams





TOP VIEW

Order Number MM54C200D or MM74C200D
See Package 3

Order Number MM74C200N
See Package 15

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C200	−55°C to +125°C
MM74C200	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.10	600	μA
CMOS/TTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC} − 1.5			V
	74C, V_{CC} = 4.75V	V_{CC} − 1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V	−4.0	−6.0		mA
	T_A = 25°C	−1.8			
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V	−16.0	−25		mA
	T_A = 25°C	−1.50			
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}	5.0	8.0		mA
	T_A = 25°C				
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}	20.0	30		mA
	T_A = 25°C				

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Access Time From Address (t_{ACC})	V_{CC} = 5.0V		450	900	ns
	V_{CC} = 10V		200	400	ns
Propagation Delay From $\overline{CE}_3$ (t_{pd})	V_{CC} = 5.0V		360	700	ns
	V_{CC} = 10V		120	300	ns
Propagation Delay From $\overline{CE}_1$ or $\overline{CE}_2$ ($t_{p\overline{CE}1}$)	V_{CC} = 5 0V		250	500	ns
	V_{CC} = 10V		85	200	ns
Address Setup Time (t_{SA})	V_{CC} = 5.0V	200	80		ns
	V_{CC} = 10V	100	30		ns
Address Hold Time (t_{HA})	V_{CC} = 5.0V	50	15		ns
	V_{CC} = 10V	25	5		ns

ac electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width ($t_{\overline{WE}}$)	V_{CC} = 5.0V	300	160		ns
	V_{CC} = 10V	150	70		ns
$\overline{CE}_3$ Pulse Widths (t_{CE})	V_{CC} = 5.0V	400	200		ns
	V_{CC} = 10V	160	80		ns
Input Capacity (C_{IN})	Any Input (Note 2)		5.0		pF
Output Capacity in TRI-STATE (C_{OUT})	(Note 2)		9.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3)		400		pF

C_L = 50 pF

PARAMETER		CONDITIONS	MM54C200 T_A = -55°C to +125°C		MM74C200 T_A = -45°C to +85°C		UNITS
			MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address	V_{CC} = 5V		1200		1100	ns
		V_{CC} = 10V		520		480	
t_{pd}	Propagation Delay from $\overline{CE}_3$	V_{CC} = 5V		950		850	ns
		V_{CC} = 10V		400		360	ns
$t_{pd\overline{CE}_1}$	Propagation Delay from $\overline{CE}_1$ or $\overline{CE}_2$	V_{CC} = 5V		650		600	ns
		V_{CC} = 10V		300		275	ns
t_{SA}	Address Setup Time	V_{CC} = 5V	250		250		ns
		V_{CC} = 10V	120		120		ns
t_{HA}	Address Hold Time	V_{CC} = 5V	100		100		ns
		V_{CC} = 10V	50		50		ns
$t_{\overline{WE}}$	$\overline{\text{Write}}$ $\overline{\text{Enable}}$ Pulse Width	V_{CC} = 5V	450		400		ns
		V_{CC} = 10V	225		200		ns
t_{CE}	Disable Pulse Width	V_{CC} = 5V	500		460		ns
		V_{CC} = 10V	250		230		ns
t_{HD}	Data Hold Time	V_{CC} = 5V	50		50		ns
		V_{CC} = 10V	25		25		ns

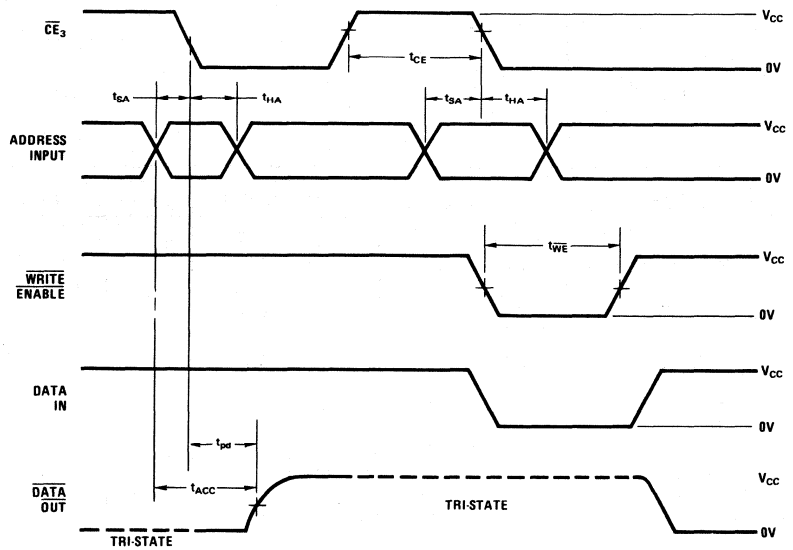
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

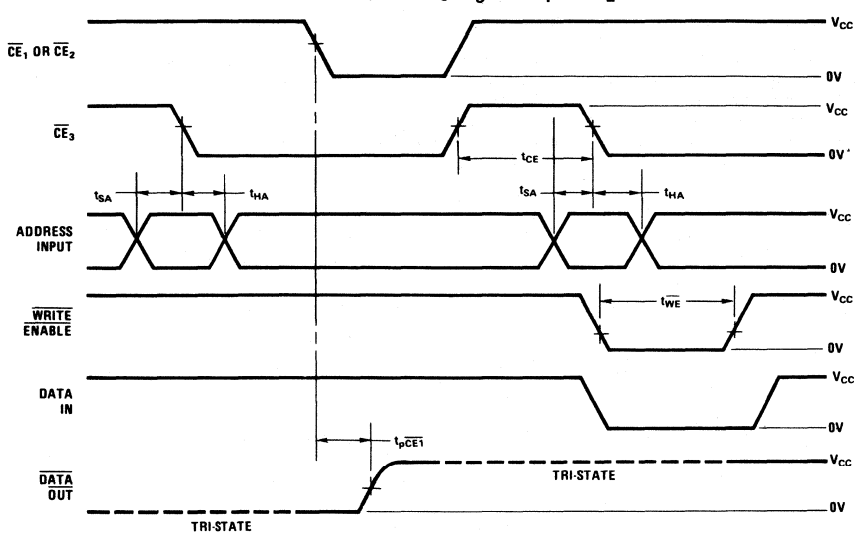
Note 3: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

switching time waveforms

Read and Write Cycles Using $\overline{CE}_3$ ($\overline{CE}_1$ = $\overline{CE}_2$ = logic 0)



Read and Write Cycles Using $\overline{CE}_3$ and $\overline{CE}_1$ (or $\overline{CE}_2$)



Note: Used for fast access time in bused systems.

National Semiconductor

MM54C221/MM74C221 Dual Monostable Multivibrator

general description

The MM54C221/MM74C221 dual monostable multivibrator is monolithic complementary MOS integrated circuit. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input, and a clear input.

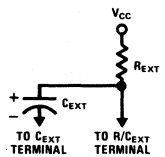
Once fired, the output pulses are independent of further transitions of the A and B inputs and are a function of the external timing components C_{EXT} and R_{EXT}. The pulse width is stable over a wide range of temperature and V_{CC}. Pulse stability will be limited by the accuracy of external timing components. The pulse width is approximately defined by the relationship $t_{W(OUT)} \approx C_{EXT}\ R_{EXT}$. For further information and applications, see AN-138.

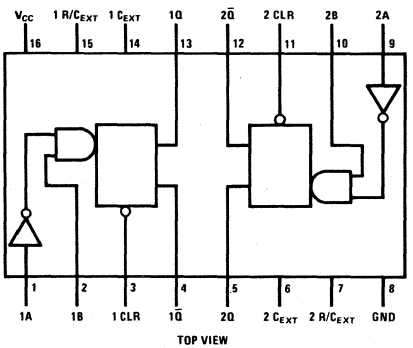
features

■ Wide supply voltage range	4.5V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} typ
■ Low power	fan out of 2
TTL compatibility	driving 74L

connection diagrams

Timing Component





truth table

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎍ = One low level pulse
X = Irrelevant

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	4.5V to 15V
MM54C221	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C221	−40°C to +85°C	$R_{EXT} \geq 80\ V_{CC}$ (Ω)	
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC}) (Standby)	V_{CC} = 15V, R_{EXT} = ∞, Q1, Q2 = Logic 0 (Note 3)		0.05	300	μA
Supply Current (I_{CC}) (During Output Pulse)	V_{CC} = 15V, Q1 = Logic 1, Q2 = Logic 0 (Figure 4)		15		mA
	V_{CC} = 5.0V, Q1 = Logic 1, Q2 = Logic 0 (Figure 4)		2		mA
Leakage Current at R/C_{EXT} Pin	V_{CC} = 15V, V_{CEXT} = 5.0V		0.01	3	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C221	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C221	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C221	V_{CC} = 4.5V			0.8	V
MM74C221	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C221	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C221	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C221	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C221	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Trigger Input (A, B) to Output Q, $\overline{Q}$ ($t_{PD\ A,B}$)	$V_{CC} = 5.0V$		250	500	ns
	$V_{CC} = 10V$		120	250	ns
Propagation Delay from Clear Input (CL) to Output Q, $\overline{Q}$ (t_{PDCL})	$V_{CC} = 5.0V$		250	500	ns
	$V_{CC} = 10V$		120	250	ns
Time Prior to Trigger Input (A,B) that Clear must be set (t_{SET})	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	60	20		ns
Trigger Input (A, B) Pulse Width ($t_{W(A,B)}$)	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	70	30		ns
Clear Input (CL) Pulse Width ($t_{W(CL)}$)	$V_{CC} = 5.0V$	150	50		ns
	$V_{CC} = 10V$	70	30		ns
Q or $\overline{Q}$ Output Pulse Width ($t_{W(OUT)}$)	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		900		ns
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		350		ns
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 0$ pF		320		ns
	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF (Figure 1)	9	10.6	12.2	μs
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF (Figure 1)	9	10	11	μs
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 1000$ pF (Figure 1)	8.9	9.8	10.8	μs
	$V_{CC} = 5.0V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu$F (Figure 2)	900	1020	1200	μs
	$V_{CC} = 10V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu$F (Figure 2)	900	1000	1100	μs
	$V_{CC} = 15V$, $R_{EXT} = 10k$, $C_{EXT} = 0.1\mu$F (Figure 2)	900	990	1100	μs
ON Resistance of Transistor Between R/C_{EXT} to C_{EXT} (R_{ON})	$V_{CC} = 5.0V$ (Note 4)		50	150	Ω
	$V_{CC} = 10V$ (Note 4)		25	65	Ω
	$V_{CC} = 15V$ (Note 4)		16.7	45	Ω
Output Duty Cycle	$R = 10k$, $C = 1000$ pF			90	%
	$R = 10k$, $C = 0.1\mu$F (Note 5)			90	%
Input Capacitance (C_{IN})	R/C_{EXT} Input (Note 2)		15	25	pF
	Any Other Input (Note 2)		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: In Standby (Q = Logic 0) the power dissipated equals the leakage current plus V_{CC}/R_{EXT}.

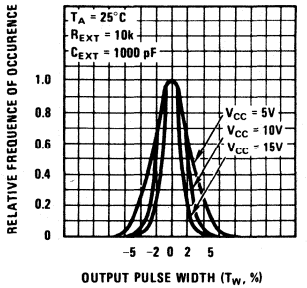
Note 4: See An-138 for detailed explanation of R_{ON}.

Note 5: Maximum output duty cycle $= \dfrac{R_{EXT}}{R_{EXT} + 1000}$

typical performance characteristics

Figure 1

Typical Distribution of Units for Output Pulse Width

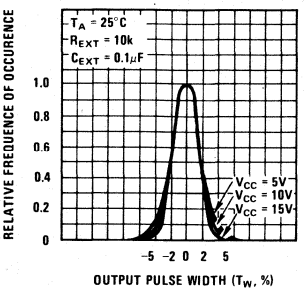


0% Point pulse width:
At V_{CC} = 5V, T_W = 10.6μs
At V_{CC} = 10V, T_W = 10μs
At V_{CC} = 15V, T_W = 9.8μs

Percentage of units within ±4%:
At V_{CC} = 5V, 90% of units
At V_{CC} = 10V, 95% of units
At V_{CC} = 15V, 98% of units

Figure 2

Typical Distribution of Units for Output Pulse Width



0% Point pulse width:
At V_{CC} = 5V, T_W = 1020μs
At V_{CC} = 10V, T_W = 1000μs
At V_{CC} = 15V, T_W = 982μs

Percentage of units within ±4%:
At V_{CC} = 5V, 95% of units
At V_{CC} = 10V, 97% of units
At V_{CC} = 15V, 98% of units

Figure 3

Typical Variation in Output Pulse Width vs Temperature

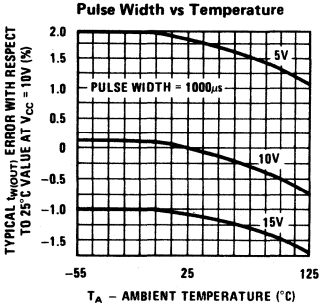
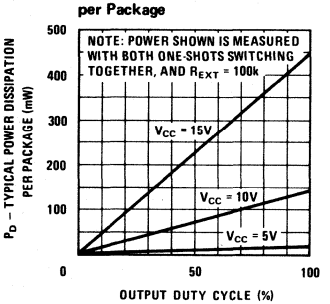
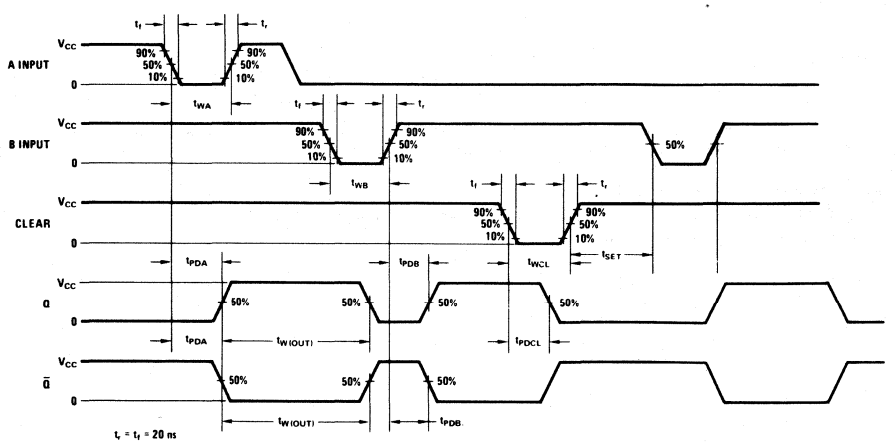


Figure 4

Typical Power Dissipation per Package



switching time waveforms



National Semiconductor

advance information

MM54C240/MM74C240 Inverting Outputs
MM54C244/MM74C244 Non-inverting Outputs
Octal Buffers and Line Drivers with TRI-STATE® Outputs

general description

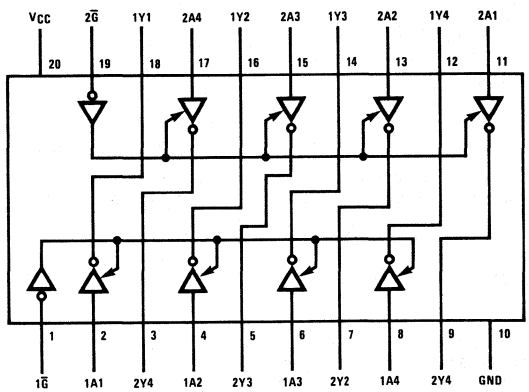
These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads. A high logic level on the output disable control input G makes the outputs go into the high impedance state.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- High capacitive load
- TRI-STATE® outputs
- Input protection
- TTL compatibility
- 20-pin dual-in-line package

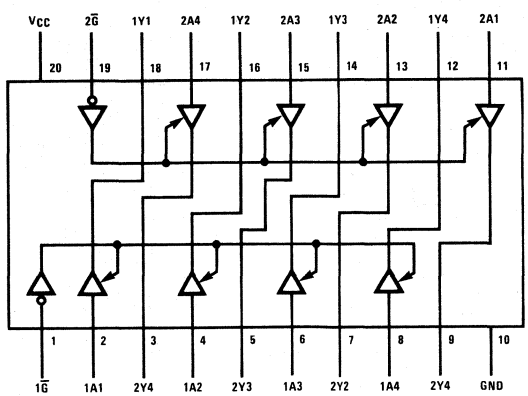
connection diagrams

(TOP VIEW)



MM74C240

(TOP VIEW)



MM74C244

National Semiconductor

MM54C373/MM74C373 TRI-STATE® Octal D-Type Latch
MM54C374/MM74C374 TRI-STATE® Octal D-Type Flip-Flop

General Description

The MM54C373/MM74C373, MM54C374/MM74C374 are integrated, complementary MOS (CMOS), 8-bit storage elements with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads, such as one might find when driving a bus, and to have a fan-out of 1 when driving standard TTL. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The MM54C373/MM74C373 is an 8-bit latch. When LATCH ENABLE is high the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs, which meets the set-up and hold time requirements, will be retained at the outputs until LATCH ENABLE returns high again.

The MM54C374/MM74C374 is an 8-bit, D-type, positive-edge triggered flip-flop. Data at the D inputs, meeting the set-up and hold time requirements, is transferred to the Q outputs on positive-going transitions of the CLOCK input.

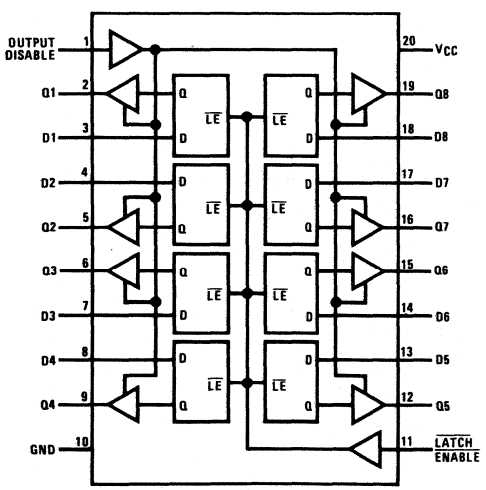
Both the MM54C373/MM74C373 and the MM54C374/MM74C374 are being assembled in 20-pin dual-in-line packages with 0.300" pin centers.

Features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- TTL compatibility — fan-out of 1 driving standard TTL
- Bus driving capability
- TRI-STATE outputs
- Eight storage elements in one package
- Single CLOCK/LATCH ENABLE and OUTPUT DISABLE control inputs
- 20-pin dual-in-line package with 0.300" centers takes half the board space of a 24-pin package

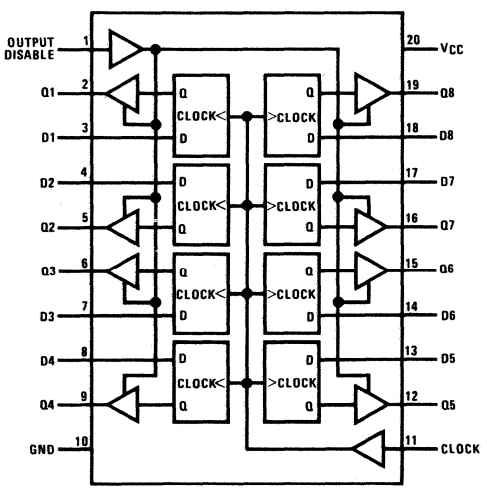
Connection Diagrams

MM54C373/MM74C373
Dual-In-Line Package



TOP VIEW

MM54C374/MM74C374
Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C373, MM54C374	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C373, MM74C374	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C		

DC Electrical Characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10 μA			0.5	V
		V_{CC} = 10V, I_O = 10 μA			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{OZ}	TRI-STATE Leakage Current	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
		74C, V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = −360 μA	V_{CC}−0.4			V
		74C, V_{CC} = 4.75V, I_O = −360 μA	V_{CC}−0.4			V
		54C, V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
		74C, V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
		74C, V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C, (Note 4)	−12.0	−24		mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C, (Note 4)	−24.0	−48		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C, (Note 4)	6.0	12		mA
I_{SINK}	Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C, (Note 4)	24.0	48		mA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, t_r = t_f = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}, t_{pd0}	Propagation Delay, $\overline{\text{LATCH ENABLE}}$	V_{CC} = 5V, C_L = 50 pF		165	330	ns
	to Output	V_{CC} = 10V, C_L = 50 pF		70	140	ns
	MM54C373, MM74C373	V_{CC} = 5V, C_L = 150 pF		195	390	ns
		V_{CC} = 10V, C_L = 150 pF		85	170	ns

AC Electrical Characteristics (Continued) $T_A = 25°C$, $C_L = 50$ pF, $t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd1}, t_{pd0}	Propagation Delay Data In to Output	$\overline{\text{LATCH ENABLE}} = V_{CC}$				
	MM54C373, MM74C373	$V_{CC} = 5V$, $C_L = 50$ pF		155	310	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		70	140	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		185	370	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		85	170	ns
t_{pd1}, t_{pd0}	Propagation Delay CLOCK to Output	$V_{CC} = 5V$, $C_L = 50$ pF		150	300	ns
	MM54C374/MM74C374	$V_{CC} = 10V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		180	360	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		80	160	ns
$t_{SET\text{-}UP}$	Minimum Set-Up Time Data In to CLOCK/$\overline{\text{LATCH ENABLE}}$	$t_{HOLD} = 0$ ns				
		$V_{CC} = 5V$		70	140	ns
		$V_{CC} = 10V$		35	70	ns
t_{PWH}	Minimum $\overline{\text{LATCH ENABLE}}$ Pulse Width	$V_{CC} = 5V$		75	150	ns
		$V_{CC} = 10V$		55	110	ns
	MM54C373, MM74C373					
t_{PWH}, t_{PWL}	Minimum CLOCK Pulse Width	$V_{CC} = 5V$		70	140	ns
	MM54C374, MM74C374	$V_{CC} = 10V$		50	100	ns
f_{MAX}	Maximum $\overline{\text{LATCH ENABLE}}$ Frequency	$V_{CC} = 5V$		6.7	3.3	MHz
		$V_{CC} = 10V$		9.0	4.5	MHz
	MM54C373, MM74C373					
f_{MAX}	Maximum CLOCK Frequency	$V_{CC} = 5V$		7.0	3.5	MHz
	MM54C374, MM74C374	$V_{CC} = 10V$		10.0	5.0	MHz
t_{1H}, t_{0H}	Propagation Delay OUTPUT DISABLE to High Impedance State (From a Logic Level)	$R_L = 10k$, $C_L = 5$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		60	120	ns
t_{H1}, t_{H0}	Propagation Delay OUTPUT DISABLE to Logic Level (From High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
		$V_{CC} = 5V$		105	210	ns
		$V_{CC} = 10V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{CC} = 5V$, $C_L = 50$ pF		65	130	ns
		$V_{CC} = 10V$, $C_L = 50$ pF		35	70	ns
		$V_{CC} = 5V$, $C_L = 150$ pF		110	220	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		70	140	ns
t_r, t_f	Maximum $\overline{\text{LATCH ENABLE}}$ Rise and Fall Time	$V_{CC} = 5V$		NA		μs
		$V_{CC} = 10V$		NA		μs
	MM54C373, MM74C373					
t_r, t_f	Maximum CLOCK Rise and Fall Time	$V_{CC} = 5V$	15	>2000		μs
	MM54C374, MM74C374	$V_{CC} = 10V$	5	>2000		μs
C_{CLK}, $C_{\overline{LE}}$	Input Capacitance	CLOCK/$\overline{\text{LE}}$ Input		7.5	10	pF
C_{OD}	Input Capacitance	OUTPUT DISABLE Input, (Note 2)		7.5	10	pF
C_{IN}	Input Capacitance	Any Other Input, (Note 2)		5.0	7.5	pF
C_{OUT}	Output Capacitance	High Impedance State, (Note 2)		10	15	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		200		pF
	MM54C373, MM74C373					
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		250		pF
	MM54C374, MM74C374					

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

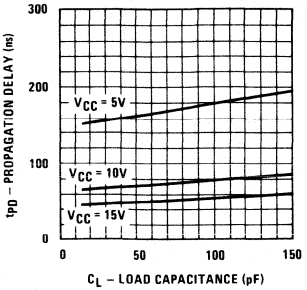
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

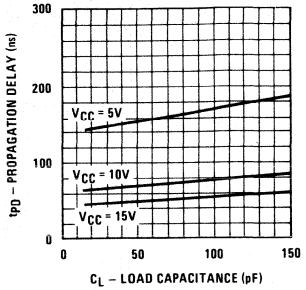
Note 4: These are peak output current capabilities. Continuous output current is rated at 12 mA max.

Typical Performance Characteristics $T_A = 25°C$

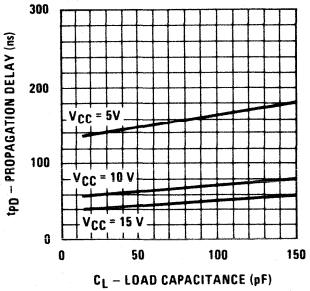
MM54C373/MM74C373
Propagation Delay, $\overline{\text{LATCH ENABLE}}$ to Output vs Load Capacitance



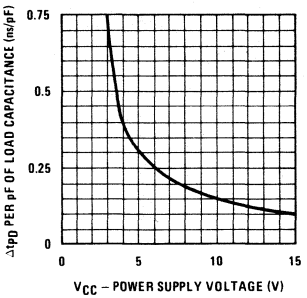
MM54C373/MM74C373
Propagation Delay, Data In to Output vs Load Capacitance



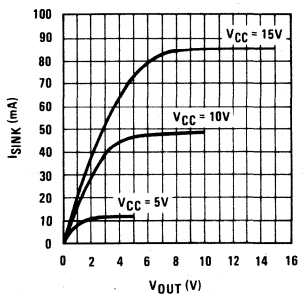
MM54C374/MM74C374
Propagation Delay, CLOCK to Output vs Load Capacitance



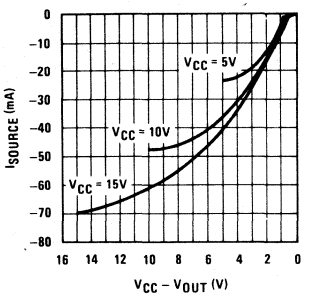
MM54C373/MM74C373,
MM54C374/MM74C374
Change in Propagation Delay per pF of Load Capacitance ($\Delta t_{PD}/pF$) vs Power Supply Voltage



MM54C373/MM74C373,
MM54C374/MM74C374
Output Sink Current vs V_{OUT}



MM54C373/MM74C373,
MM54C374/MM74C374 Output Source Current vs $V_{CC} - V_{OUT}$



Truth Tables

MM54C373/MM74C373

OUTPUT DISABLE	$\overline{\text{LATCH ENABLE}}$	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q
H	X	X	Hi-Z

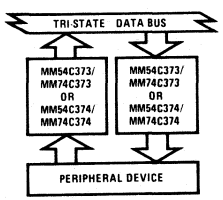
MM54C374/MM74C374

OUTPUT DISABLE	CLOCK	D	Q
L	⌐	H	H
L	⌐	L	L
L	L	X	Q
L	H	X	Q
H	X	X	Hi-Z

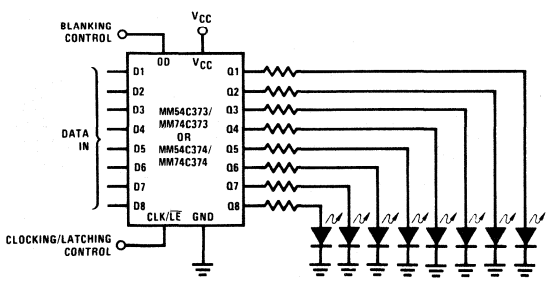
L = low logic level
H = high logic level
X = irrelevant
⌐ = low to high logic level transition
Q = preexisting output level
Hi-Z = high impedance output state

Typical Applications

Data Bus Interfacing Element

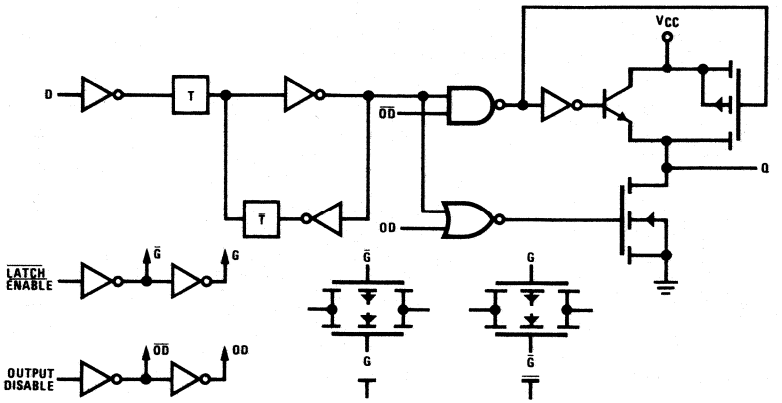


Simple, Latching, Octal, LED Indicator Driver with Blanking For Use As Data Display, Bus Monitor, μP Front Panel Display, Etc.

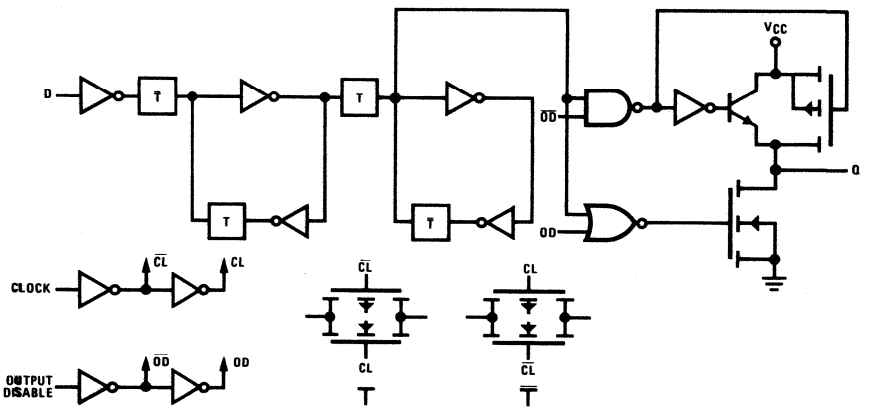


Logic Diagrams

MM54C373/MM74C373 (1 of 8 Latches)

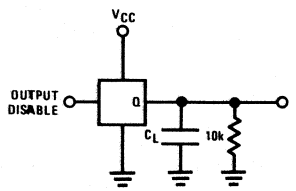


MM54C374/MM74C374 (1 of 8 Flip-Flops)

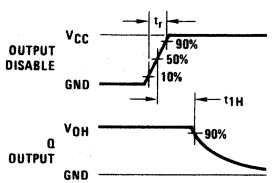


TRI-STATE® Test Circuits and Timing Diagrams

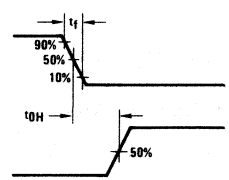
t_{1H}, t_{H1}



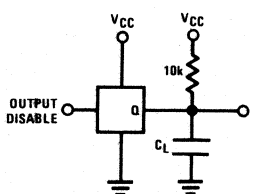
t_{1H}, C_L = 5 pF



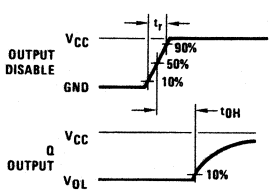
t_{H1}, C_L = 50 pF



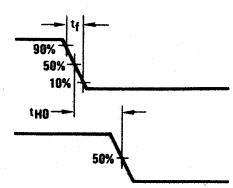
t_{0H}, t_{H0}



t_{0H}, C_L = 5 pF

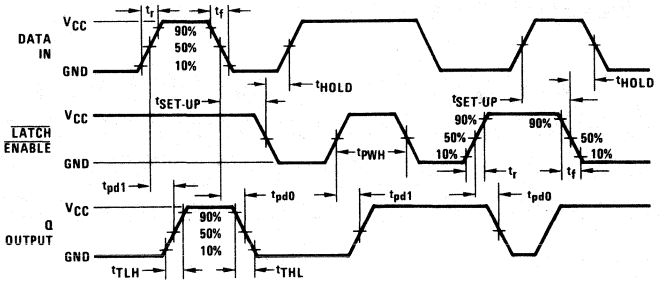


t_{H0}, C_L = 50 pF



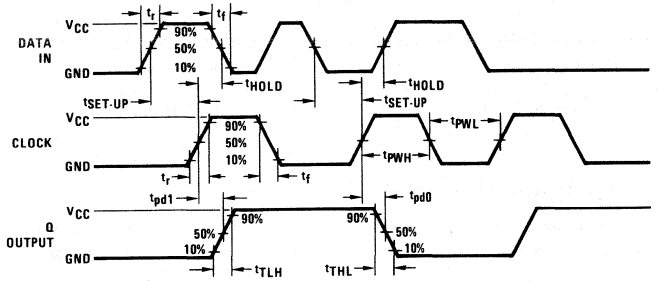
Switching Time Waveforms

MM54C373/MM74C373



OUTPUT DISABLE = GND

MM54C374/MM74C374



OUTPUT DISABLE = GND

National Semiconductor

MM54C901/MM74C901 Hex Inverting TTL Buffer
MM54C902/MM74C902 Hex Non-Inverting TTL Buffer
MM54C903/MM74C903 Hex Inverting CMOS Buffer
MM54C904/MM74C904 Hex Non-Inverting CMOS Buffer

general description

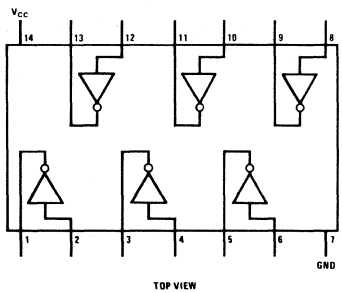
These hex buffers employ complementary MOS to achieve wide supply operating range, low power consumption, high noise immunity. These buffers provide direct interface from PMOS into CMOS or TTL and direct interface from CMOS to TTL or CMOS operating at a reduced V_{CC} supply. For specific applications see MOS Brief 18 in the back of this catalog.

features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatibility — fan out of 2 driving standard TTL

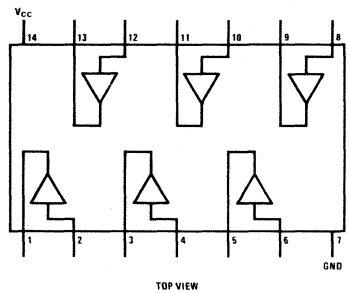
connection and logic diagrams

MM54C901/MM74C901
MM54C903/MM74C903



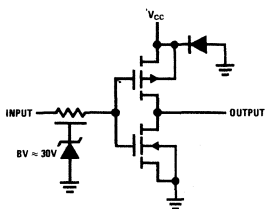
TOP VIEW

MM54C902/MM74C902
MM54C904/MM74C904

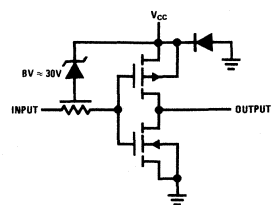


TOP VIEW

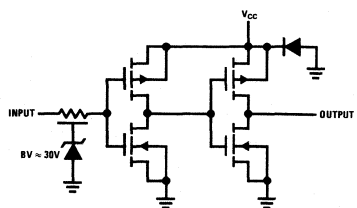
MM54C901/MM74C901
CMOS to TTL Inverting Buffer



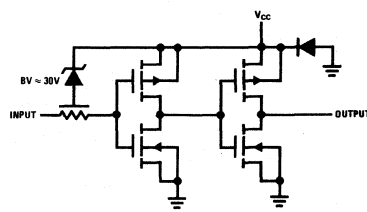
MM54C903/MM74C903
PMOS to TTL or CMOS Inverting Buffer



MM54C902/MM74C902
CMOS to TTL Buffer



MM54C904/MM74C904
PMOS to TTL or CMOS Buffer



absolute maximum ratings (Note 1)

Voltage at Any Output Pin	$-0.3V$ to V_{CC} $+0.3V$
Voltage at Any Input Pin	
MM54C901/MM74C901	$-0.3V$ to $+15V$
MM54C902/MM74C902	$-0.3V$ to $+15V$
MM54C903/MM74C903	V_{CC} $-17V$ to V_{CC} $+0.3V$
MM54C904/MM74C904	V_{CC} $-17V$ to V_{CC} $+0.3V$
Operating Temperature Range	
MM54C901, MM54C902, MM54C903, MM54C904	$-55°C$ to $+125°C$
MM74C901, MM74C902, MM74C903, MM74C904	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	$300°C$

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = $-10\mu A$	4.5			V
	V_{CC} = 10V, I_O = $-10\mu A$	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = $+10\mu A$			0.5	V
	V_{CC} = 10V, I_O = $+10\mu A$			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	-1.0	-0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	15	μA
TTL TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	$V_{CC}-1.5$			V
	74C, V_{CC} = 4.75V	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
CMOS TO TTL					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V	4.0			V
MM54C902, MM54C904	V_{CC} = 4.5V	$V_{CC}-1.5$			V
MM74C901, MM74C903	V_{CC} = 4.75	4.25			V
MM74C902, MM74C904	V_{CC} = 4.75	$V_{CC}-1.5$			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V			1.0	V
MM54C902, MM54C904	V_{CC} = 4.5V			1.5	V
MM74C901, MM74C903	V_{CC} = 4.75			1.0	V
MM74C902, MM74C904	V_{CC} = 4.75			1.5	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = $-800\mu A$	2.4			V
	74C, V_{CC} = 4.75V, I_O = $-800\mu A$	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C901, MM54C903	V_{CC} = 4.5V, I_O = 2.6 mA			0.4	V
MM54C902, MM54C904	V_{CC} = 4.5V, I_O = 3.2 mA			0.4	V
MM74C901, MM74C903	V_{CC} = 4.75V, I_O = 2.6 mA			0.4	V
MM74C902, MM74C904	V_{CC} = 4.75V, I_O = 3.2 mA			0.4	V
OUTPUT DRIVE (MM54C901/MM74C901, MM54C903/MM74C903) (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C, V_{IN} = 0V	-5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C, V_{IN} = 0V	-20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C, V_{IN} = V_{CC}	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V, T_A = 25°C, V_{IN} = V_{CC}	3.8			mA

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (MM54C902/MM74C902, MM54C904/MM74C904 (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	−5.0			mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V T_A = 25°C, V_{IN} = V_{CC}	−20			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC} T_A = 25°C, V_{IN} = 0V	9			mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = 0.4V T_A = 25°C, V_{IN} = 0V	3.8			mA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
MM54C901/MM74C901, MM54C903/MM74C903					
Input Capacitance (C_{IN})	Any Input (Note 2)		14		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		38 22	70 30	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		21 13	35 20	ns ns
MM54C902/MM74C902, MM54C904/MM74C904					
Input Capacitance (C_{IN})	Any Input (Note 2)		5.0		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		50		pF
Propagation Delay Time to a Logical "1" ($t_{pd(1)}$)	V_{CC} = 5.0V V_{CC} = 10V		57 27	90 40	ns ns
Propagation Delay Time to a Logical "0" ($t_{pd(0)}$)	V_{CC} = 5.0V V_{CC} = 10V		54 25	90 40	ns ns

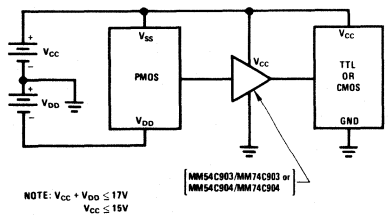
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

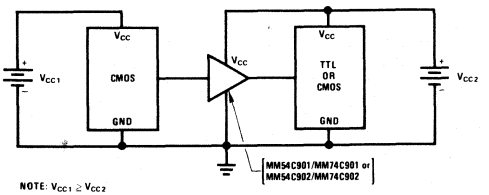
typical applications

PMOS to CMOS or TTL Interface



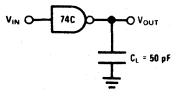
NOTE: $V_{CC} + V_{DD} \leq 17V$
$V_{CC} \leq 15V$

CMOS to TTL or CMOS at a Lower V_{CC}



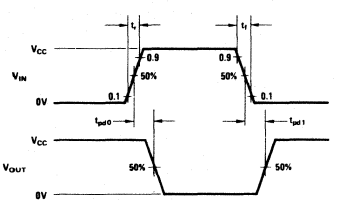
NOTE: $V_{CC1} \geq V_{CC2}$

ac test circuit and switching time waveforms



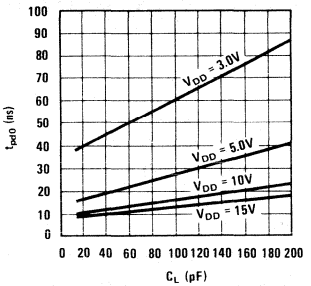
Note: Delays measured with input t_r, t_f = 20 ns.

CMOS to CMOS

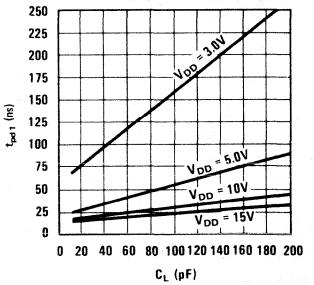


typical performance characteristics

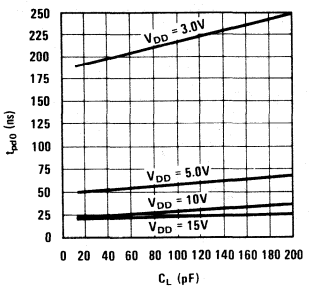
Typical Propagation Delay to a Logical "0" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



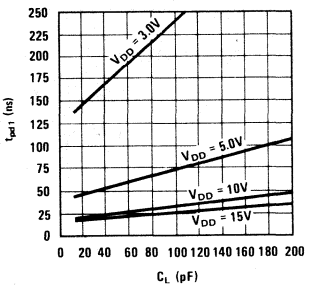
Typical Propagation Delay to a Logical "1" for the MM54C901/ MM74C901 and MM54C903/ MM74C903



Typical Propagation Delay to a Logical "0" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



Typical Propagation Delay to a Logical "1" for the MM54C902/ MM74C902 and MM54C904/ MM74C904



National Semiconductor

MM54C905/MM74C905 12-Bit Successive Approximation Register

general description

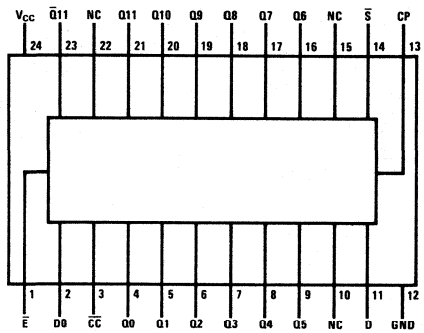
The MM54C905/MM74C905 CMOS 12-bit successive approximation register contains all the digit control and storage necessary for successive approximation analog-to-digital conversion. Because of the unique capability of CMOS to switch to each supply rail without any offset voltage, it can also be used in digital systems as the control and storage element in repetitive routines.

features

- Wide supply voltage range 3.0V to 15V
- Guaranteed noise margin 1.0V
- High noise immunity 0.45 V_{CC} typ
- Low power TTL compatibility fan out of 2 driving 74L
- Provision for register extension or truncation
- Operates in START/STOP or continuous conversion mode
- Drive ladder switches directly. For 10 bits or less with 50k/100k R/2R ladder network

connection diagram

Dual-In-Line Package



truth table

TIME	INPUTS			OUTPUTS												
t_n	D	$\overline{S}$	$\overline{E}$	D0	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X	X	X	X	X
1	D11	H	L	X	L	H	H	H	H	H	H	H	H	H	H	H	H
2	D10	H	L	D11	D11	L	H	H	H	H	H	H	H	H	H	H	H
3	D9	H	L	D10	D11	D10	L	H	H	H	H	H	H	H	H	H	H
4	D8	H	L	D9	D11	D10	D9	L	H	H	H	H	H	H	H	H	H
5	D7	H	L	D8	D11	D10	D9	D8	L	H	H	H	H	H	H	H	H
6	D6	H	L	D7	D11	D10	D9	D8	D7	L	H	H	H	H	H	H	H
7	D5	H	L	D6	D11	D10	D9	D8	D7	D6	L	H	H	H	H	H	H
8	D4	H	L	D5	D11	D10	D9	D8	D7	D6	D5	L	H	H	H	H	H
9	D3	H	L	D4	D11	D10	D9	D8	D7	D6	D5	D4	L	H	H	H	H
10	D2	H	L	D3	D11	D10	D9	D8	D7	D6	D5	D4	D3	L	H	H	H
11	D1	H	L	D2	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	L	H	H
12	D0	H	L	D1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	L	H
13	X	H	L	D0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
14	X	X	L	X	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = High level
L = Low level
X = Don't care
NC = No change

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range	
MM54C905	−55°C to +125°C
MM74C905	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	16V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5.0V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5.0V, I_O = 10μA			0.5	V
	V_{CC} = 10V, I_O = 10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	300	μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)					
MM54C905	V_{CC} = 4.5V	V_{CC}−1.5			V
MM74C905	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
MM54C905	V_{CC} = 4.5V			0.8	V
MM74C905	V_{CC} = 4.75V			0.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)					
MM54C905	V_{CC} = 4.5V, I_O = −360μA	2.4			V
MM74C905	V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)					
MM54C905	V_{CC} = 4.5V, I_O = 360μA			0.4	V
MM74C905	V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5.0V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5.0V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA
Q11−Q0 Outputs	V_{CC} = 10V ±5%				
R_{SOURCE}	V_{OUT} = V_{CC} − 0.3V, T_A = 25°C	150		350	Ω
R_{SINK}	V_{CC} = 10V ±5%				
	V_{OUT} = 0.3V, T_A = 25°C	80		230	Ω

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

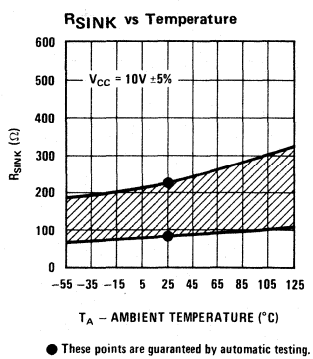
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time From Clock Input To Outputs (Q0–Q11) ($t_{pd(Q)}$)	$V_{CC} = 5.0V$		200	350	ns
	$V_{CC} = 10V$		80	150	ns
Propagation Delay Time From Clock Input To D_O ($t_{pd(D_O)}$)	$V_{CC} = 5.0V$		180	325	ns
	$V_{CC} = 10V$		70	125	ns
Propagation Delay Time From Register Enable ($\overline{E}$) To Output (Q11) ($t_{pd(\overline{E})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	150	ns
Propagation Delay Time From Clock To $\overline{CC}$ ($t_{pd(\overline{CC})}$)	$V_{CC} = 5.0V$		190	350	ns
	$V_{CC} = 10V$		75	0.50	ns
Data Input Set-Up Time (t_{DS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Start Input Set-Up Time (t_{SS})	$V_{CC} = 5.0V$	80			ns
	$V_{CC} = 10V$	30			ns
Minimum Clock Pulse Width (t_{PWL}, t_{PWH})	$V_{CC} = 5.0V$	250	125		ns
	$V_{CC} = 10V$	100	50		ns
Maximum Clock Rise and Fall Time (t_r, t_f)	$V_{CC} = 5.0V$			15	μs
	$V_{CC} = 10V$			5	μs
Maximum Clock Frequency (f_{MAX})	$V_{CC} = 5.0V$	2	4		MHz
	$V_{CC} = 10V$	5	10		MHz
Clock Input Capacitance (C_{CLK})	Clock Input (Note 2)		10		pF
Input Capacitance (C_{IN})	Any Other Input (Note 2)		5		pF
Power Dissipation Capacitance (C_{PD})	(Note 3)		100		pF

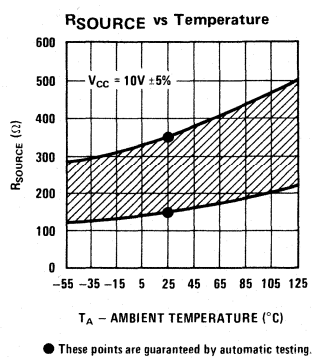
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

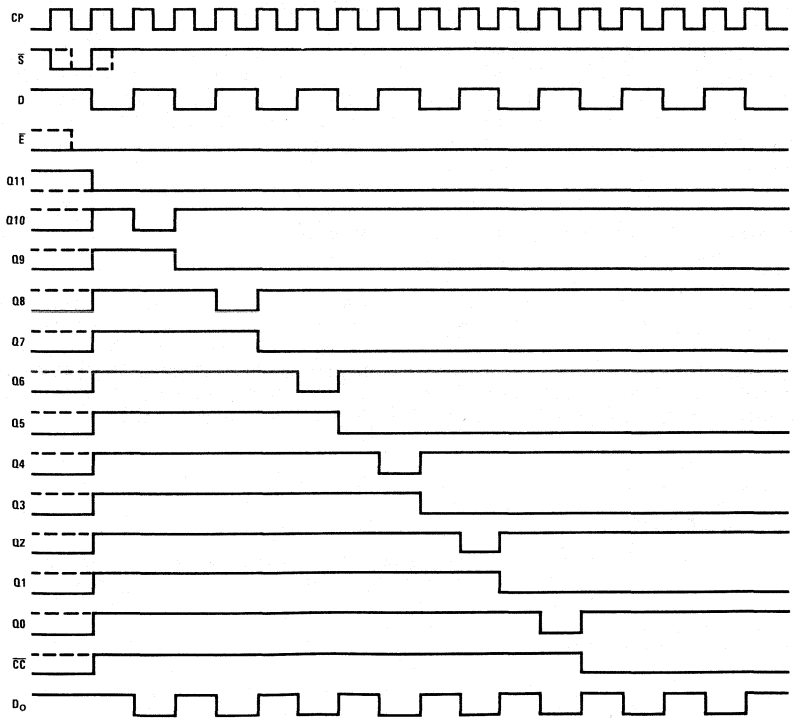
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

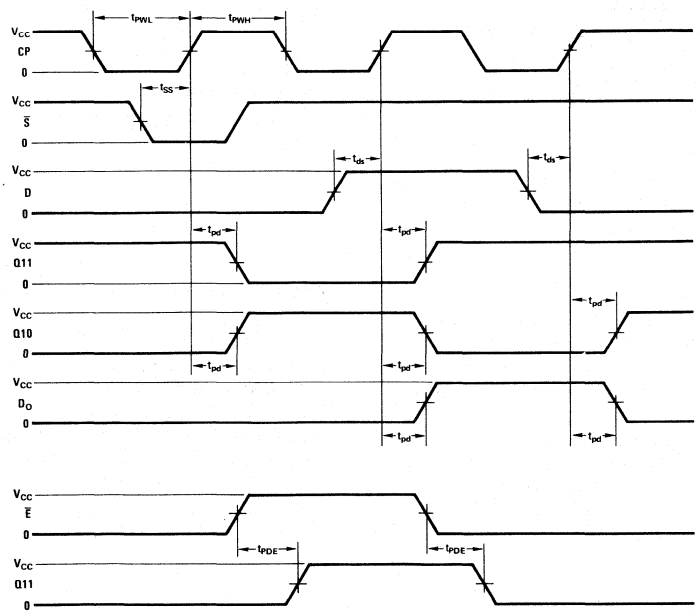




timing diagram



switching time waveforms



USER NOTES FOR A/D CONVERSION

The register can be used with either current switches that require a low voltage level to turn the switch ON or current switches that require a high voltage level to turn the switch ON. If current switches are used which turn ON with a low logic level, the resulting digit output from the register is active low. That is, a logic "1" is represented as a low voltage level. If current switches are used which turn ON with a high logic level, the resulting digit output is active high. A logic "1" is represented as a high voltage level.

For a maximum error of ±1/2 LSB, the comparator must be biased. If current switches that require a high voltage level to turn ON are used, the comparator should be biased +1/2 LSB and if the current switches require a low logic level to turn ON, then the comparator must be biased −1/2 LSB.

The register can be used to perform 2's complement conversion by offsetting the comparator one half full range +1/2 LSB and using the complement of the MSB Q11 as the sign bit.

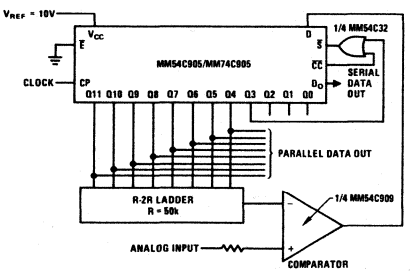
If the register is truncated and operated in the continuous conversion mode, a lock-up condition may occur on power-ON. This situation can be overcome by making the START input the "OR" function of $\overline{CC}$ and the appropriate register output.

The register, by suitable selection of register ladder network, can be used to perform either binary or BCD conversion.

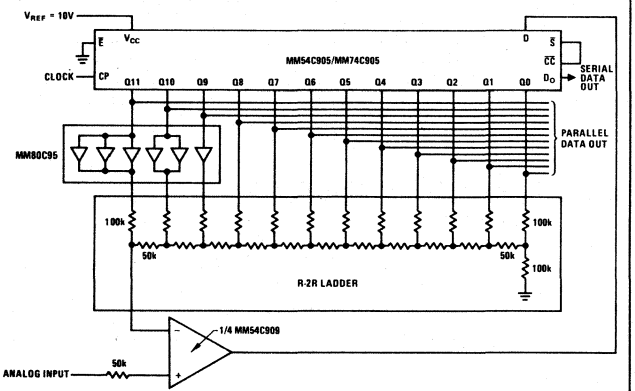
The register outputs can drive the 10 bits or less with 50k/100k R/2R ladder network directly for V_{CC} = 10V or higher. In order to drive the 12-bit 50k/100k ladder network and have the ±1/2 LSB resolution, the MM54C902/MM74C902 or MM54C904/MM74C904 is used as buffers, three buffers for MSB (Q11), two buffers for Q10, and one buffer for Q9.

typical applications

12-Bit Successive Approximation A-to-D Converter Operating in Continuous 8-Bit Truncated Mode



12-Bit Successive Approximation A-to-D Converter, Operating in Continuous Mode, Drives the 50k/100k Ladder Network Directly



definition of terms

CP: Register *clock* input.

$\overline{CC}$: *Conversion complete*—this output remains at $V_{OUT(1)}$ during a conversion and goes to $V_{OUT(0)}$ when conversion is complete.

D: Serial *data* input—connected to comparator output in A-to-D applications.

$\overline{E}$: *Register enable*—this input is used to expand the length of the register. When $\overline{E}$ is at $V_{IN(1)}$ Q11 is forced to $V_{OUT(1)}$ and inhibits conversion. When not used for expansion $\overline{E}$ must be connected to $V_{IN(0)}$ (GND).

Q11: True register MSB output.

$\overline{Q11}$: Complement of register MSB output.

Qi (i = 0 to 11): Register outputs.

$\overline{S}$: *Start input*—holding start input at $V_{IN(0)}$ for at least one clock period will initiate a conversion by setting MSB (Q11) at $V_{OUT(0)}$ and all other output (Q10–Q0) at $V_{OUT(1)}$. If set-up time requirements are met, a conversion may be initiated by holding start input at $V_{IN(0)}$ for less than one clock period.

DO: *Serial data output*—D input delayed by one clock period.

National Semiconductor

MM54C906/MM74C906 Hex Open Drain N-Channel Buffers
MM54C907/MM74C907 Hex Open Drain P-Channel Buffers

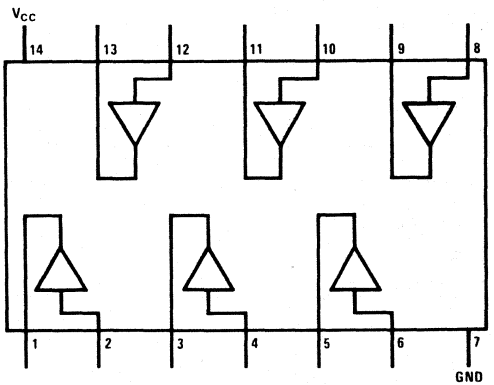
general description

These buffers employ monolithic CMOS technology in achieving open drain outputs. The MM54C906/MM74C906 consists of six inverters driving six N-channel devices; and the MM54C907/MM74C907 consists of six inverters driving six P-channel devices. The open drain feature of these buffers makes level shifting or wire AND and wire OR functions by just the addition of pull-up or pull-down resistors. All inputs are protected from static discharge by diode clamps to V_{CC} and to ground.

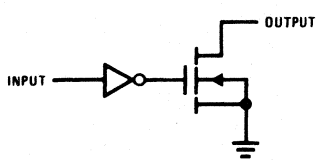
features

- Wide supply voltage range — 3.0V to 15V
- Guaranteed noise margin — 1.0V
- High noise immunity — 0.45 V_{CC} typ
- High current sourcing and sinking open drain outputs

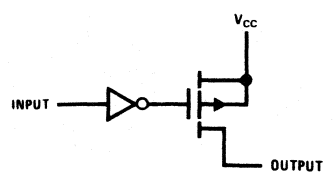
connection diagram



logic diagrams



MM54C906/MM74C906



MM54C907/MM74C907

absolute maximum ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} + 0.3V
Voltage at Any Output Pin	
MM54C906/MM74C906	−0.3V to +18V
MM54C907/MM74C907	V_{CC} − 18V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C906/MM54C907	−55°C to +125°C
MM74C906/MM74C907	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Output Open		0.05	15	μA
Output Leakage					
MM54C906	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = 18V				
MM74C906	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = 18V				
MM54C907	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−18V				
MM74C907	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}		0.005	5	μA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−18V				
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	54C, V_{CC} = 4.5V	V_{CC}−1.5			V
	74C, V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$)	54C, V_{CC} = 4.5V			0.8	V
	74C, V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE CURRENT					
MM54C906	V_{CC} = 4.5V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.5V, V_{OUT} = 0.5V	2.1	8		mA
	V_{CC} = 4.5V, V_{OUT} = 1.0V	4.2	12		mA
MM74C906	V_{CC} = 4.75V, V_{IN} = 1.0V + 0.1 V_{CC}				
	V_{CC} = 4.75V, V_{OUT} = 0.5V	2.1	8		mA
	V_{CC} = 4.75V, V_{OUT} = 1.0V	4.2	12		mA
MM54C907	V_{CC} = 4.5V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−0.5V	−1.05	−1.5		mA
	V_{CC} = 4.5V, V_{OUT} = V_{CC}−1.0V	−2.1	−3.0		mA
MM74C907	V_{CC} = 4.75V, V_{IN} = V_{CC}−1.5				
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−0.5V	−1.05	−1.5		mA
	V_{CC} = 4.75V, V_{OUT} = V_{CC}−1.0V	−2.1	−3.0		mA
MM54C906/MM74C906	V_{CC} = 10V, V_{IN} = 2.0V				
	V_{CC} = 10V, V_{OUT} = 0.5V	4.2	−20		mA
	V_{CC} = 10V, V_{OUT} = 1.0V	8.4	−30		mA
MM54C907/MM74C907	V_{CC} = 10V, V_{IN} = 8.0V				
	V_{CC} = 10V, V_{OUT} = 9.5V	−2.1	−4.0		mA
	V_{CC} = 10V, V_{OUT} = 9.0V	−4.2	−8.0		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logical "0" (t_{pd0})					
MM54C906/MM74C906	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
MM54C907/MM74C907	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V, (Note 4)			75 + 0.7 RC	ns
Propagation Delay to a Logical "1" (t_{pd1})					
MM54C906/MM74C906	V_{CC} = 5V, (Note 4)			150 + 0.7 RC	ns
	V_{CC} = 10V (Note 4)			75 + 0.7 RC	ns
MM54C907/MM74C907	V_{CC} = 5V, R = 10k			150	ns
	V_{CC} = 10V, R = 10k			75	ns
Input Capacity (C_{IN})	(Note 2)		5		pF
Output Capacity (C_{OUT})	(Note 2)		20		pF
Power Dissipation Capacity (C_{pd})	(Note 3) Per Buffer		30		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

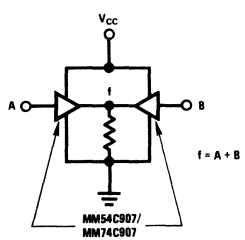
Note 2: Capacitance is guranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90. (Assumes outputs are open.)

Note 4: "C" used in calculating propagation includes output load capacity (C_L) plus device output capacity (C_{OUT}).

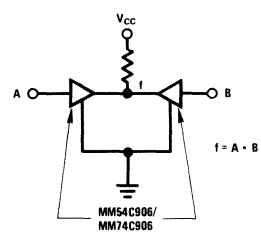
typical applications

Wire OR Gate



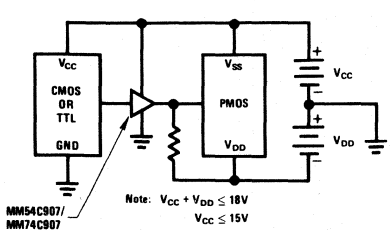
Note: Can be extended to more than 2 inputs.

Wire AND Gate

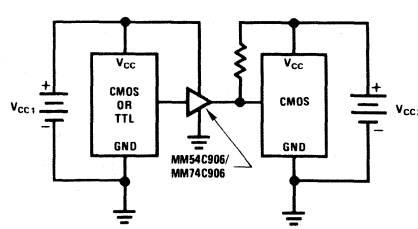


Note: Can be extended to more than 2 inputs.

CMOS or TTL to PMOS Interface



CMOS or TTL to CMOS at a Higher V_{CC}



National Semiconductor

MM74C908/MM74C918 Dual CMOS 30-Volt Driver

general description

The MM74C908 and MM74C918 are general purpose dual high voltage drivers, each capable of sourcing a minimum of 250 mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = +65°C$.

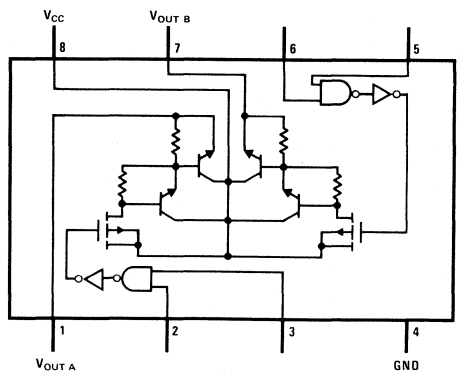
The MM74C908 and MM74C918 consist of two CMOS NAND gates driving an emitter follower darlington output to achieve high current drive and high voltage capabilities. In the "OFF" state the outputs can withstand a maximum of −30V across the device. These CMOS drivers are useful in interfacing normal CMOS voltage levels to driving relays, regulators, lamps, etc.

features

■ Wide supply voltage range	3V to 18V
■ High noise immunity	0.45 V_{CC} (typ)
■ Low output "ON" resistance	8Ω (typ)
■ High voltage	−30V
■ High current	250 mA

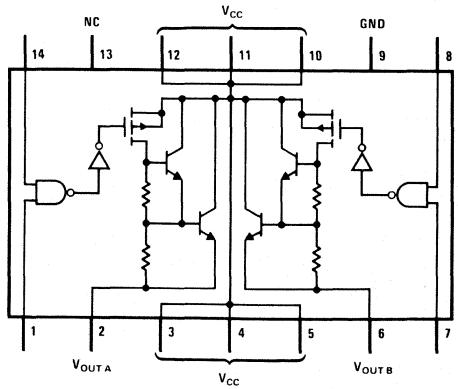
connection diagrams

MM74C908



TOP VIEW

MM74C918



TOP VIEW

absolute maximum ratings (Note 1)

Voltage at Any Input Pin	−0.3V to V_{CC} +0.3V
Voltage at Any Output Pin	32V
Operating Temperature Range	
MM74C908/MM74C918	−40°C to +85°C
Operating V_{CC} Range	3V to 18V
Absolute Maximum V_{CC}	19V
I_{SOURCE}	500 mA
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Package Dissipation	Refer to Maximum Power Dissipation vs Ambient Temperature Graph

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V V_{CC} = 10V	3.5 8			V V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V V_{CC} = 10V			1.5 2	V V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, Outputs Open Circuit		0.05	15	μA
Output "OFF" Voltage	V_{IN} = V_{CC}, I_{OUT} = −200μA		−30		V
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$) MM74C908/MM74C918	V_{CC} = 4.75V	V_{CC}−1.5			V
Logical "0" Input Voltage ($V_{IN(0)}$) MM74C908/MM74C918	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE					
Output Voltage (V_{OUT})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C I_{OUT} = −175 mA, $V_{CC} \geq$ 5V, T_j = 150°C	V_{CC}−2.7 V_{CC}−3.0 V_{CC}−3.15	V_{CC}−1.8 V_{CC}−1.9 V_{CC}−2.0		V V V
Output Resistance (R_{ON})	I_{OUT} = −300 mA, $V_{CC} \geq$ 5V, T_j = 25°C I_{OUT} = −250 mA, $V_{CC} \geq$ 5V, T_j = 65°C I_{OUT} = −175 mA, $V_{CC} \geq$ 5V, T_j = 150°C		6 7.5 10	9 12 18	Ω Ω Ω
Output Resistance Temperature Coefficient			0.55	0.80	%/°C
Thermal Resistance (θ_{jA}) MM74C908 MM74C918	 (Note 3) (Note 3)		 100 45	 110 55	 °C/W °C/W

ac electrical characteristics

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay to a Logic "1" (t_{pd1})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		150 65	300 120	ns ns
Propagation Delay to a Logic "0" (t_{pd0})	V_{CC} = 5V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C V_{CC} = 10V, R_L = 50Ω, C_L = 50 pF, T_A = 25°C		2 4	10 20	μs μs
Input Capacitance (C_{IN})	(Note 2)		5.0		pF

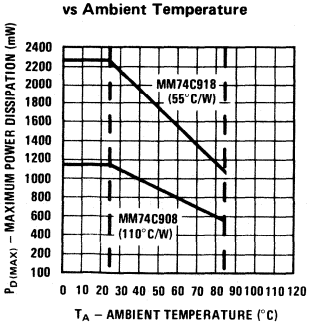
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

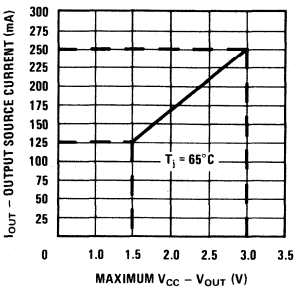
Note 3: θ_{jA} measured in free air with device soldered into printed circuit board.

typical performance characteristics

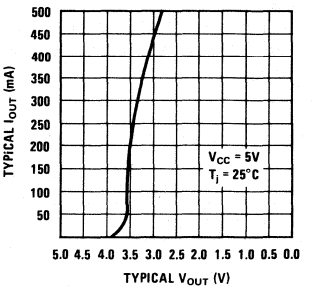
Maximum Power Dissipation vs Ambient Temperature



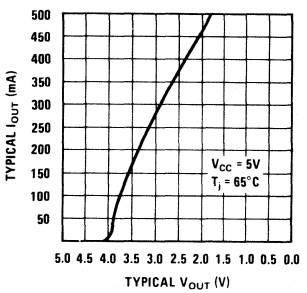
Maximum $V_{CC} - V_{OUT}$ vs I_{OUT}



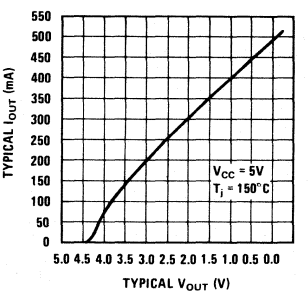
Typical I_{OUT} vs Typical V_{OUT}



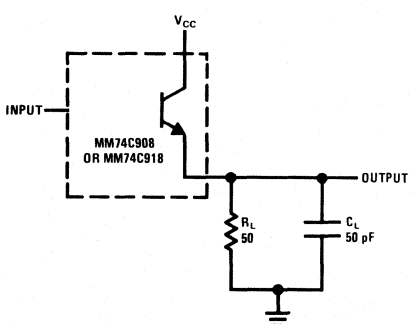
Typical I_{OUT} vs Typical V_{OUT}



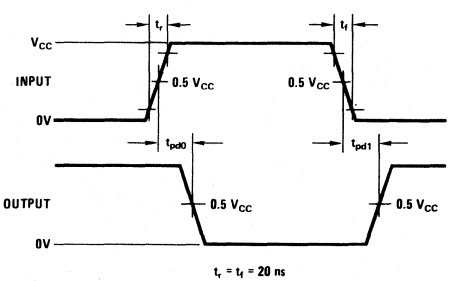
Typical I_{OUT} vs Typical V_{OUT}



ac test circuit



switching time waveforms



power considerations

Calculating Output "ON" Resistance ($R_L > 18\Omega$)

The output "ON" resistance, R_{ON}, is a function of the junction temperature, T_j, and is given by:

$$R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 \qquad (1)$$

and T_j is given by:

$$T_j = T_A + P_{DAV}\ \theta_{jA}, \qquad (2)$$

where T_A = ambient temperature, θ_{jA} = thermal resistance, and P_{DAV} is the average power dissipated within the device. P_{DAV} consists of normal CMOS power terms (due to leakage currents, internal capacitance, switching, etc.) which are insignificant when compared to the power dissipated in the outputs. Thus, the output power term defines the allowable limits of operation and includes both outputs, A and B. P_D is given by:

$$P_D = I_{OA}^2\ R_{ON} + I_{OB}^2\ R_{ON}, \qquad (3)$$

where I_O is the output current, given by:

$$I_O = \frac{V_{CC} - V_L}{R_{ON} + R_L} \qquad (4)$$

V_L is the load voltage.

The average power dissipation, P_{DAV}, is a function of the duty cycle:

$$P_{DAV} = I_{OA}^2\ R_{ON}\ (\text{Duty Cycle}_A) + I_{OB}^2\ R_{ON}\ (\text{Duty Cycle}_B) \qquad (5)$$

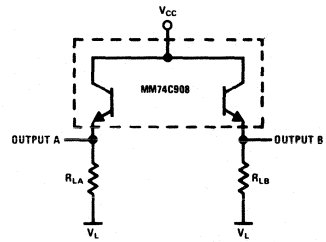
where the duty cycle is the % time in the current source state. Substituting equations (1) and (5) into (2) yields:

$$T_j = T_A + \theta_{jA}\ [9\ (T_j - 25)\ (0.008) + 9]\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)] \qquad (6a)$$

simplifying:

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]} \qquad (6b)$$

Equations (1), (4), and (6b) can be used in an iterative method to determine the output current, output resistance and junction temperature.



For example, let $V_{CC} = 15V$, $R_{LA} = 100\Omega$, $R_{LB} = 100\Omega$, $V_L = 0V$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$, Duty $\text{Cycle}_A = 50\%$, Duty $\text{Cycle}_B = 75\%$.
Assuming $R_{ON} = 11\Omega$, then:

$$I_{OA} = \frac{V_{CC} - V_L}{R_{ON} + R_{LA}} = \frac{15}{11 + 100} = 135.1\ \text{mA},$$

$$I_{OB} = \frac{V_{CC} - V_L}{R_{ON} + R_{LB}} = 135.1\ \text{mA}$$

and

$$T_j = \frac{T_A + 7.2\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}{1 - 0.072\ \theta_{jA}\ [I_{OA}^2\ (\text{Duty Cycle}_A) + I_{OB}^2\ (\text{Duty Cycle}_B)]}$$

$$T_j = \frac{25 + (7.2)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}{1 - (0.072)\ (110)\ [(0.1351)^2\ (0.5) + (0.1351)^2\ (0.75)]}$$

$T_j = 52.6°C$

and $R_{ON} = 9\ (T_j - 25)\ (0.008) + 9 =$

$9\ (52.6 - 25)\ (0.008) + 9 = 11\Omega$

applications

(See AN-177 for applications.)

National Semiconductor

MM54C909/MM74C909 Quad Comparator

general description

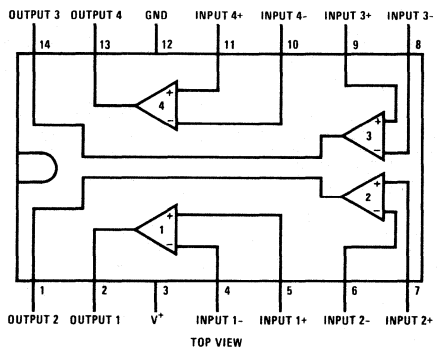
The MM54C909/MM74C909 contains four independent voltage comparators designed to operate from standard 54C/74C power supplies. The output allows current sinking only thus the wire OR function is possible using a common resistor pull up.

Not only does the MM54C909/MM74C909 function as a comparator for analog inputs but also has many applications as a voltage translator and buffer when interfacing the 54C/74C family to other logic systems.

features

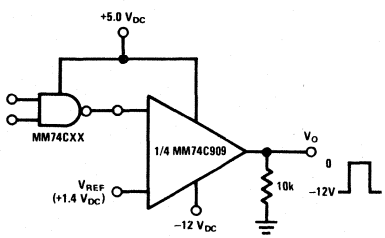
■ Wide supply voltage range	3.0V to 15V
■ TTL compatibility	fan out of 1 driving 74
■ Low power consumption	I_{CC} = 800μA typ at V_{CC} = 5.0 V_{DC}
■ Low input bias current	250 nA max
■ Low input offset current	±50 nA max
■ Low input offset voltage	±5.0 mV max
■ Large common mode input voltage range	0V to V_{CC}−1.5V
■ Large differential input voltage range	V_{CC}

connection diagram

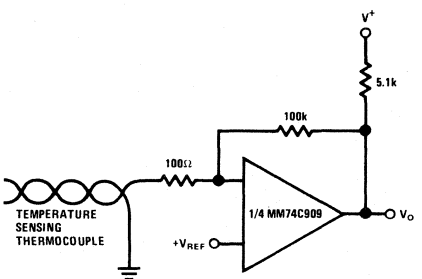


TOP VIEW

typical applications (V^+ = 5.0 V_{DC})



CMOS/TTL to MOS Logic Converter



Ground Referenced Thermocouple in Single Supply System

absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C909	−55°C to +125°C
MM74C909	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (Notes 2 and 3)	500 mW
Operating V_{CC} Range	3.0V to 15V
Absolute Maximum V_{CC}	18V
Input Current ($V_{IN} < -0.3V$) (Note 4)	50 mA
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics

Min/max limits apply across temperature range, unless otherwise noted. (V_{CC} = +5.0 V_{DC})

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 9)				±9	mV
	T_A = 25°C		±2	±5	mV
Input Bias Current ($I_{IN(+)}$ or $I_{IN(-)}$) (Note 5)	T_A = 25°C, With Output in Linear Range		25	250 400	nA nA
Input Offset Current ($I_{IN(+)} - I_{IN(-)}$)	T_A = 25°C		±5	±150 ±50	nA nA
Input Common Mode Voltage (Note 6)		0		V_{CC}−2	V
	T_A = 25°C	0		V_{CC}−1.5	V
Supply Current (I_{CC})	T_A = 25°C, R_L = ∞ On All Outputs		800	2000	μA
Voltage Gain	T_A = 25°C, $R_L \geq 15\ k\Omega$		200		V/mV
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Sink Current (I_{SINK})					
MM54C909	V_{CC} = 4.50V	1.6	3.2		mA
MM74C909	V_{CC} = 4.75V, V_{OUT} = 0.4V				
	$V_{IN(-)} \geq 1.0\ V_{DC}$ $V_{IN(+)} = 0\ V_{DC}$				
Output Leakage Current	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 15\ V_{DC}$			1	μA
	$V_{IN(+)} \geq 1.0\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V_{OUT} = 5\ V_{DC}$, T_A = 25°C		0.1		nA
Differential Input Voltage (Note 8)	All V_{IN}'s $\geq 0\ V_{DC}$			15	V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: For operating at high temperatures, the MM74C909 must be derated based on +125°C maximum junction temperature and a thermal resistance of +175°C/W which applies to the device soldered in a printed circuit board, operating in a still air ambient. The MM54C909 must be derated based on a +150°C maximum junction temperature. The low bias dissipation and the ON-OFF characteristic of the outputs keeps the chip dissipation very small (Pd ≤ 100 mW), provided the output sink current is within specified limits.

Note 3: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 4: This input current will only exist when the voltage at any of the input leads is driven negative. There is a lateral NPN parasitic transistor action on the IC chip. The transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will reestablish when the input voltage, which was negative, again returns to a value greater than −0.3V.

Note 5: The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to +15V without damage.

Note 7: The response time specified is for a 100 mV input step with 5.0 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

Note 8: The positive excursions of the input can equal V_{CC} supply voltage level, and if the other input voltage remains within the common-mode voltage range, the comparator will provide a proper output state. The low input voltage state must not be less than −0.3V.

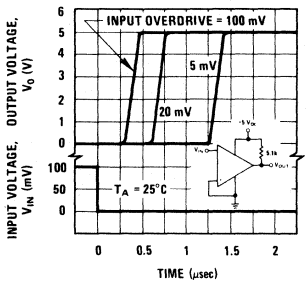
Note 9: At output switch point, V_O = 1.4 V_{DC}, R_S = 0Ω with V^+ from 5 V_{DC} to 30 V_{DC} and over the full input common mode range (0V_{DC}) to V^+ ±1.5 V_{DC}).

ac electrical characteristics R_L = 5.1 kΩ, V_{RL} = 5.0 V_{DC}, unless otherwise specified.

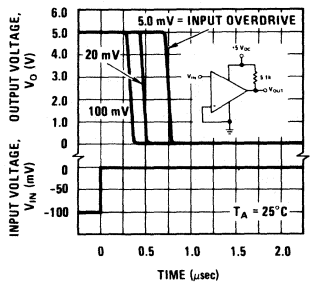
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Large Signal Response Time	V_{IN} = TTL Swing V_{REF} = 1.4 V_{DC}		300		ns
Response Time	T_A = 25°C		1.3		μs

typical performance characteristics

Response Time for Various Input Overdrives — Positive Transition



Response Time for Various Input Overdrives — Negative Transition



application hints

The MM54C909/MM74C909 is a high gain, wide bandwidth device; which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to <10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the I/C and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

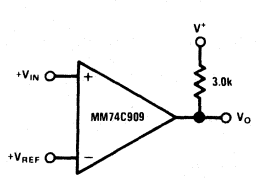
The bias network of the MM54C909/MM74C909 establishes an I_{CC} current which is independent of the magnitude of the power supply voltage over the range of from 3.0V to 15V

It is usually unnecessary to use a bypass capacitor across the power supply line.

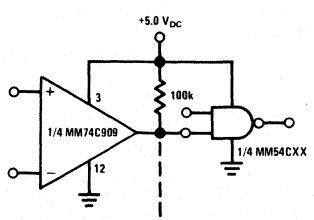
The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode and input resistor can be used as shown in the applications section.

Many outputs can be tied together to provide an output OR'ing function. An output "pull-up" resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the MM54C909/MM74C909 package. The output can also be used as a simple SPST switch to ground (when a "pull-up" resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the gain of the output device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly.

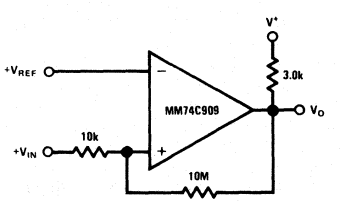
typical applications (con't) (V^+ = 5.0 V_{DC})



Basic Comparator

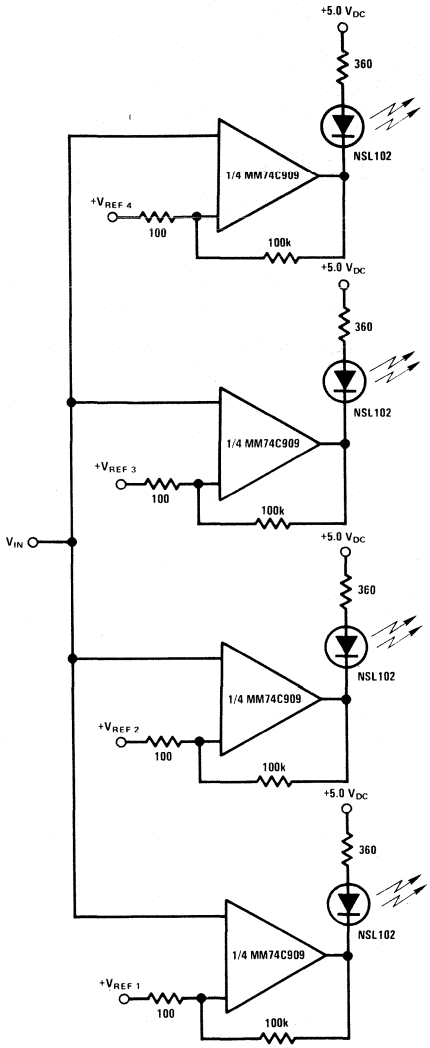


Driving CMOS

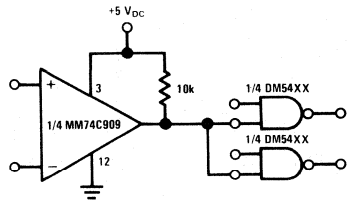


Non-Inverting Comparator with Hysteresis

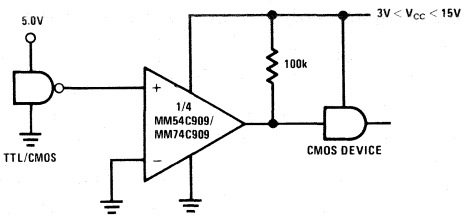
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



Visible Voltage Indicator

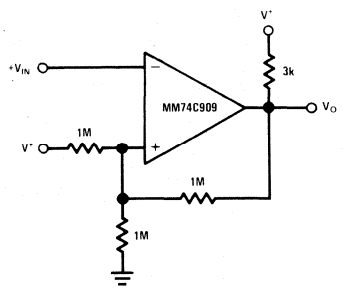


Driving TTL

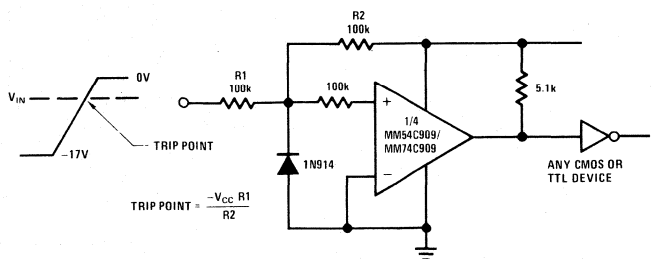


Note: For inverting buffer reverse input connection.

5V Logic to CMOS Operating at $V_{CC} \neq 5V$



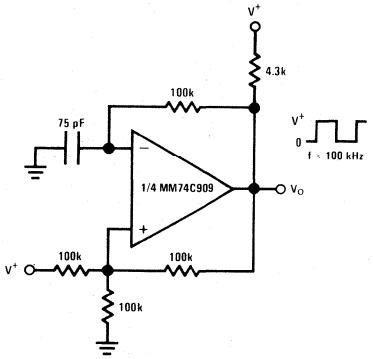
Inverting Comparator with Hysteresis



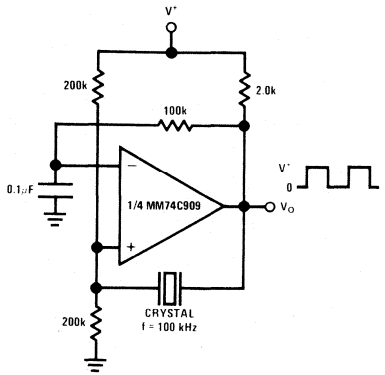
Note: For non-inverting buffer reverse input connection.

Hi Voltage Inverting PMOS to CMOS or TTL

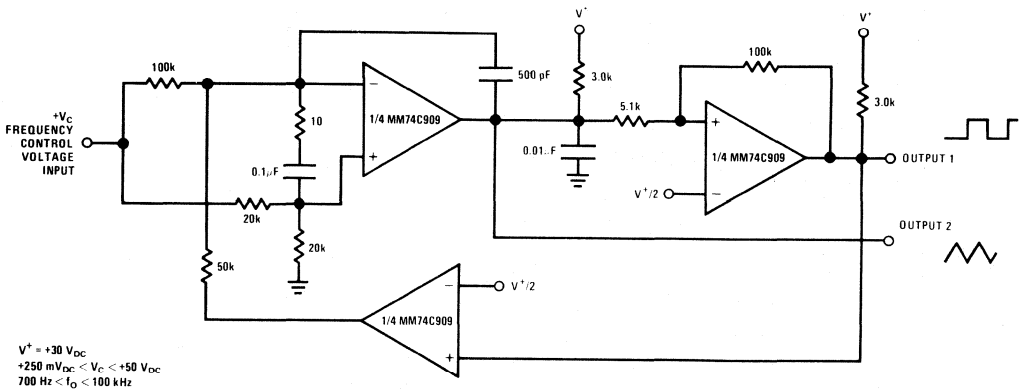
typical applications (con't) ($V^+ = 5.0\ V_{DC}$)



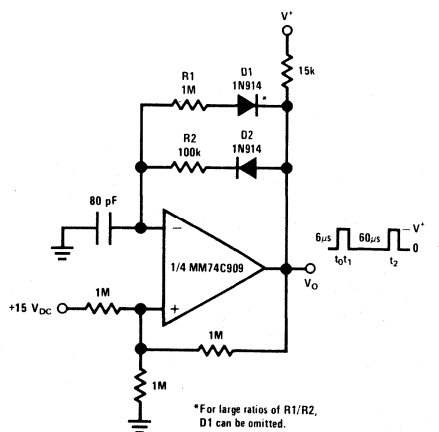
Squarewave Oscillator



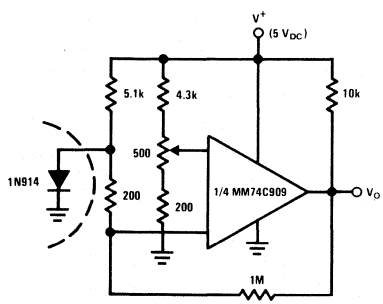
Crystal Controlled Oscillator



Two-Decade High-Frequency VCO



Pulse Generator



Remote Temperature Sensing

National Semiconductor

MM54C910/MM74C910 256-Bit TRI-STATE® Random Access Read/Write Memory

general description

The MM54C910/MM74C910 is a 64 word by 4 bit random access memory. Inputs consist of six address lines, four data input lines, a write enable, and a memory enable line. The six address lines are internally decoded to select one of 64 word locations. An internal address register, latches the address information on the positive to negative transition of memory enable. The TRI-STATE outputs allow for easy memory expansion.

Address Operation: Address inputs must be stable (t_{SA}) prior to the positive to negative transition of memory enable, and (t_{HA}) after the positive to negative transition of memory enable. The address register holds the information and stable address inputs are not needed at any other time.

Write Operation: Data is written into memory at the selected address if write enable goes low while memory enable is low. Write enable must be held low for $t_{\overline{WE}}$ and data must remain stable t_{HD} after write enable returns high.

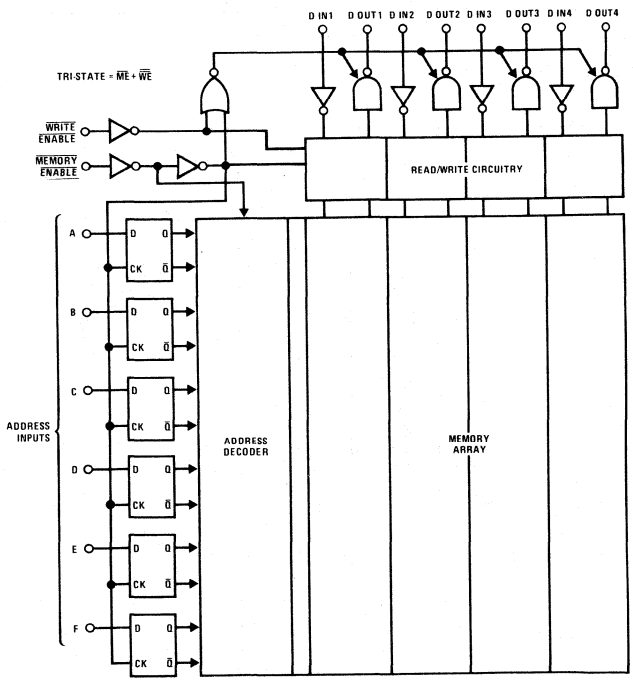
Read Operation: Data is nondestructively read from a memory location by an address operation with write enable held high.

Outputs are in the TRI-STATE (Hi-Z) condition when the device is writing or disabled.

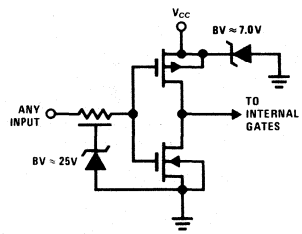
features

- Supply voltage range — 3V to 5.5V
- High noise immunity — 0.45 V_{CC} typ
- TTL compatible fan out — 1 TTL load
- Input address register
- Low power consumption — 250 nW/package typ (chip enabled or disabled)
- Fast access time — 250 ns typ at 5V
- TRI-STATE outputs
- High voltage inputs

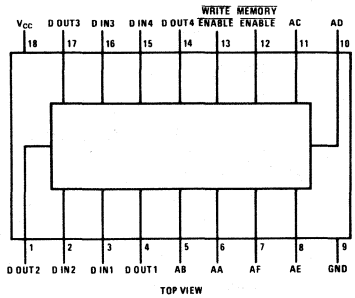
logic and connection diagrams



Input Protection



Dual-In-Line Package



absolute maximum ratings (Note 1)

Voltage At Any Output Pin	−0.3V to V_{CC} +0.3V
Voltage At Any Input Pin	−0.3V to +15V
Package Dissipation	500 mW
Operating V_{CC} Range	3.0V to 5.5V
Standby V_{CC} Range	1.5V to 5.5V
Absolute Maximum V_{CC}	6.0V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C910	4.5	5.5	V
MM74C910	4.75	5.25	V
Temperature (T_A)			
MM54C910	−55	+125	°C
MM74C910	−40	+85	°C

dc electrical characteristics MM54C910/MM74C910

(Min/max limits apply across the temperature and power supply range indicated).

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	Full Range	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	Full Range			0.8	V
$I_{IN(1)}$	Logical "1" Input Current	V_{IN} = 15V		0.005	2	μA
		V_{IN} = 5V		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{IN} = 0V	−1	−0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −150μA	V_{CC}−0.5			V
		I_O = −400μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
	Output Current in High	V_O = 5V		0.005	1	μA
	Impedence State	V_O = 0V	−1	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V		0.05	300	μA

ac electrical characteristics MM54C910/MM74C910

T_A = 25°C, V_{CC} = 5V, C_L = 50 pF

	PARAMETER	MIN	TYP	MAX	UNITS
t_{ACC}	Access Time from Address		250	500	ns
t_{PD}	Propagation Delay from $\overline{ME}$		180	360	ns
t_{SA}	Address Input Set-Up Time	140	70		ns
t_{HA}	Address Input Hold Time	20	10		ns
t_{ME}	$\overline{\text{Memory Enable}}$ Pulse Width	200	100		ns
$t_{\overline{ME}}$	$\overline{\text{Memory Enable}}$ Pulse Width	400	200		ns
t_{SD}	Data Input Set-Up Time	0			ns
t_{HD}	Data Input Hold Time	30	15		ns
$t_{\overline{WE}}$	$\overline{\text{Write Enable}}$ Pulse Width	140	70		ns
t_{1H}, t_{OH}	Delay to TRI-STATE (Note 4)		100	200	ns
	CAPACITANCE				
C_{IN}	Input Capacity				
	Any Input (Note 2)		5		pF
C_{OUT}	Output Capacity				
	Any Output (Note 2)		9		pF
C_{PD}	Power Dissipation Capacity (Note 3)		350		pF

ac electrical characteristics (con't)

C_L = 50 pF

PARAMETER		MM54C910 T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V		MM74C910 T_A = −40°C to +85°C V_{CC} = 4.75V to 5.25V		UNITS
		MIN	MAX	MIN	MAX	
t_{ACC}	Access Time from Address		860		700	ns
t_{PD1}, t_{PD0}	Propagation Delay from $\overline{ME}$		660		540	ns
t_{SA}	Address Input Set-Up Time	200		160		ns
t_{HA}	Address Input Hold Time	20		20		ns
t_{ME}	$\overline{Memory\ Enable}$ Pulse Width	280		260		ns
$t_{\overline{ME}}$	$\overline{Memory\ Enable}$ Pulse Width	750		600		ns
t_{SD}	Data Input Set-Up Time	0		0		ns
t_{HD}	Data Input Hold Time	50		50		ns
$t_{\overline{WE}}$	$\overline{Write\ Enable}$ Pulse Width	200		180		ns
t_{1H}, t_{0H}	Delay to TRI-STATE (Note 4)		200		200	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

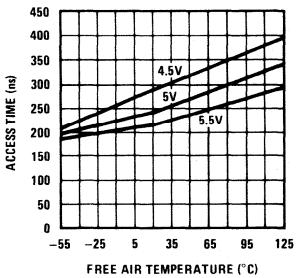
Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{pd} determines the no load ac power consumption for any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

Note 4: See ac test circuit for t_{1H}, t_{0H}.

typical performance characteristics

Typical Access Time vs Ambient Temperature

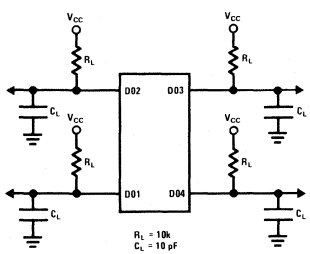


truth table

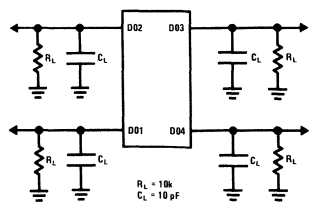
$\overline{ME}$	$\overline{WE}$	OPERATION	OUTPUTS
L	L	Write	TRI-STATE
L	H	Read	Data
H	L	Inhibit, Store	TRI-STATE
H	H	Inhibit, Store	TRI-STATE

ac test circuits

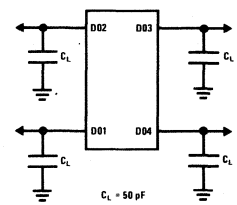
t_{0H}



t_{1H}

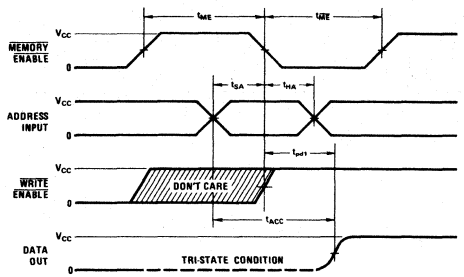


All Other AC Tests

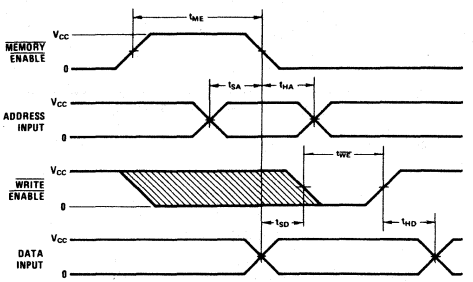


switching time waveforms

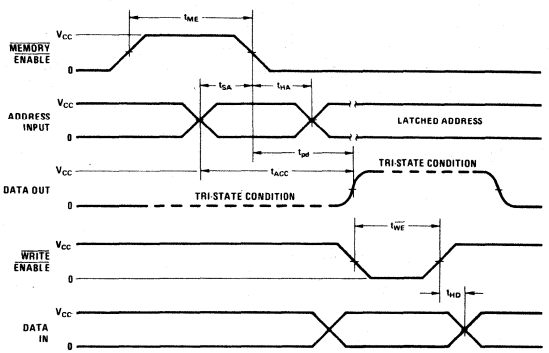
Read Cycle
(See Note 1)



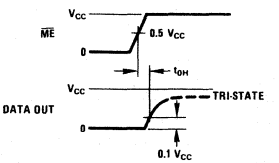
Write Cycle
(See Note 1)



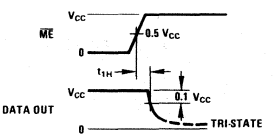
Read Modify Write Cycle
(See Note 1)



t_{0H}



t_{1H}



Note 1: MEMORY ENABLE must be brought high for t_{ME} nanoseconds between every address change.
Note 2: $t_r = t_f = 20$ ns for all inputs.

National Semiconductor

MM74C911 4-Digit Expandable Segment Display Controller

General Description

The MM74C911 display controller is an interface element with memory that directly drives a 4-digit, 8-segment LED display. The MM74C911 allows individual control of any segment in the 4-digit display. The number of segments per digit can be expanded without any external components. For example, 2 MM74C911's can be cascaded to drive a 16-segment alpha-numeric display.

The display controllers receive data information through 8 data lines a, b . . . DP, and digit information through 2 address inputs K1 and K2. The input data is written into the register selected by the address information when Chip Enable, $\overline{CE}$, and Write Enable, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required.

A self-contained internal oscillator sequentially presents the stored data to high drive (100 mA typ) TRI-STATABLE output drivers which directly drive the LED display. The drivers are active when the control pin labeled Segment Output Enable, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control, or for disabling the output drive for power conservation.

The digit outputs directly drive the base of the digit transistor when the control pin labeled Digit Input Output, $\overline{DIO}$, is low. When $\overline{DIO}$ is high, the digit lines turn into inputs and the internal scanning multiplexer is disabled.

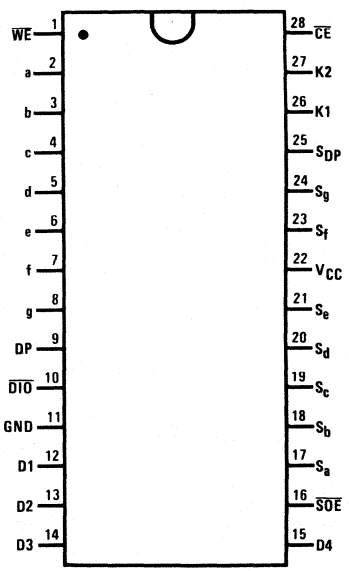
When any digit line is forced high by an external device, usually another MM74C911, the data information for that digit is presented to the output. In this manner, 16-segment alpha-numeric displays, 24 or 32-segment displays, or an array of discrete LED's can be controlled by the simple cascading of expandable segment display controllers. All inputs except digit inputs are TTL compatible and do not clamp input voltages above V_{CC}.

Features

- Direct segment drive (100 mA typ) TRI-STATABLE
- 4 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor
- Segment expandability without external components
- TTL compatible inputs
- Power saver mode—5 μW typical

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS		$\overline{WE}$	OPERATION
	K2	K1		
0	0	0	0	Write digit 1
0	0	0	1	Latch digit 1
0	0	1	0	Write digit 2
0	0	1	1	Latch digit 2
0	1	0	0	Write digit 3
0	1	0	1	Latch digit 3
0	1	1	0	Write digit 4
0	1	1	1	Latch digit 4
1	X	X	X	Disable writing

Output Control

$\overline{DOE}$	$\overline{SOE}$	DIGIT LINES				OPERATION
		D4	D3	D2	D1	
0	0	R	R	R	R	Refresh display
0	1	R	R	R	R	Disable segment outputs
1	0	0	0	0	0	Digits are now inputs
1	0	0	0	0	1	Display digit 1
1	0	0	0	1	0	Display digit 2
1	0	0	1	0	0	Display digit 3
1	0	1	0	0	0	Display digit 4
1	1	0	0	0	0	Power saver mode

R = Refresh (digit lines sequentially pulsed)
X = Don't care

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	$-0.3V$ to $V_{CC} + 0.3V$
Voltage at Any Input Except Digits	$-0.3V$ to $+15V$
Operating Temperature Range, T_A	$-40°C$ to $+85°C$
Storage Temperature Range	$-65°C$ to $+150°C$
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	$300°C$

DC Electrical Characteristics Min/max limits apply at $-40°C \leq T_J \leq +85°C$, unless otherwise noted

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 5V$	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{CC} = 5V$, $V_{IN} = 15V$		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{CC} = 5V$, $V_{IN} = 0V$	-1.0	-0.005		μA
I_{CC}	Supply Current (Normal)	$V_{CC} = 5V$, Outputs Open		0.50	2.5	mA
I_{CC}	Supply Current (Power Saver)	$V_{CC} = 5V$, $\overline{SOE}$, $\overline{DIO}$ = "1", D1, D2, D3, D4 = "0"		1	600	μA
I_{OUT}	TRI-STATE Output Current	$V_O = 5V$		0.03	3	μA
		$V_O = 0V$	-3	-0.03		
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC} = 4.75V$	$V_{CC}-2.0$			V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC} = 4.75V$			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	$V_{CC} = 5V$, $V_O = 3.4V$				
		$T_J = 25°C$	-60	-100		mA
		$T_J = 100°C$	-40	-60		mA
I_{DH}	High Level Digit Current	$V_{CC} = 5V$, $V_O = 3V$				
		$T_J = 25°C$	-10	-20		mA
		$T_J = 100°C$	-7	-10		mA
		$V_{CC} = 5V$, $V_O = 1V$				
		$T_J = 25°C$	-15	-40		mA
		$T_J = 100°C$	-10	-15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage, Any Digit	$V_{CC} = 5V$, $I_O = -360\ \mu A$	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage, Any Output	$V_{CC} = 5V$, $I_O = 360\ \mu A$			0.4	V
θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range", they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltage reference to ground.

Note 3: θ_{JA} measured in free-air with device soldered into printed circuit board.

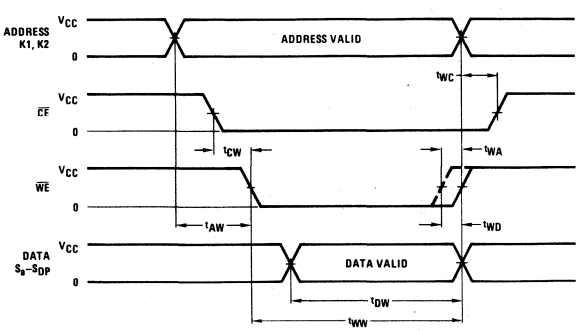
AC Electrical Characteristics V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable Set-Up Time	T_J = 25°C	35	15		ns
		T_J = 125°C	50	20		ns
t_{AW}	Address to Write Enable Set-Up Time	T_J = 25°C	35	15		ns
		T_J = 125°C	50	20		ns
t_{WW}	Write Enable Width	T_J = 25°C	400	225		ns
		T_J = 125°C	450	250		ns
t_{DW}	Data to Write Enable Set-Up Time	T_J = 25°C	390	225		ns
		T_J = 125°C	430	250		ns
t_{WD}	Write Enable to Data Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	T_J = 25°C	0	−10		ns
		T_J = 125°C	0	−15		ns
t_{WC}	Write Enable to Chip Enable Hold Time	T_J = 25°C	55	30		ns
		T_J = 125°C	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels into TRI-STATE	R_L = 10k, C_L = 10 pF				
		T_J = 25°C		275	500	ns
		T_J = 125°C		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" or Logical "0" Levels	R_L = 10k, C_L = 50 pF				
		T_J = 25°C		325	600	ns
		T_J = 125°C		375	700	ns
t_{D1}, t_{D0}	Propagation Delay From Digit Input to Segment Output	T_J = 25°C		500	1000	ns
		T_J = 125°C		700	1400	ns
t_{IB}	Interdigit Blanking Time	T_J = 25°C	5	10		μs
		T_J = 125°C	10	20		μs
f_{MUX}	Multiplex Scan Frequency	T_J = 25°C		525		Hz
		T_J = 125°C		375		Hz
C_{IN}	Input Capacitance	(Note 4)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 4)		30	50	pF

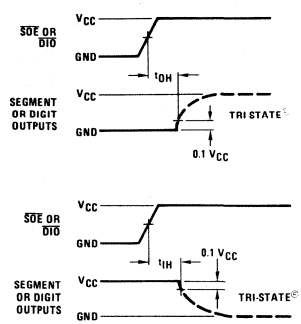
Note 4: Capacitance guaranteed by periodic testing.

Switching Time Waveforms

Write Data Waveforms

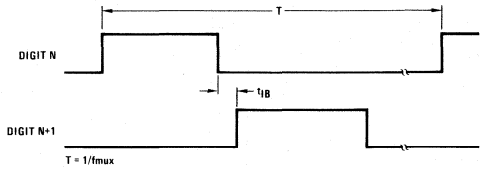


TRI-STATE Waveforms

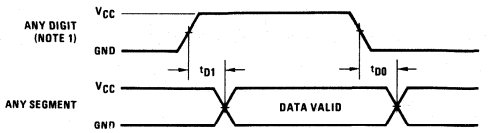


Switching Time Waveforms (Continued)

Multiplexing Output Waveforms



Read Data Waveforms



Note 1: All other digit lines are at a low level. $\overline{DIO}$ at a high level.

Functional Description

The MM74C911 display controller is manufactured on standard metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin to suppress current transients.

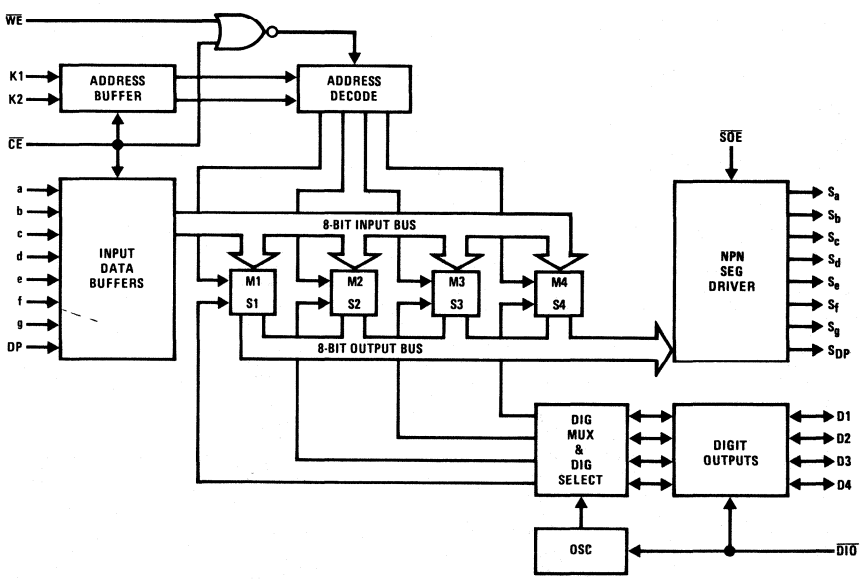
The digit outputs directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration. If an MM74C911 is driving a digit transistor and also supplying digit information to a cascaded MM74C911, base resistors are needed in the digit transistors to provide an adequate high level to the digit inputs of the cascaded MM74C911.

As seen in the block diagram, these display controllers contain four 8-bit registers; any one may be randomly written into. In normal operation, the internal multiplexer scans the registers and refreshes the display. In cascaded operation, 1 MM74C911 serves as a master refresh device and cascaded MM74C911's are slaved to it through digit lines operating as inputs.

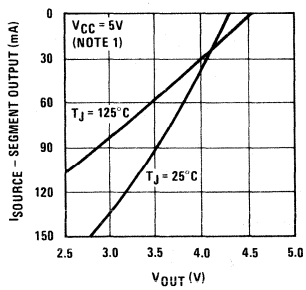
The MM74C911 appears to a microprocessor as memory and to the user as a self-scan display. Since every segment is under microprocessor control, great versatility is obtained.

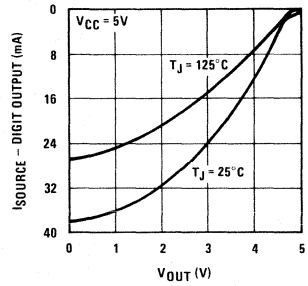
Low power standby operation occurs with both $\overline{SOE}$ and $\overline{DIO}$ inputs high. This condition forces the MM74C911 to a quiescent state typically drawing less than 1 μA of supply current with a standby supply voltage as low as 3V.

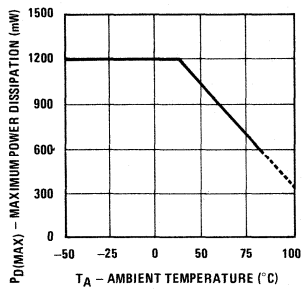
Block Diagram

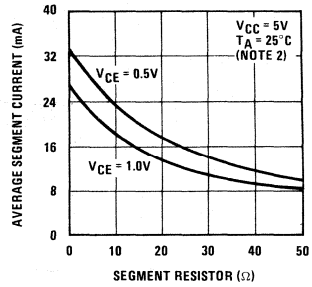


Typical Performance Characteristics





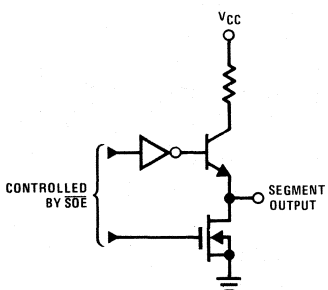




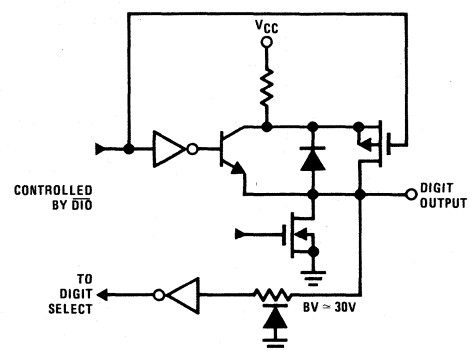
Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.
Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

Applications

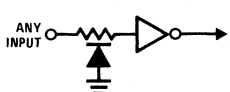
Segment Output Structure



Digit Output Structure

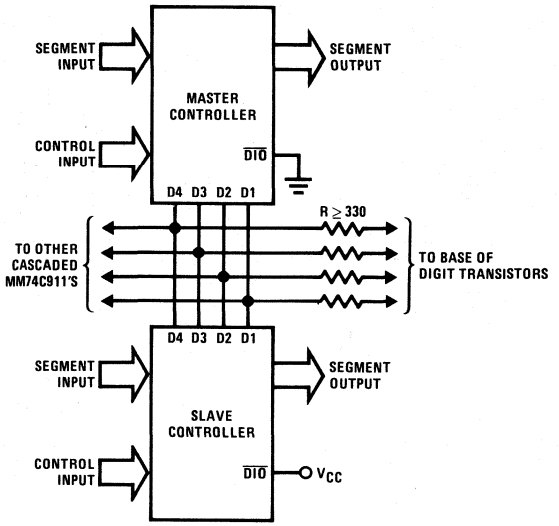


Input Protection

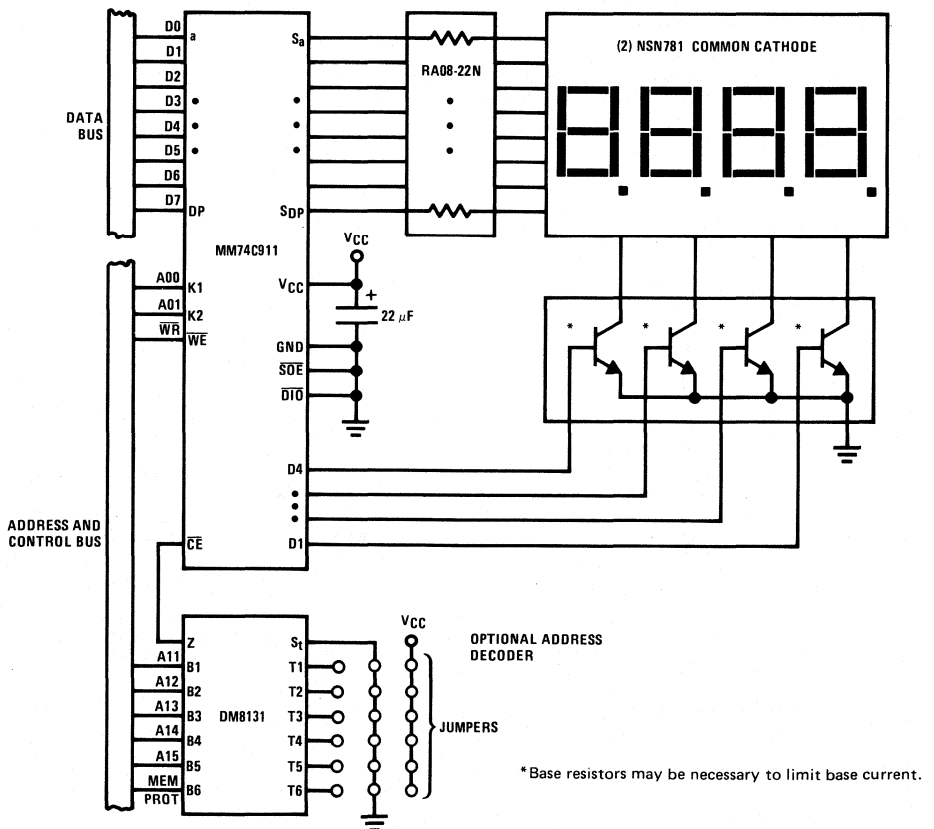


Applications (Continued)

Segment Expansion



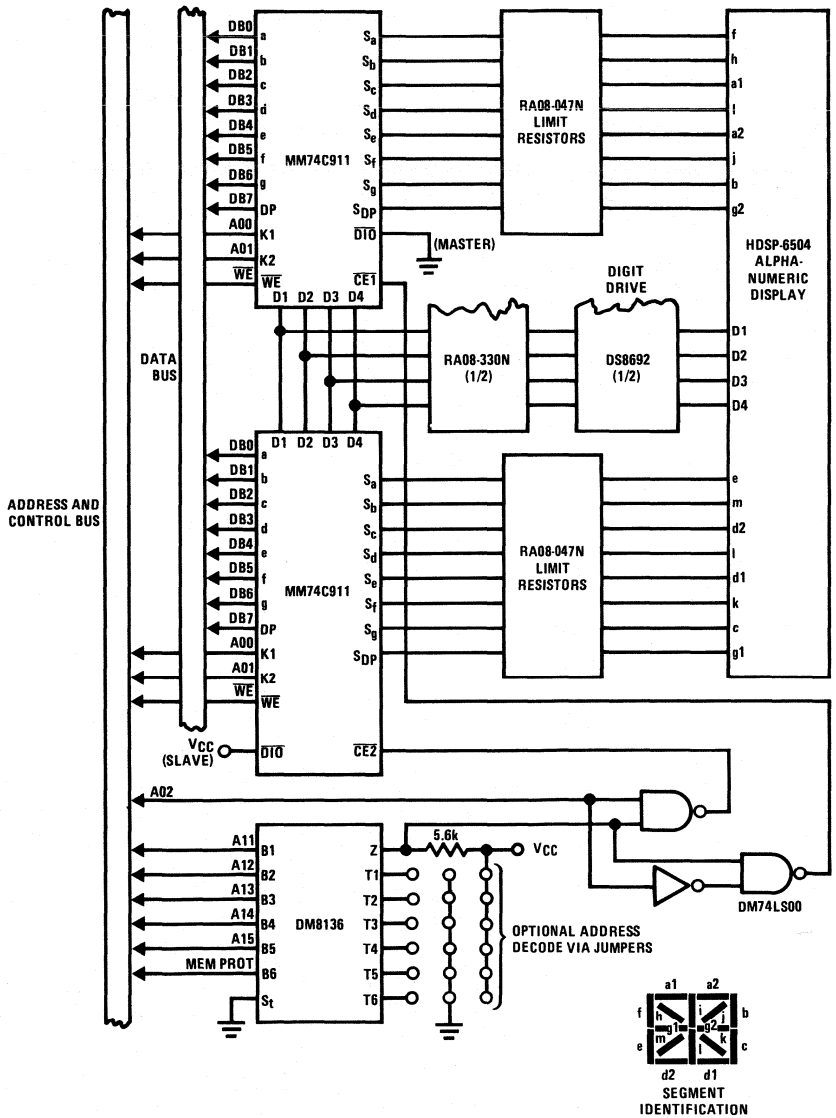
Typical Application



*Base resistors may be necessary to limit base current.

Applications (Continued)

4-Digit, 16-Segment Alpha-Numeric Display



National Semiconductor

MM74C912 6-Digit BCD Display Controller/Driver
MM74C917 6-Digit Hex Display Controller/Driver

General Description

The MM74C912, MM74C917 display controllers are interface elements, with memory, that directly drive a 6-digit, 8-segment LED display.

The display controllers receive data information through 5 data inputs A, B, C, D and DP, and digit information through 3 address inputs K1, K2 and K3.

The input data is written into the register selected by the address information when CHIP ENABLE, $\overline{CE}$, and WRITE ENABLE, $\overline{WE}$, are low and is latched when either $\overline{CE}$ or $\overline{WE}$ return high. Data hold time is not required. A self-contained internal oscillator sequentially presents the stored data to a decoder where 4 data bits control the format of the displayed character and 1 bit controls the decimal point. The internal oscillator is controlled by a control input labeled OSCILLATOR ENABLE, $\overline{OSE}$, which is tied low in normal operation. A high level at $\overline{OSE}$ prevents automatic refresh of the display.

The 7-segment plus decimal point output information directly drives a LED display through high drive (100 mA typ) output drivers. The drivers are active when the control pin labeled SEGMENT OUTPUT ENABLE, $\overline{SOE}$, is low and go into TRI-STATE® when $\overline{SOE}$ is high. This feature allows for duty cycle brightness control and for disabling the output drivers for power conservation.

The MM74C912 segment decoder converts BCD data into 7-segment format. The MM74C917 converts binary data into hex format.

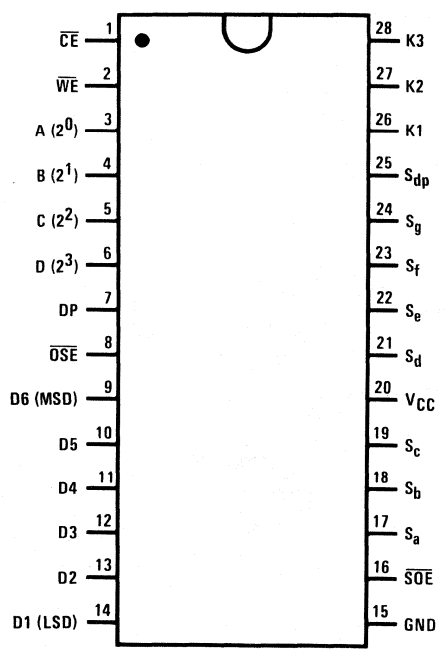
All inputs are TTL compatible and do not clamp to the V_{CC} supply.

Features

- Direct segment drive (100 mA typ) TRI-STATEABLE
- 6 registers addressed like RAM
- Internal oscillator and scanning circuit
- Direct base drive to digit transistor (20 mA typ)
- Internal segment decoder
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TOP VIEW

Truth Tables

Input Control

$\overline{CE}$	DIGIT ADDRESS			$\overline{WE}$	OPERATION
	K3	K2	K1		
0	0	0	0	0	Write Digit 1
0	0	0	0	1	Latch Digit 1
0	0	0	1	0	Write Digit 2
0	0	0	1	1	Latch Digit 2
0	0	1	0	0	Write Digit 3
0	0	1	0	1	Latch Digit 3
0	0	1	1	0	Write Digit 4
0	0	1	1	1	Latch Digit 4
0	1	0	0	0	Write Digit 5
0	1	0	0	1	Latch Digit 5
0	1	0	1	0	Write Digit 6
0	1	0	1	1	Latch Digit 6
0	1	1	0	0	Write Null Digit
0	1	1	0	1	Latch Null Digit
0	1	1	1	0	Write Null Digit
0	1	1	1	1	Latch Null Digit
1	X	X	X	X	Disable Writing

X = don't care

Output Control

$\overline{SOE}$	$\overline{OSE}$	OPERATION
0	0	Refresh Display
0	1	Stop Oscillator*
1	0	Disable Segment Outputs
1	1	Standby Mode

*Segment drive may exceed maximum display dissipation.

Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Inputs	−0.3V to V_{CC}+0.3V	Package Dissipation	Refer to P_D MAX vs T_A Graph
Voltage at Any Input	−0.3V to +15V	Operating V_{CC} Range	3V to 6V
Operating Temperature Range (T_A)	−40°C to +85°C	Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C	Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics Min/max limits apply at 40°C ≤ T_J ≤ 85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5V, Outputs Open		0.5	2	mA
I_{OUT}	TRI-STATE Output Current	V_{CC} = 5V, V_O = 5V		0.03	3	μA
		V_{CC} = 5V, V_O = 0V	−3	−0.03		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−2.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
OUTPUT DRIVE						
I_{SH}	High Level Segment Current	V_{CC} = 5V, V_O = 3.4V,				mA
		T_J = 25°C	−60	−100		
		T_J = 100°C	−40	−60		mA
I_{DH}	High Level Digit Current	V_{CC} = 5V, V_O = 1V,				
		T_J = 25°C	−10	−20		mA
		T_J = 100°C	−7	−15		mA
$V_{OUT(1)}$	Logical "1" Output Voltage Any Digit	V_{CC} = 5V, I_O = −360 μA	4.6			V
$V_{OUT(0)}$	Logical "0" Output Voltage Any Output	V_{CC} = 5V, I_O = 360 μA			0.4	V
Θ_{JA}	Thermal Resistance	(Note 3)		100		°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages reference to ground.

Note 3: Θ_{JA} measured in free air with device soldered into printed circuit board.

AC Electrical Characteristics V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

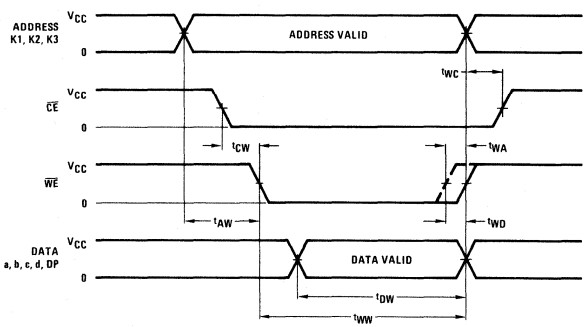
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{CW}	Chip Enable to Write Enable	T_J = 25°C	35	15		ns
	Setup Time	T_J = 125°C	50	20		ns
t_{AW}	Address to Write Enable	T_J = 25°C	35	15		ns
	Setup Time	T_J = 125°C	50	20		ns
t_{WW}	Write Enable Width	T_J = 25°C	400	225		ns
		T_J = 125°C	450	250		ns

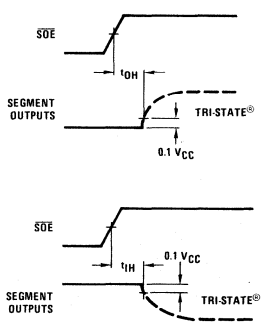
AC Electrical Characteristics (Continued) V_{CC} = 5V, $t_r = t_f$ = 20 ns, C_L = 50 pF

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{DW}	Data to Write Enable Setup Time	$T_J = 25°C$	390	225		ns
		$T_J = 125°C$	430	250		ns
t_{WD}	Write Enable to Data Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WA}	Write Enable to Address Hold Time	$T_J = 25°C$	0	−10		ns
		$T_J = 125°C$	0	−15		ns
t_{WC}	Write Enable to Chip Enable	$T_J = 25°C$	50	30		ns
	Hold Time	$T_J = 125°C$	75	40		ns
t_{1H}, t_{0H}	Logical "1", Logical "0" Levels	R_L = 10k, $T_J = 25°C$		275	500	ns
	Into TRI-STATE	C_L = 10 pF, $T_J = 125°C$		325	600	ns
t_{H1}, t_{H0}	TRI-STATE to Logical "1" to	R_L = 10k, $T_J = 25°C$		325	600	ns
	Logical "0" Level	C_L = 50 pF, $T_J = 125°C$		375	700	ns
t_{IB}	Interdigit Blanking Time	$T_J = 25°C$	5	10		μs
		$T_J = 125°C$	10	20		μs
f_{MUX}	Multiplex Scan Frequency	$T_J = 25°C$		350		Hz
		$T_J = 125°C$		250		Hz
C_{IN}	Input Capacitance	Note 4		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Note 4		30	50	pF

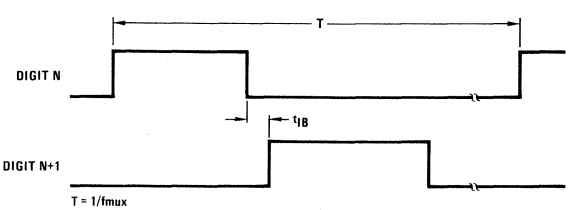
Note 4: Capacitance is guranteed by periodic testing.

Switching Time Waveforms





Multiplexing Output Waveforms

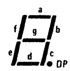


Functional Description

Character Font

MM74C917	Hi-Z	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F	F.
MM74C912	Hi-Z	0	1	2	3	4	5	6	7	8	9	o	°	‾	-	_		.
Input A 2^0	X	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1
Data B 2^1	X	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	1
C 2^2	X	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	1
D 2^3	X	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1
DP	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Output Enable $\overline{SOE}$	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Segment Identification

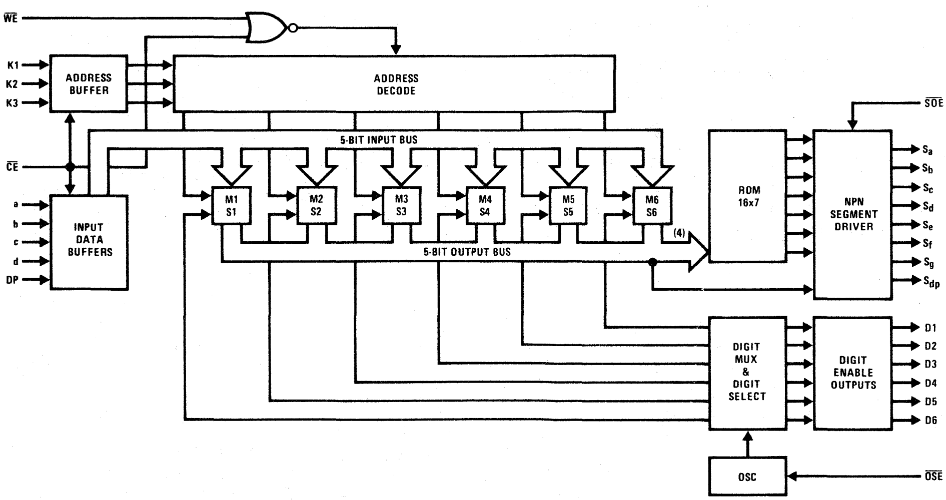


The MM74C912, MM74C917 display controllers are manufactured using metal gate CMOS technology. A single 5V 74 series TTL supply can be used for power and should be bypassed at the V_{CC} pin.

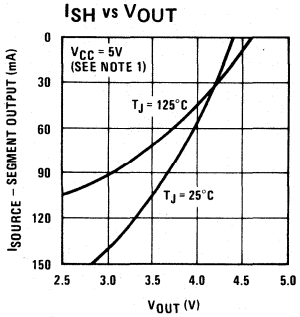
All inputs are TTL compatible; the segment outputs drive the LED display directly through current limiting resistors. The digit outputs are designed to directly drive the base of a grounded emitter digit transistor without the need of a Darlington configuration.

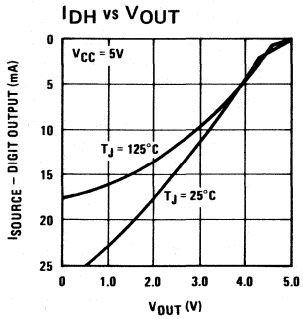
As seen in the block diagram, these display controllers contain six 5-bit registers; any one of which may be randomly written. The internal multiplexer scans the registers and refreshes the display. This combination of write only memory and self-scan display makes the display controller a "refreshing experience" for an over-burdened microprocessor.

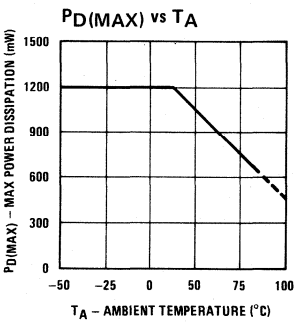
Block Diagram

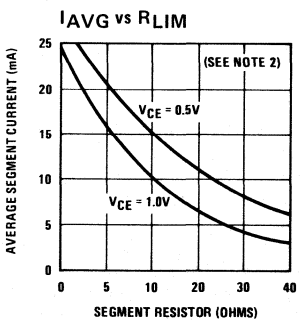


Typical Performance Characteristics







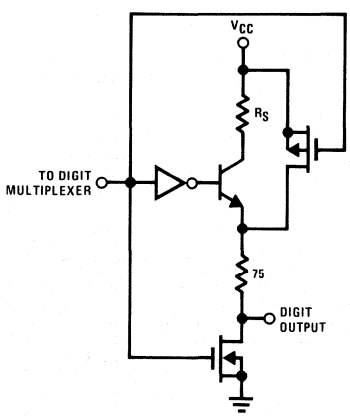


Note 1: Segment outputs if shorted to ground will exceed maximum power dissipation of the device.

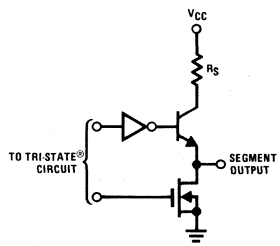
Note 2: V_{CE} is the saturation voltage of the digit drive transistor.

Applications

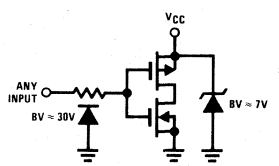
Digit Output Structure



Segment Output Structure



Input Protection



National Semiconductor

MM54C914/MM74C914 Hex Schmitt Trigger with Extended Input Voltage

general description

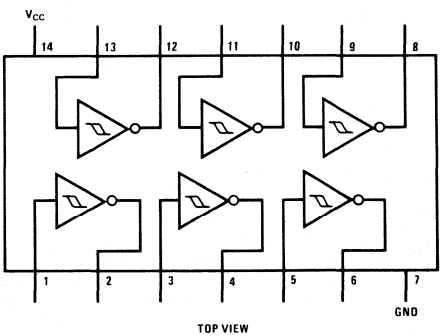
The MM54C914/MM74C914 is a monolithic CMOS Hex Schmitt trigger with special input protection scheme. This scheme allows the input voltage levels to exceed V_{CC} or ground by at least 10V (V_{CC} – 25V to GND + 25V), and is valuable for applications involving voltage level shifting or mismatched power supplies.

The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{CC} = 10V). And the hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{CC}$ is guaranteed.

features

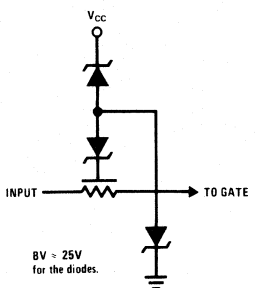
■ Hysteresis	0.4 V_{CC} typ 0.2 V_{CC} guaranteed
■ Special input protection	Extended Input Voltage Range
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.70 V_{CC} typ
■ Low power TTL compatibility	fan out of 2 driving 74L

connection diagram



TOP VIEW

Special Input Protection



absolute maximum ratings

Voltage at Any Input Pin	V_{CC} − 25V to GND + 25V	Storage Temperature Range	−65°C to +150°C
Voltage at Any Other Pin	−0.3V to V_{CC} +0.3V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3.0V to 15V
MM54C914	−55°C to +125°C	Absolute Maximum V_{CC}	18V
MM74C914	−40°C to +85°C	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
V_{T+} Positive Going Threshold Voltage	V_{CC} = 5V	3.0	3.6	4.3	V
	V_{CC} = 10V	6.0	6.8	8.6	V
	V_{CC} = 15V	9.0	10.0	12.9	
V_{T-} Negative Going Threshold Voltage	V_{CC} = 5V	0.7	1.4	2.0	V
	V_{CC} = 10V	1.4	3.2	4.0	V
	V_{CC} = 15V	2.1	5.0	6.0	
Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5V	1.0	2.2	3.6	V
	V_{CC} = 10V	2.0	3.6	7.2	V
	V_{CC} = 15V	3.0	5.0	10.8	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	V_{CC} = 5V, I_O = −10μA	4.5			V
	V_{CC} = 10V, I_O = −10μA	9.0			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	V_{CC} = 5V, I_O = +10μA			0.5	V
	V_{CC} = 10V, I_O = +10μA			1.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 25V		0.005	5.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = −10V	−100.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V, V_{IN} = −10V/25V		0.05	300	μA
	V_{CC} = 5V, V_{IN} = 2.5V (Note 4)		20		μA
	V_{CC} = 10V, V_{IN} = 5V (Note 4)		200		μA
	V_{CC} = 15V, V_{IN} = 7.5V (Note 4)		600		μA
CMOS/LPTTL INTERFACE					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5V	4.3			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5V			0.7	V
Logical "1" Output Voltage ($V_{OUT(1)}$)	54C, V_{CC} = 4.5V, I_O = −360μA	2.4			V
	74C, V_{CC} = 4.75V, I_O = −360μA	2.4			V
Logical "0" Output Voltage ($V_{OUT(0)}$)	54C, V_{CC} = 4.5V, I_O = 360μA			0.4	V
	74C, V_{CC} = 4.75V, I_O = 360μA			0.4	V
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
Output Source Current (I_{SOURCE}) (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8.0	−15		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
Output Sink Current (I_{SINK}) (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8.0	16		mA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay from Input to Output (t_{pd0} or t_{pd1})	$V_{CC} = 5V$ $V_{CC} = 10$		220 80	400 200	ns ns
Input Capacitance	Any Input (Note 2)		5.0		pF
Power Dissipation Capacitance (C_{PD})	(Note 3) Per Gate		20		pF

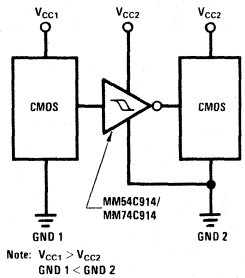
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

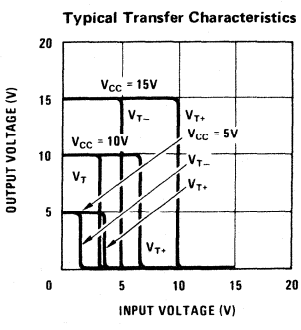
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

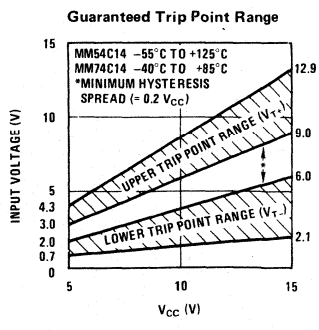
Note 4: Only one input is at 1/2 V_{CC}, the others are either at V_{CC} or GND.

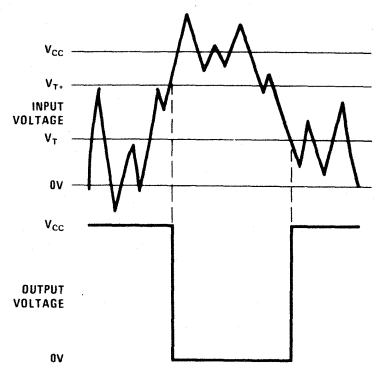
typical application



typical performance characteristics







National Semiconductor

MM54C915/MM74C915 7-Segment-to-BCD Converter

general description

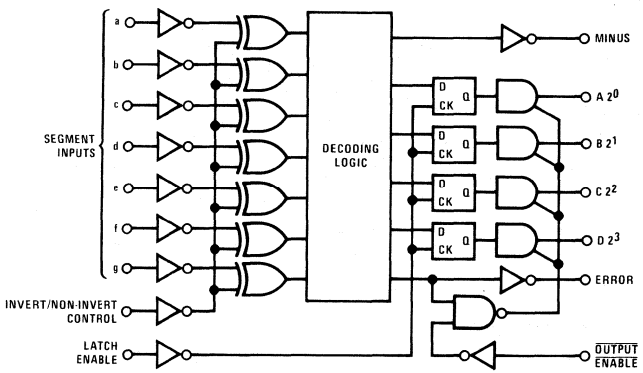
The MM54C915/MM74C915 is a monolithic complementary MOS (CMOS) integrated circuit, constructed with N and P-channel enhancement-mode transistors. This circuit accepts 7-segment information and converts it into BCD information. The true state of the Segment inputs can be selected by use of the Invert/Non-invert control pin. A logical "0" on the Invert/Non-invert control pin selects active high true decoding at the Segment inputs. A logical "1" on the Invert/Non-invert control pin selects active low true decoding at the Segment inputs. In addition to 4 TTL compatible BCD outputs, an Error output and Minus output are available. The Error output goes to an active "1" whenever a non-standard 7-segment code appears at the Segment inputs. The BCD outputs are forced into a TRI-STATE® condition when an error is detected. This allows the user to program his own error code by tying the BCD outputs to V_{CC} or Ground via high value resistors (~ 500k). The BCD outputs may also be forced into TRI-STATE by a logical "1" on output enable ($\overline{OE}$).

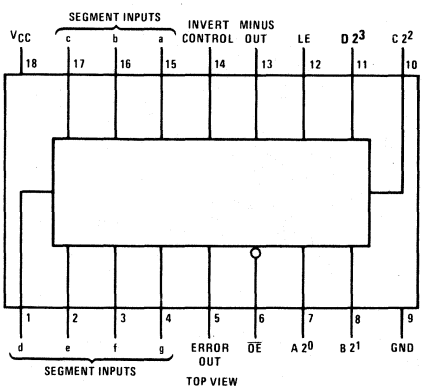
The Minus output goes to a logical "1" whenever a minus code is detected and is useful as a microprocessor interrupt. The BCD outputs are in a flow-though condition when Latch Enable (LE) is at a logical "0", and latched when LE is at a logical "1". The inputs will not clamp signals to the positive supply, allowing simple level translation from MOS to TTL.

features

■ Wide supply range	3V–15V
■ High noise immunity	0.45 V_{CC} typ
■ TTL compatible fan out	1 TTL load
■ Selectable active true inputs	
■ TRI-STATE outputs	
■ On-chip latch	
■ Error output	
■ Minus output	

logic and connection diagrams





absolute maximum ratings

Voltage at Any Output	$-0.3V$ to $V_{CC}+0.3V$	Storage Temperature Range	$-65°C$ to $+150°C$
Voltage at Any Input	$-0.3V$ to 18V	Package Dissipation	500 mW
Operating Temperature Range		Operating V_{CC} Range	3V to 15V
MM54C915	$-55°C$ to $+125°C$	Maximum V_{CC}	18V
MM74C915	$-40°C$ to $+85°C$	Lead Temperature, (Soldering, 10 seconds)	$300°C$

dc electrical characteristics

Min/max limits apply across temperature range unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	$V_{CC}=5V$	3.3	4.5		V
		$V_{CC}=10V$	8	9		V
		$V_{CC}=15V$	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage	$V_{CC}=5V$		0.5	1.5	V
		$V_{CC}=10V$		1	2	V
		$V_{CC}=15V$		1.5	2.5	V
$I_{IN(1)}$	Logical "1" Input Current	$V_{IN}=15V$		0.005	1	μA
$I_{IN(0)}$	Logical "0" Input Current	$V_{IN}=0V$	-1	-0.005		μA
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$		4.5		V
		$V_{CC}=10V$		9		V
		$V_{CC}=15V$		13.5		V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=10\mu A$				
		$V_{CC}=5V$		0.5		V
		$V_{CC}=10V$		1		V
		$V_{CC}=15V$		1.5		V
I_{CC}	Supply Current	$V_{CC}=5V$		0.25	1	mA
		$V_{CC}=10V$		0.75	2.5	mA
		$V_{CC}=15V$		1.00	3	mA
CMOS/TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage					
	MM54C915	$V_{CC}=4.5V$	$V_{CC}-1.7$			V
	MM74C915	$V_{CC}=4.75V$	$V_{CC}-1.7$			V
$V_{IN(0)}$	Logical "0" Input Voltage					
	MM54C915	$V_{CC}=4.5V$			0.8	V
	MM74C915	$V_{CC}=4.75V$			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	$I_O=-360\mu A$				
	MM54C915	$V_{CC}=4.5V$	2.4			V
	MM74C915	$V_{CC}=4.75V$	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	$I_O=1.6$ mA				
	MM54C915	$V_{CC}=4.5V$			0.4	V
	MM74C915	$V_{CC}=4.75V$			0.4	V
OUTPUT DRIVE						
I_{SOURCE}	Output Source Current	$T_A=25°C$, $V_O=0V$,				
	P-Channel	(Note 2)				
		$V_{CC}=5V$	-1.75	-3.3		mA
		$V_{CC}=10V$	-8	-15		mA
		$V_{CC}=15V$	-15	-25		mA
I_{SINK}	Output Sink Current	$T_A=25°C$, $V_O=V_{CC}$				
	N-Channel	(Note 2)				
		$V_{CC}=5V$	5	8		mA
		$V_{CC}=10V$	20	30		mA
		$V_{CC}=15V$	30	50		mA

ac electrical characteristics $T_A = 25°C$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0}, t_{pd1}	Propagation Delay Time to	C_L = 50 pF				
	Logical "0" or a Logical "1"	V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_{0H}, t_{1H}	Propagation Delay Time From	R_L = 10k, C_L = 10 pF				
	Logical "0" or Logical "1"	V_{CC} = 5V		110	200	ns
	into High Impedance State	V_{CC} = 10V		75	130	ns
		V_{CC} = 15V		60	110	ns
t_{H0}, t_{H1}	Propagation Delay Time From	R_L = 10k, C_L = 50 pF				
	High Impedance State to a	V_{CC} = 5V		150	250	ns
	Logical "0" or Logical "1"	V_{CC} = 10V		80	140	ns
		V_{CC} = 15V		70	125	ns
t_S	Input Data Set-Up Time	C_L = 50 pF				
		V_{CC} = 5V		500	1000	ns
		V_{CC} = 10V		300	600	ns
		V_{CC} = 15V		300	600	ns
t_H	Input Data Hold Time	C_L = 50 pF				
		V_{CC} = 5V		−150	0	ns
		V_{CC} = 10V		−100	0	ns
		V_{CC} = 15V		−100	0	ns
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF
C_{OUT}	TRI-STATE Output Capacitance	Any Output, (Note 3)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: These specifications apply to transient operation. It is not meant to imply that the device should be operated at these limits in sustained operation.

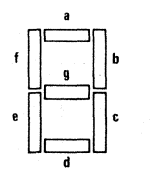
Note 3: Capacitance is guaranteed by periodic testing.

truth table

CHARACTER AT SEGMENT INPUTS	BCD OUTPUTS D 2^3	C 2^2	B 2^1	A 2^0	NON-BCD OUTPUTS ERROR	MINUS
0	0	0	0	0	0	0
1	0	0	0	1	0	0
2	0	0	0	1	0	0
3	0	0	1	0	0	0
4	0	0	1	1	0	0
5	0	1	0	0	0	0
6	0	1	0	1	0	0
7	0	1	1	0	0	0
8	0	1	1	0	0	0
9	0	1	1	1	0	0
	1	0	0	0	0	0
	1	0	0	1	0	0
	1	0	0	1	0	0
	1	1	1	1	0	0
-	X	X	X	X	1	1
All other input	X	X	X	X	1	0
combinations	X	X	X	X	1	0

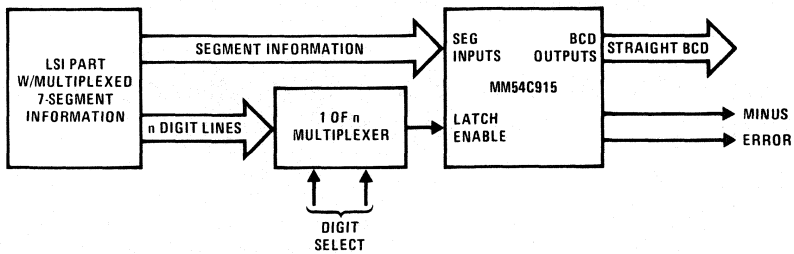
X = represents TRI-STATE condition

SEGMENT IDENTIFICATION

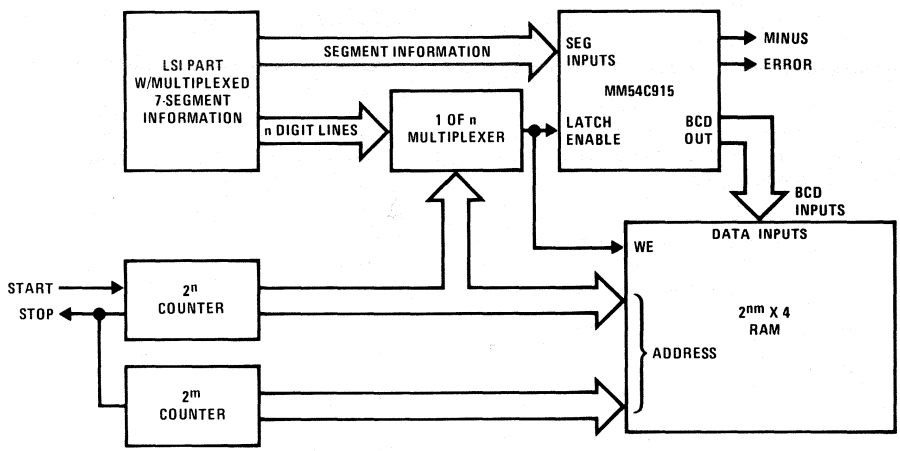


typical applications

Multiplex 7-Segment to Straight BCD



Memory Expansion from 7-Segment Outputs



National Semiconductor

MM54C920/MM74C920, MM54C921/MM74C921 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C920/MM74C920 256 x 4 random access read/write memory is manufactured using silicon gate CMOS technology. Data output is the same polarity as data input. Internal latches store address inputs $\overline{CES}$ and data output. This RAM is specifically designed to operate from standard 54/74 TTL power supplies. All inputs and outputs are TTL compatible.

The MM54C921/MM74C921 is identical to the MM54C920/MM74C920, except data inputs are internally connected to data outputs; the number of package leads thereby is reduced to 18.

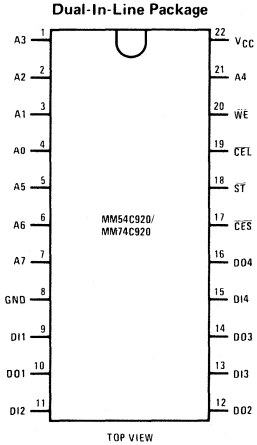
Complete address decoding as well as 2-chip select functions, $\overline{CEL}$ and $\overline{CES}$, and TRI-STATE® outputs allow easy expansion with a minimum of external components. Versatility plus high speed and low power make these RAMs ideal elements for use in microprocessor, minicomputer as well as main frame memory applications.

Features

- 256 x 4-bit organization
- Access time
  - 250 ns max MM74C920, MM74C921
  - 275 ns max MM54C920, MM54C921
  - 300 ns max MM74C920-3, MM74C921-3
- TRI-STATE outputs
- Low power
- On-chip registers
- Single 5V supply
- Data retained with V_{CC} as low as 2V

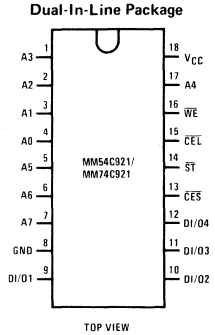
Connection Diagrams

Dual-In-Line Package



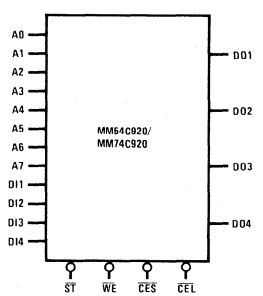
TOP VIEW

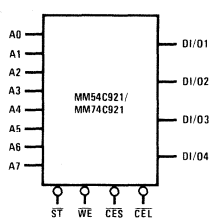
Dual-In-Line Package



TOP VIEW

Logic Symbols





Ordering Information

	MILITARY	COMMERCIAL	PACKAGE*
MM54C920, MM54C921	X		J, D
MM74C920, MM74C921		X	N, J, D
MM74C920–3, MM74C921–3		X	N, J, D

*J and N package available late 1977

Functional Description

The functional description will reference the logic diagram of the MM54C920/MM74C920 shown in *Figure 1*. Input addresses and $\overline{CES}$ are clocked into the input latches by the falling edge of $\overline{STROBE}$. Input set-up and hold times must be observed on these signals (see timing diagrams). The true and complement address information is fed to the row and column decoders which access the selected 4-bit memory word.

The addressed word (4 bits) is fed to 4 sense amplifiers through the column decoders. The information from the sense amplifiers is latched into the output register when $\overline{STROBE}$ rises. The register drives the TRI-STATE output buffers.

Chip select inputs, $\overline{CEL}$ and $\overline{CES}$, have identical functions except that $\overline{CES}$ (Chip Enable Stored) is clocked into a latch on the falling edge of $\overline{STROBE}$; $\overline{CEL}$ (Chip Enable Level) is not.

Note that set-up and hold times must be observed on $\overline{CES}$. Because $\overline{CEL}$ is not clocked by $\overline{STROBE}$, it may fall after $\overline{STROBE}$ has fallen without affecting access time provided that the t_{OE} requirement is met.

The outputs are in a high impedance state when the chip is not selected ($\overline{CES}$ or $\overline{CEL}$ high) or when writing ($\overline{WE}$ low). Note that the information stored in the output latches will be changed whenever $\overline{STROBE}$ falls, regardless of the logic states of $\overline{WE}$, $\overline{CEL}$ or $\overline{CES}$.

The switching time waveforms in *Figures 2, 3 and 4* define the read, write, and output enable/disable parameters respectively.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, $\overline{ST}$ logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*

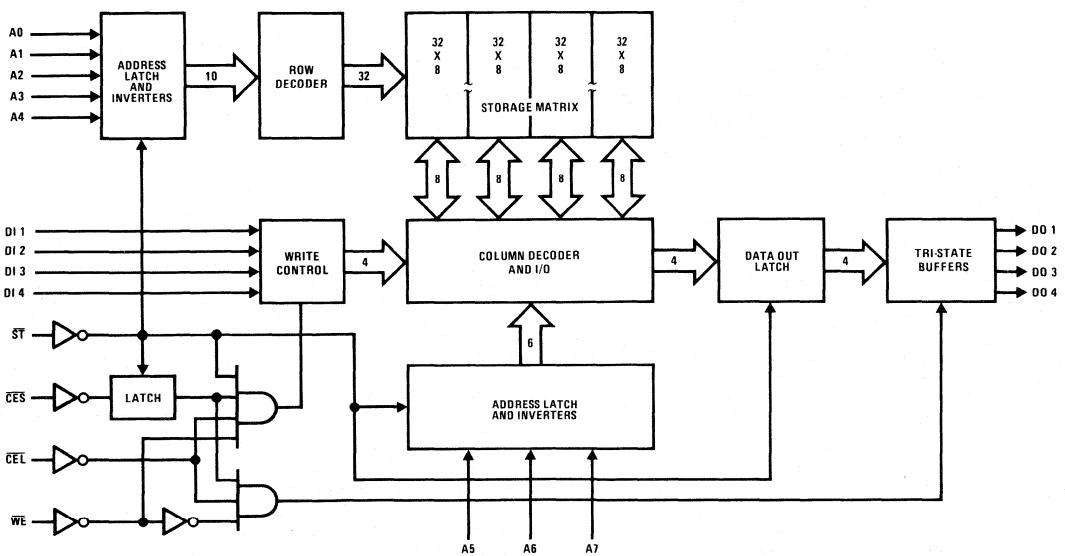


FIGURE 1. MM54C920/MM74C920

*The logic diagram for the MM54C921/MM74C921 is identical to this except that data inputs (DI1–DI4) are connected to data outputs (DO1–DO4).

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

Operating Conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
MM54C920, MM54C921	4.5	5.5	V
MM74C920, MM74C921	4.5	5.5	V
MM74C920-3, MM74C921-3	4.75	5.25	V
Ambient Temperature (T_A)			
MM54C920, MM54C921	−55	+125	°C
MM74C920, MM74C921	−40	+85	°C
MM74C920-3, MM74C921-3	0	+70	°C

DC Electrical Characteristics (Note 2)

SYMBOL	PARAMETER	CONDITIONS	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920−3, MM74C921−3		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−1.5	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = −1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, $\overline{CEL}$ = V_{CC}	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	V_{IN} = V_{CC}, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	$\overline{CEL}$ = V_{CC} = 2V, Typical at 25°C		0.01 (typ)		0.01 (typ)		0.1 (typ)	μA

Capacitance (Note 4)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		4	7	pF
C_O	Output Capacitance	V_{IN} = 0V, f = 1 MHz, T_A = 25°C		6	9	pF
$C_{I/O}$	Data Input/Output Capacitance	MM54C921/MM74C921 Only		8	12	pF

Note 1: "Absolute Maximum Ratings" are those values above which the device may be permanently damaged. They do not mean the device may be operated at these values.

Note 2: These limits apply over the entire operating range specified in the "Operating Conditions" unless otherwise stated.

Note 3: $\overline{CEL}$ = V_{CC} − 2V or = 2V, whichever is greater.

Note 4: Capacitance is guaranteed by periodic testing.

Truth Table

$\overline{ST}$	$\overline{CES}$*	$\overline{CEL}$	$\overline{WE}$	DI*	FUNCTION
X	X	1	X	X	Output in Hi-Z state
0	1	X	X	X	Output in Hi-Z state
X	X	X	0	X	Output in Hi-Z state
0	0	0	0	0	Write "0", output in Hi-Z state
0	0	0	0	1	Write "1", output in Hi-Z state
0	0	0	1	X	Read data, output enabled

*Set-up and hold times must be met
X = don't care

AC Electrical Characteristics (Note 5)

SYMBOL	PARAMETER	MM54C920, MM54C921		MM74C920, MM74C921		MM74C920–3 MM74C921–3		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		275		250		325	ns
t_{ACS}	Access Time From Strobe		250		225		300	ns
t_{AS}	Address Set-Up Time	25		25		25		ns
t_{AH}	Address Hold Time	25		25		25		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{ST}}$	$\overline{ST}$ Pulse Width (Negative)	150		130		165		ns
t_{ST}	ST Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time	100		90		90		ns
t_{DH}	Data Hold Time	60		60		60		ns

Note 5: These limits apply over the operating range specified in the "Operating Conditions" with $t_{RISE} = t_{FALL} = 5$ ns, load = 1 TTL gate + 50 pF.

Switching Time Waveforms

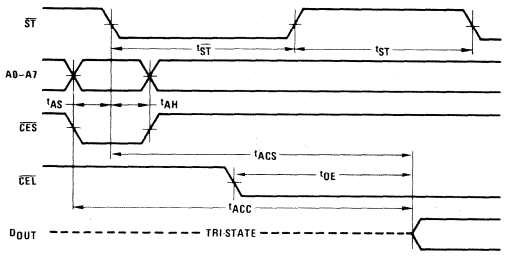
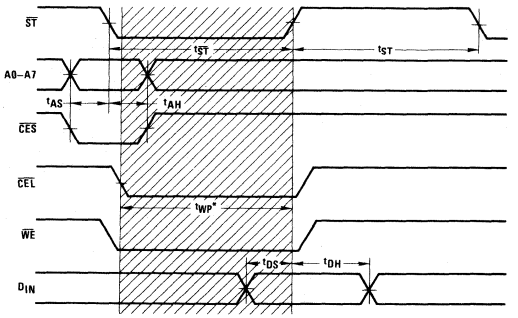
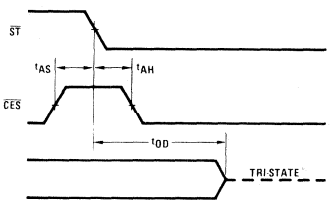


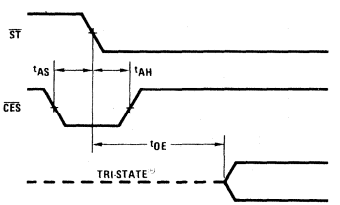
FIGURE 2. Read Cycle ($\overline{WE}$ = V_{IH})



*t_{WP} (the Write Pulse Width) is the time $\overline{ST}$, $\overline{CEL}$ and $\overline{WE}$ are coincidentally low

FIGURE 3. Write Cycle





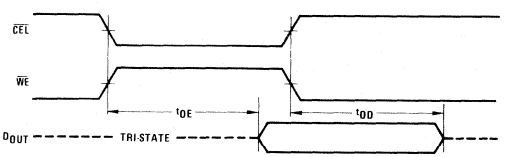
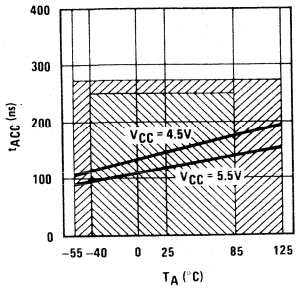


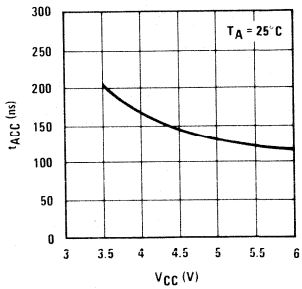
FIGURE 4. Output Enable/Disable

Typical Performance Characteristics

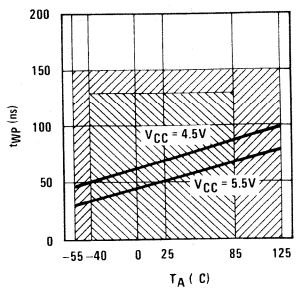
Access Time vs Ambient Temperature



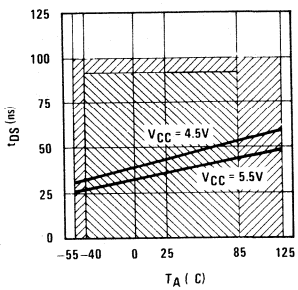
Access Time vs Power Supply Voltage



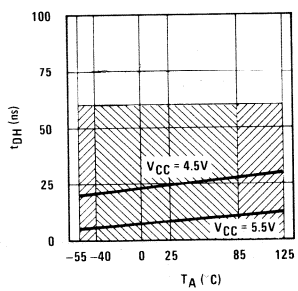
Minimum Write Pulse Width vs Ambient Temperature



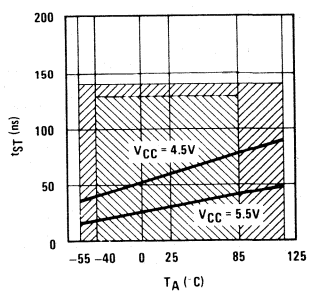
Data-In Setup Time vs Ambient Temperature



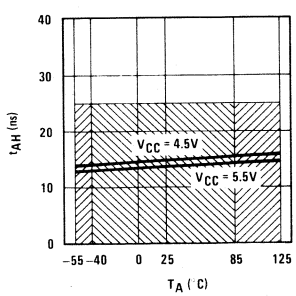
Data In Hold Time vs Ambient Temperature



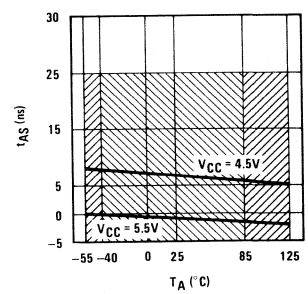
Minimum ST Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

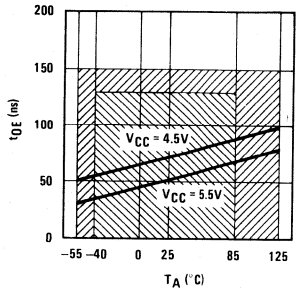


Address Setup Time vs Ambient Temperature

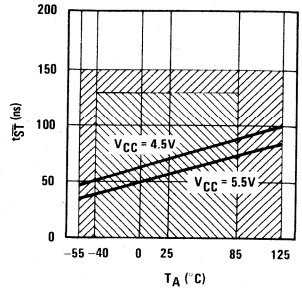


Typical Performance Characteristics (Continued)

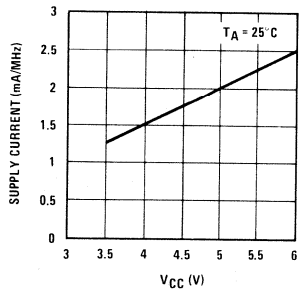
Output Enable Time vs Ambient Temperature



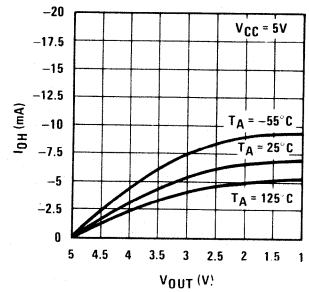
Minimum $\overline{ST}$ Pulse Width (Negative) vs Ambient Temperature



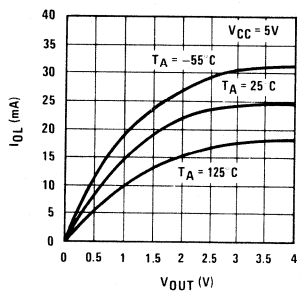
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, V_{IL} = 0V)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



Test Limit MM54C920, MM54C921

Test Limit MM74C920, MM74C921

National Semiconductor

MM54C922/MM74C922 16-Key Encoder
MM54C923/MM74C923 20-Key Encoder

general description

These CMOS key encoders provide all the necessary logic to fully encode an array of SPST switches. The keyboard scan can be implemented by either an external clock or external capacitor. These encoders also have on-chip pull-up devices which permit switches with up to 50 kΩ on resistance to be used. No diodes in the switch array are needed to eliminate ghost switches. The internal debounce circuit needs only a single external capacitor and can be defeated by omitting the capacitor. A Data Available output goes to a high level when a valid keyboard entry has been made. The Data Available output returns to a low level when the entered key is released, even if another key is depressed. The Data Available will return high to indicate acceptance of the new key after a normal debounce period; this two key roll over is provided between any two switches.

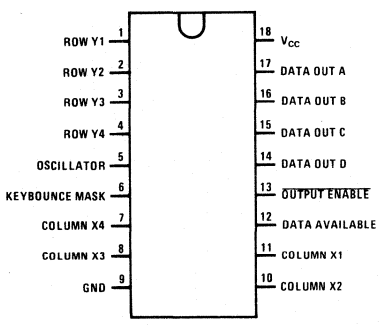
An internal register remembers the last key pressed even after the key is released. The TRI-STATE® outputs provide for easy expansion and bus operation and are LPTTL compatible.

features

- 50 kΩ maximum switch on resistance
- On or off chip clock
- On chip row pull-up devices
- 2 key roll-over
- Keybounce elimination with single capacitor
- Last key register at outputs
- TRI-STATE outputs LPTTL compatible
- Wide supply range 3V to 15V
- Low power consumption

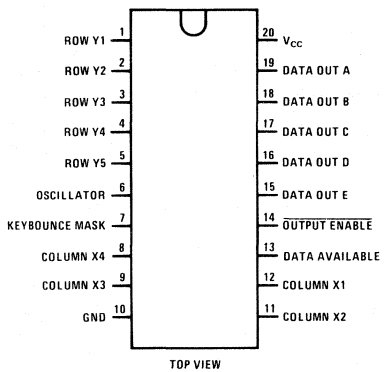
connection diagrams

Dual-In-Line Package



Order Number MM54C922N
or MM74C922N
See Package 20

Dual-In-Line Package



Order Number MM54C923N
or MM74C923N
See Package 20A

absolute maximum ratings

Voltage at Any Pin	V_{CC} – 0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C922, MM54C923	–55°C to +125°C
MM74C922, MM74C923	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
V_{T+}	Positive-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	3	3.6	4.3	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	6	6.8	8.6	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	9	10	12.9	V
V_{T-}	Negative-Going Threshold Voltage at Osc and KBM Inputs	V_{CC} = 5V, $I_{IN} \geq 0.7$ mA	0.7	1.4	2	V
		V_{CC} = 10V, $I_{IN} \geq 1.4$ mA	1.4	3.2	4	V
		V_{CC} = 15V, $I_{IN} \geq 2.1$ mA	2.1	5	6	V
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,	3.5	4.5		V
		V_{CC} = 10V,	8	9		V
		V_{CC} = 15V,	12.5	13.5		V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	V_{CC} = 5V,		0.5	1.5	V
		V_{CC} = 10V,		1	2	V
		V_{CC} = 15V,		1.5	2.5	V
I_{rp}	Row Pull-Up Current at Y1, Y2, Y3, Y4 and Y5 Inputs	V_{CC} = 5V, V_{IN} = 0.1 V_{CC}		–2	–5	μA
		V_{CC} = 10V		–10	–20	μA
		V_{CC} = 15V		–22	–45	μA
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = –10μA	4.5			V
		V_{CC} = 10V, I_O = –10μA	9			V
		V_{CC} = 15V, I_O = –10μA	13.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = 10μA			0.5	V
		V_{CC} = 10V, I_O = 10μA			1	V
		V_{CC} = 15V, I_O = 10μA			1.5	V
R_{on}	Column "ON" Resistance at X1, X2, X3 and X4 Outputs	V_{CC} = 5V, V_O = 0.5V		500	1400	Ω
		V_{CC} = 10V, V_O = 1V		300	700	Ω
		V_{CC} = 15V, V_O = 1.5V		200	500	Ω
I_{CC}	Supply Current	V_{CC} = 5V, Osc at 0V		0.55	1.1	mA
		V_{CC} = 10V		1.1	1.9	mA
		V_{CC} = 15V		1.7	2.6	mA
$I_{IN(1)}$	Logical "1" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current at $\overline{\text{Output Enable}}$	V_{CC} = 15V, V_{IN} = 0V	–1.0	–0.005		μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V	V_{CC}–1.5			V
		74C, V_{CC} = 4.75V	V_{CC}–1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage, Except Osc and KBM Inputs	54C, V_{CC} = 4.5V			0.8	V
		74C, V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	54C, V_{CC} = 4.5V, I_O = –360μA	2.4			V
		74C, V_{CC} = 4.75V, I_O = –360μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	54C, V_{CC} = 4.5V, I_O = –360μA			0.4	V
		74C, V_{CC} = 4.75V, I_O = –360μA			0.4	V

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT DRIVE (See 54C/74C Family Characteristics Data Sheet)					
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 5V, V_{OUT} = 0V, T_A = 25°C	−1.75	−3.3		mA
I_{SOURCE} Output Source Current (P-Channel)	V_{CC} = 10V, V_{OUT} = 0V, T_A = 25°C	−8	−15		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_A = 25°C	1.75	3.6		mA
I_{SINK} Output Sink Current (N-Channel)	V_{CC} = 10V, V_{OUT} = V_{CC}, T_A = 25°C	8	16		mA

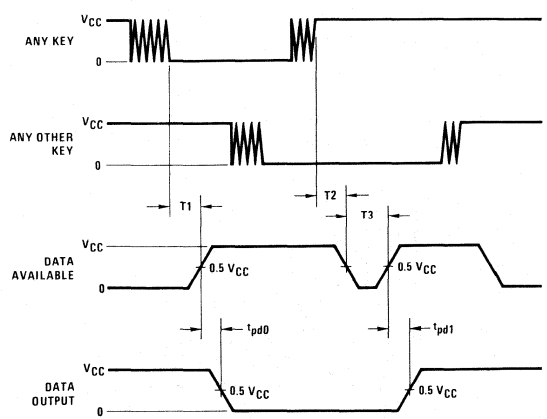
ac electrical characteristics T_A = 25°C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0},t_{pd1} Propagation Delay Time to	C_L = 50 pF, *(Figure 1)*				
Logical "0" or Logical "1"	V_{CC} = 5V		60	150	ns
from D.A.	V_{CC} = 10V		35	80	ns
	V_{CC} = 15V		25	60	ns
t_{0H},t_{1H} Propagation Delay Time from	R_L = 10k, C_L = 5 pF, *(Figure 2)*				
Logical "0" or Logical "1"	V_{CC} = 5V R_L = 10k		80	200	ns
into High Impedance State	V_{CC} = 10V C_L = 10 pF		65	150	ns
	V_{CC} = 15V		50	110	ns
t_{H0},t_{H1} Propagation Delay Time from	R_L = 10k, C_L = 50 pF, *(Figure 2)*				
High Impedance State to a	V_{CC} = 5V R_L = 10k		100	250	ns
Logical "0" or Logical "1"	V_{CC} = 10V C_L = 50 pF		55	125	ns
	V_{CC} = 15V		40	90	ns
C_{IN} Input Capacitance	Any Input, (Note 2)		5	7.5	pF
C_{OUT} TRI-STATE Output Capacitance	Any Output, (Note 2)		10		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

switching time waveforms



T1 ≃ T2 ≈ RC, T3 ≈ 0.7 RC where R ≃ 10k and C is external capacitor at KBM input.

FIGURE 1

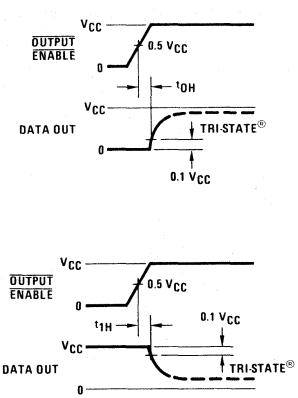
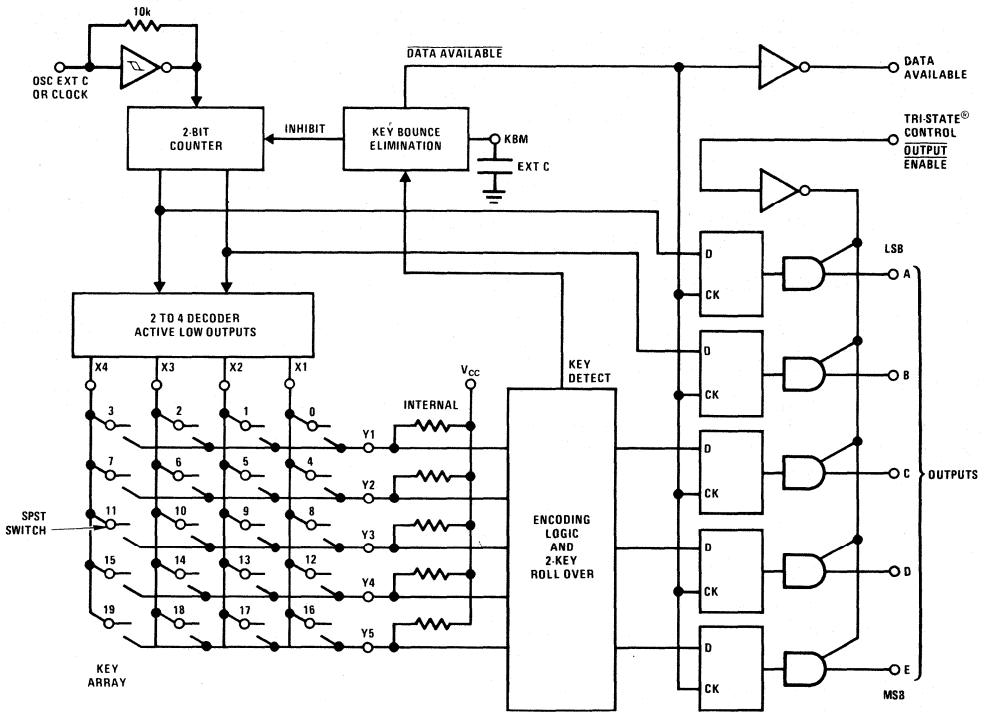


FIGURE 2

block diagram



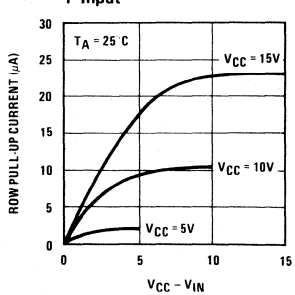
truth table

SWITCH POSITION		0 Y1,X1	1 Y1,X2	2 Y1,X3	3 Y1,X4	4 Y2,X1	5 Y2,X2	6 Y2,X3	7 Y2,X4	8 Y3,X1	9 Y3,X2	10 Y3,X3	11 Y3,X4	12 Y4,X1	13 Y4,X2	14 Y4,X3	15 Y4,X4	16 Y5*,X1	17 Y5*,X2	18 Y5*,X3	19 Y5*,X4
DATA OUT	A	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	B	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
	C	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
	D	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
	E*	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

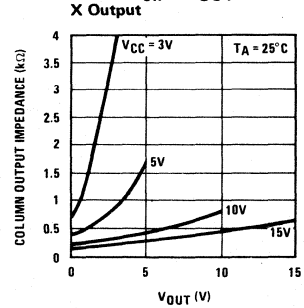
*Omit for MM54C922/MM74C922

typical performance characteristics

Typical I_{rp} vs V_{IN} at Any Y Input

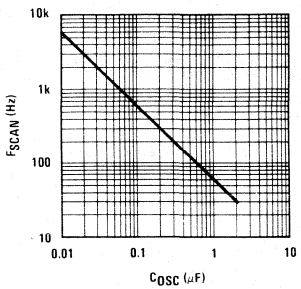


Typical R_{on} vs V_{OUT} at Any X Output

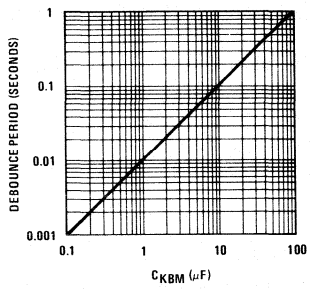


typical performance characteristics (con't)

Typical F_{SCAN} vs C_{OSC}

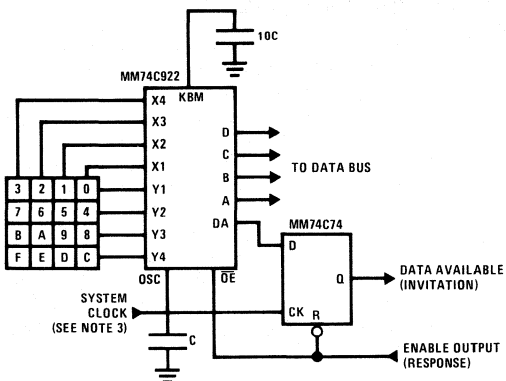


Typical Debounce Period vs C_{KBM}

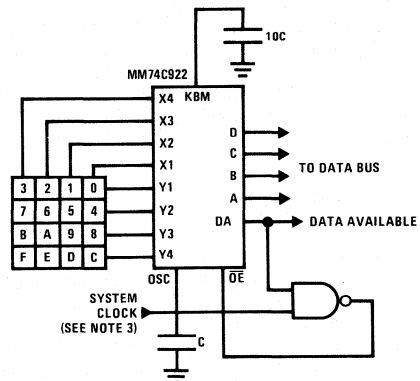


typical applications

Synchronous Handshake (MM74C922)

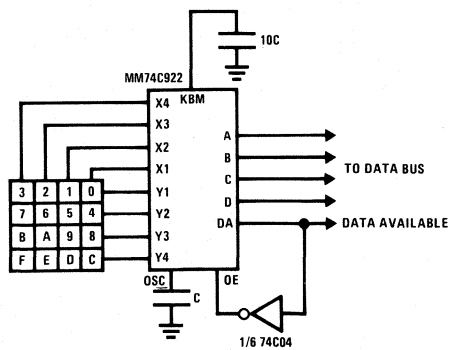


Synchronous Data Entry Onto Bus (MM74C922)



Outputs are enabled when valid entry is made and go into TRI-STATE when key is released.

Asynchronous Data Entry Onto Bus (MM74C922)



Outputs are in TRI-STATE until key is pressed, then data is placed on bus. When key is released, outputs return to TRI-STATE.

Keyboard Suppliers

Mini Key Series KL
Digitran Company
Pasadena, California

Computronics Engineering
7235 Hollywood Blvd
Hollywood, California 90046

Note 3: The keyboard may be synchronously scanned by omitting the capacitor at osc. and driving osc. directly if the system clock rate is lower than 10 kHz.

National Semiconductor

MM74C925, MM74C926, MM74C927, MM74C928 4-Digit Counters with Multiplexed 7-Segment Output Drivers

general description

These CMOS counters consist of a 4-digit counter, an internal output latch, NPN output sourcing drivers for a 7-segment display, and an internal multiplexing circuitry with four multiplexing outputs. The multiplexing circuit has its own free-running oscillator, and requires no external clock. The counters advance on negative edge of clock. A high signal on the Reset input will reset the counter to zero, and reset the carry-out low. A low signal on the Latch Enable input will latch the number in the counters into the internal output latches. A high signal on Display Select input will select the number in the counter to be displayed; a low level signal on the Display Select will select the number in the output latch to be displayed.

The MM74C925 is a 4-decade counter and has Latch Enable, Clock and Reset inputs.

The MM74C926 is like the MM74C925 except that it has a display select and a carry-out used for cascading counters. The carry-out signal goes high at 6000, goes back low at 0000.

The MM74C927 is like the MM74C926 except the second most significant digit divides by 6 rather than 10. Thus, if the clock input frequency is 10 Hz, the display would read tenths of seconds and minutes (i.e., 9:59.9).

The MM74C928 is like the MM74C926 except the most significant digit divides by 2 rather than 10 and the carry-out is an overflow indicator which is high at 2000, and it goes back low only when the counter is reset. Thus, this is a 3 1/2-digit counter.

features

- Wide supply voltage range — 3V to 6V
- Guaranteed noise margin — 1V
- High noise immunity — 0.45 V_{CC} typ
- High segment sourcing current — 40 mA @ V_{CC} − 1.6V, V_{CC} = 5V
- Internal multiplexing circuitry

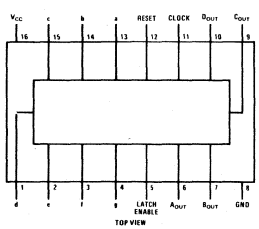
design considerations

Segment resistors are desirable to minimize power dissipation and chip heating. The DM75492 serves as a good digit driver when it is desired to drive bright displays. When using this driver with a 5V supply at room temperature, the display can be driven without segment resistors to full illumination. The user must use caution in this mode however, to prevent overheating of the device by using too high a supply voltage or by operating at high ambient temperatures.

The input protection circuitry consists of a series resistor, and a diode to ground. Thus input signals exceeding V_{CC} will not be clamped. This input signal should not be allowed to exceed 15V.

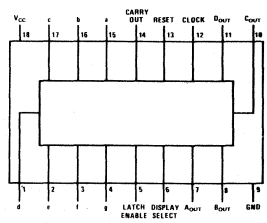
connection diagrams

Dual-In-Line Package
MM74C925



TOP VIEW

Dual-In-Line Package
MM74C926, MM74C927 and MM74C928



TOP VIEW

functional description

Reset — Asynchronous, active high

Display Select — High, displays output of counter
Low, displays output of latch

Latch Enable — High, flow through condition
Low, latch condition

Clock — Negative edge sensitive

Segment Output — Current sourcing with 80 mA @ V_{OUT} = V_{CC} − 1.6V typical. Also, sink capability = 2 LTTL loads

Digit Output — Current sourcing with 1 mA @ V_{OUT} = 1.75V. Also, sink capability = 2 LTTL loads

Carry-out — 2 LTTL loads. See carry-out waveforms.

absolute maximum ratings (Note 1)

Voltage at Any Output Pin	Gnd − 0.3V to V_{CC}+0.3V
Voltage at Any Input Pin	Gnd − 0.3V to +15V
Operating Temperature Range (T_A)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	Refer to $P_{D(MAX)}$ vs T_A Graph
Operating V_{CC} Range	3V to 6V
V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply at −40°C ≤ T_j ≤ +85°C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-out and Digit Output Only)	V_{CC} = 5.0V, I_O = −10 μA	4.5			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V, I_O = 10 μA			0.5	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 5.0V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 5.0V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 5.0V, Outputs Open Circuit, V_{IN} = 0V or 5V		20	1000	μA
CMOS/LPTTL INTERFACE						
$V_{IN(1)}$*	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Carry-Out and Digit Output Only)	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE						
V_{OUT}	Output Voltage (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		V_{CC}−1.3		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C	V_{CC}−1.6	V_{CC}−1.2		V
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C	V_{CC}−2	V_{CC}−1.4		V
R_{ON}	Output Resistance (Segment Sourcing Output)	I_{OUT} = −65 mA, V_{CC} = 5V, T_j = 25°C		20		Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 100°C		30	40	Ω
		I_{OUT} = −40 mA, V_{CC} = 5V, T_j = 150°C		35	50	Ω
	Output Resistance (Segment Output) Temperature Coefficient			0.6	0.8	%/°C
I_{SOURCE}	Output Source Current (Digit Output)	V_{CC} = 4.75V, V_{OUT} = 1.75V, T_j = 150°C	−1	−2		mA
I_{SOURCE}	Output Source Current (Carry-out)	V_{CC} = 5V, V_{OUT} = 0V, T_j = 25°C	−1.75	−3.3		mA
I_{SINK}	Output Sink Current (All Outputs)	V_{CC} = 5V, V_{OUT} = V_{CC}, T_j = 25°C	1.75	3.6		mA
θ_{jA}	Thermal Resistance	MM74C925 (Note 4)		75	100	°C/W
		MM74C926, MM74C927, MM74C928		70	90	°C/W

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

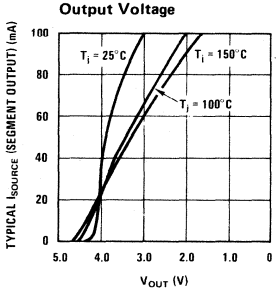
Note 4: θ_{jA} measured in free-air with device soldered into printed circuit board.

ac electrical characteristics $T_j = 25°C$, $C_L = 50$ pF, unless otherwise specified

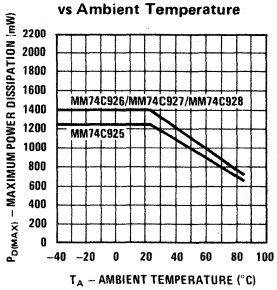
PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5.0V$,	$T_j = 25°C$	2	4		MHz
		Square Wave Clock	$T_j = 100°C$	1.5	3		MHz
t_r, t_f	Maximum Clock Rise or Fall Time	$V_{CC} = 5.0V$				15	μs
t_{WR}	Reset Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
t_{WLE}	Latch Enable Pulse Width	$V_{CC} = 5.0V$	$T_j = 25°C$	250	100		ns
			$T_j = 100°C$	320	125		ns
$t_{SET(CK,LE)}$	Clock to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	2500	1250		ns
			$T_j = 100°C$	3200	1600		ns
t_{LR}	Latch Enable to Reset	$V_{CC} = 5.0V$	$T_j = 25°C$	0	−100		ns
	Wait Time		$T_j = 100°C$	0	−100		ns
$t_{SET(R,LE)}$	Reset to Latch Enable Set-Up Time	$V_{CC} = 5.0V$	$T_j = 25°C$	320	160		ns
			$T_j = 100°C$	400	200		ns
f_{MUX}	Multiplexing Output Frequency	$V_{CC} = 5.0V$			1000		Hz
C_{IN}	Input Capacitance	Any Input (Note 2)			5		pF

typical performance characteristics

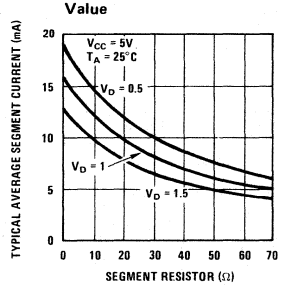
Typical Segment Current vs Output Voltage



Maximum Power Dissipation vs Ambient Temperature



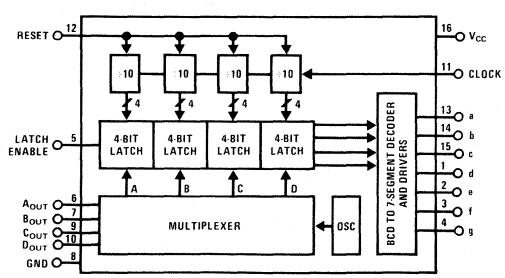
Typical Average Segment Current vs Segment Resistor Value



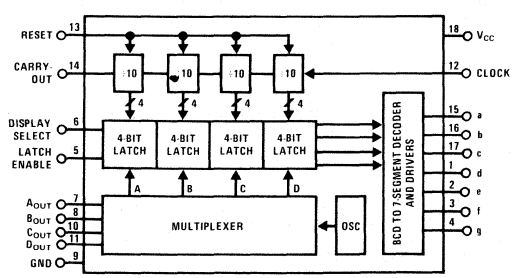
Note. V_D = Voltage across digit driver.

logic and block diagrams

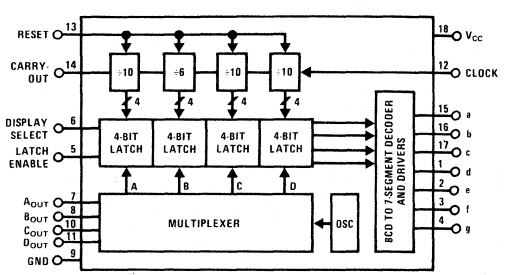
MM74C925



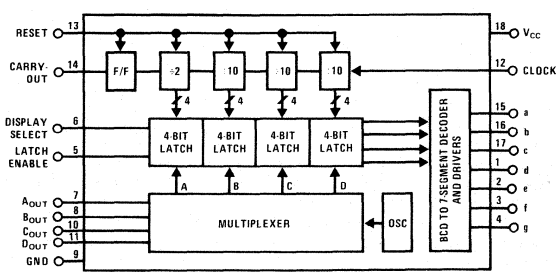
MM74C926



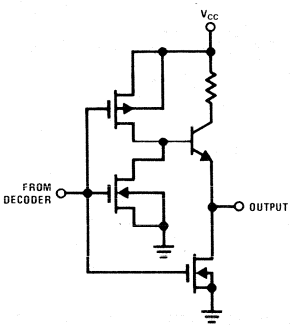
MM74C927



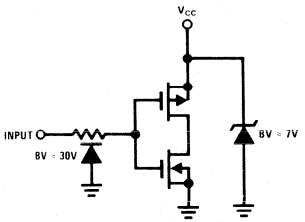
MM74C928



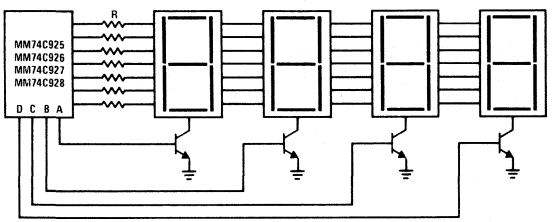
Segment Output Driver



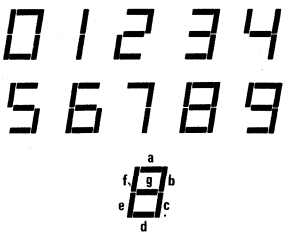
Input Protection



Common Cathode LED Display

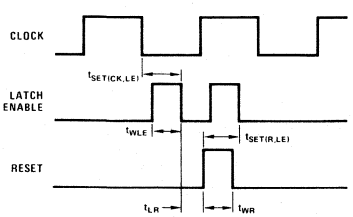


Segment Identification

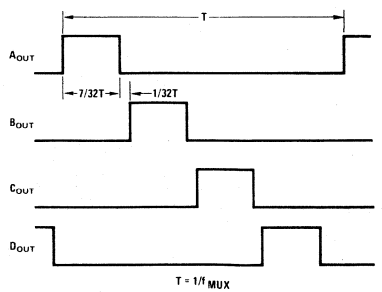


switching time waveforms

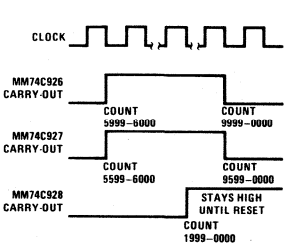
Input Waveforms



Multiplexing Output Waveforms



Carry-Out Waveforms



National Semiconductor

MM54C929/MM74C929, MM54C930/MM74C930 1024-Bit Static Silicon Gate CMOS RAMs

General Description

The MM54C929/MM74C929 and the MM54C930/MM74C930 1024 x 1 random access read/write memories are manufactured using silicon-gate CMOS technology. These RAMs are specifically designed to operate from standard 54/74 TTL power supplies; all inputs and outputs are TTL compatible. Data output is the same polarity as data input. Internal latches store the address inputs and data output. Chip select input $\overline{CS1}$ serves as a chip strobe, controlling address and data latching. The Data-In and Data-Out terminals can be tied together for common I/O applications. Complete address decoding, 3-chip select functions (MM54C930/MM74C930) and TRI-STATE® output allow easy memory expansion and organization. The MM54C929/MM74C929 differs from the MM54C930/MM74C930 only in that $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$ are internally connected together, providing a single chip-select input $\overline{CS}$.

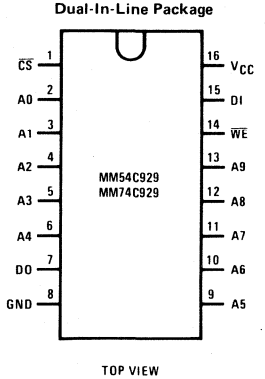
Versatility, high speed, and low power make these RAMs ideal elements for use in many microprocessor, minicomputer and main-frame-memory applications.

Features

- Fast access—250 ns max
- TRI-STATE outputs
- Low power—10 μA max standby
- On-chip registers
- Single 5V supply
- Inputs and output TTL compatible
- Data retained with V_{CC} as low as 2V
- Can be operated common I/O

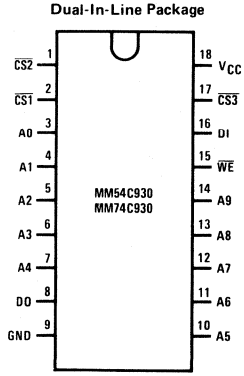
Connection Diagrams

Dual-In-Line Package



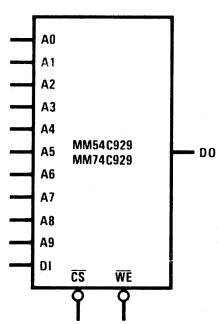
TOP VIEW

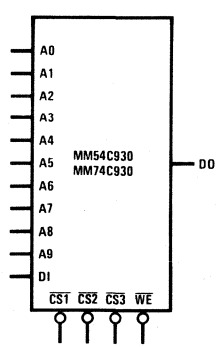
Dual-In-Line Package



TOP VIEW

Logic Symbols





Ordering Information

	MILITARY	COMMERICAL	PACKAGE*
MM54C929, MM54C930	X		J, D
MM74C929, MM74C930		X	N,J,D
MM74C929–3, MM74C930–3		X	N,J,D

*J and N package available late 1977

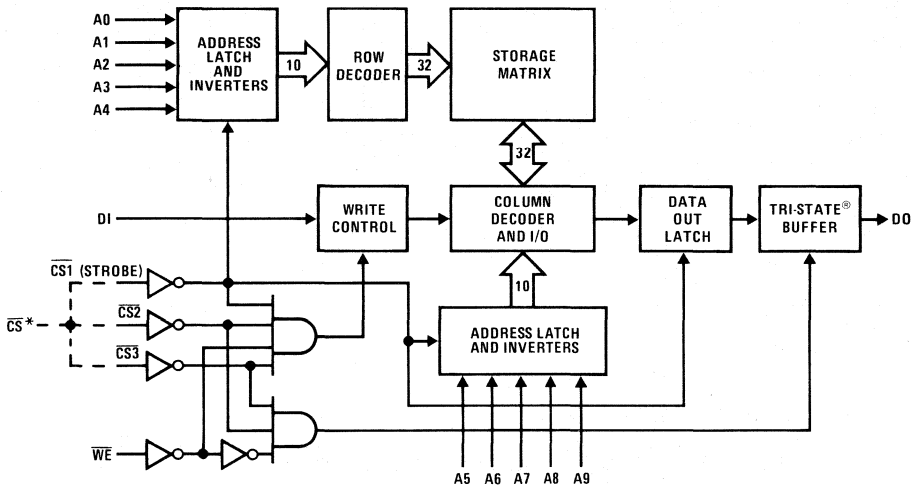
Functional Description

Address inputs are clocked into the input latches by the falling edge of chip strobe $\overline{CS1}$; set-up and hold times must be observed on these input signals (see timing diagram). The true and complement address information is fed to the row and column decoders which select one of the 1024-bit locations. The addressed bit is fed, via a sense amplifier, to the output register and TRI-STATE buffer. The information is latched into the output register on the rising edge of chip strobe $\overline{CS1}$. The output is in a high impedance state when the chip is not selected ($\overline{CS2}$ or $\overline{CS3}$ high) or when writing ($\overline{WE}$ low). Output buffer control is independent of chip strobe $\overline{CS1}$.

Reduced-Voltage Operation

These memories will retain data with reduced V_{CC} and hence are useful for battery-backup data storage. Certain precautions must be observed as V_{CC} is reduced: (1) input voltages must remain between the V_{CC} and ground of the RAM or supply latch-up can occur, (2) WRITE mode must be avoided, (3) during power-up of V_{CC}, strobe ($\overline{CS}$ for the MM74C929 and $\overline{CS1}$ for the MM74C930) logic state must be maintained (either GND or V_{CC}) while address control lines stabilize.

Logic Diagram*



*The MM74C930 has 3 chip selects $\overline{CS1}$, $\overline{CS2}$ and $\overline{CS3}$. The MM74C929 has these internally connected together providing a single chip select input $\overline{CS}$.

FIGURE 1

Absolute Maximum Ratings

Supply Voltage, V_{CC}	7V
Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
MM54C929, MM54C930	−55°C to +125°C
MM74C929, MM74C930	−40°C to +85°C
MM74C929-3, MM74C930-3	0°C to +70°C
Package Dissipation	500 mW
Lead Temperature (Soldering 10 seconds)	300°C

DC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{IH}	Logical "1" Input Voltage		V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V_{CC}−2.0	V_{CC}	V
V_{IL}	Logical "0" Input Voltage		0	0.8	0	0.8	0	0.8	V
V_{OH1}	Logical "1" Output Voltage	I_{OH} = 1 mA	2.4		2.4		2.4		V
V_{OH2}	Logical "1" Output Voltage	I_{OUT} = 0	V_{CC}−0.1		V_{CC}−0.1		V_{CC}−0.1		V
V_{OL1}	Logical "0" Output Voltage	I_{OL} = 2.0 mA		0.4		0.4		0.4	V
V_{OL2}	Logical "0" Output Voltage	I_{OUT} = 0		0.01		0.01		0.01	V
I_{IL}	Input Leakage	$0V \leq V_{IN} \leq V_{CC}$	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_O	Output Leakage	$0V \leq V_O \leq V_{CC}$, (Note 2)	−1.0	1.0	−1.0	1.0	−1.0	1.0	μA
I_{CC}	Supply Leakage Current	$V_{IN} = V_{CC}$, V_O = 0V		20		10		100	μA
V_{DR}	V_{CC} for Data Retention	(Note 3)	2.0		2.0		2.0		V
I_{DR}	I_{CC} for Data Retention	V_{CC} = 2V, T_A = 25°C, (Note 2)		0.01 (typ)		0.01 (typ)		0.1 (typ)	μA

Note 1: V_{CC} = 5V ±5%.
Note 2: $\overline{CS2} = \overline{CS3} = V_{CC}$ or $\overline{CS} = V_{CC}$.
Note 3: $\overline{CS2}$ or $\overline{CS3}$ or $\overline{CS}$ = V_{CC} − 2V or = 2V, whichever is greater.

AC Electrical Characteristics V_{CC} = 5V ±10%, T_A = Operating Range, unless otherwise noted

TTL Interface ($V_{IH} = V_{CC} - 2V$, V_{IL} = 0.8V, Input $t_{RISE} = t_{FALL}$ = 5 ns, Load = 1 TTL Gate + 50 pF)

SYMBOL	PARAMETER	MM54C929, MM54C930		MM74C929, MM74C930		MM74C929-3, MM74C930-3 (NOTE 1)		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_C	Cycle Time	290		255		330		ns
t_{ACC}	Access Time From Address		265		240		315	ns
t_{ACS},t_{ACS1}	Access Time From $\overline{CS}$, $\overline{CS1}$		250		225		300	ns
t_{AS}	Address Set-Up Time	15		15		15		ns
t_{AH}	Address Hold Time	50		50		50		ns
t_{OE}	Output Enable Time		150		130		130	ns
t_{OD}	Output Disable Time		150		130		130	ns
$t_{\overline{CS}}$,$t_{\overline{CS1}}$ (Note 4)	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Negative)	150		130		165		ns
t_{CS},t_{CS1}	$\overline{CS}$, $\overline{CS1}$ Pulse Width (Positive)	140		125		165		ns
t_{WP}	Write Pulse Width (Negative)	150		130		165		ns
t_{DS}	Data Set-Up Time, (Note 5)	150		140		140		ns
t_{DH}	Data Hold Time, (Note 5)	0		0		0		ns

Note 4: Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation.

Note 5: t_{DS} and t_{DH} are referenced to the low-to-high transition of $\overline{CS1}$ or $\overline{CS2}$ or $\overline{CS3}$ or $\overline{WE}$,whichever switches first, for the MM54C930/MM74C930 and are referenced to the $\overline{CS}$ or $\overline{WE}$ low-to-high transition, whichever switches first, for the MM54C929/MM74C929.

Capacitance (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
C_{IN}	Input Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	4	7	pF
C_O	Output Capacitance	V_{IN} = 0, f = 1 MHz, T_A = 25°C	6	9	pF
$C_{\overline{CS}}$	Chip Select Capacitance	MM54C929/MM74C929, MM74C929-3	8	12	pF

Note 6: Capacitance maximum is guaranteed by periodic testing.

Truth Tables

MM54C929/MM74C929

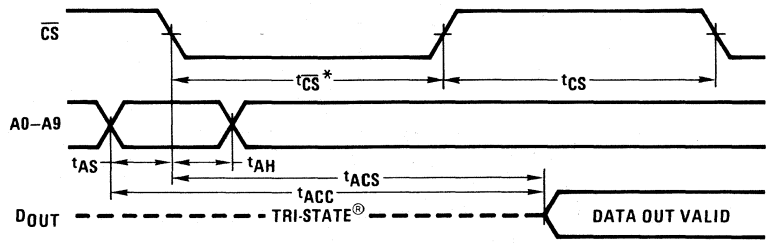
$\overline{CS}$	$\overline{WE}$	DI	FUNCTION
1	X	X	Output in Hi-Z State
X	0	X	Output in Hi-Z State
0	0	0	Write "0," Output in Hi-Z State
0	0	1	Write "1," Output in Hi-Z State
0	1	X	Read Data, Output Enabled

X = Don't care

MM54C930/MM74C930

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$	$\overline{WE}$	DI	FUNCTION
X	1	X	X	X	Output in Hi-Z State
X	X	1	X	X	Output in Hi-Z State
X	X	X	0	X	Output in Hi-Z State
0	0	0	0	0	Write "0," Output in Hi-Z State
0	0	0	0	1	Write "1," Output in Hi-Z State
0	0	0	1	X	Read Data, Output Enabled

Switching Time Waveforms



*Greater than minimum $\overline{CS}$ pulse width must be used when reading data from the MM54C929/MM74C929 to ensure that output TRI-STATING does not occur before data becomes valid. Writing has no such limitation, *(Figure 4a)*.

FIGURE 2a. MM54C929/MM74C929 Read Cycle

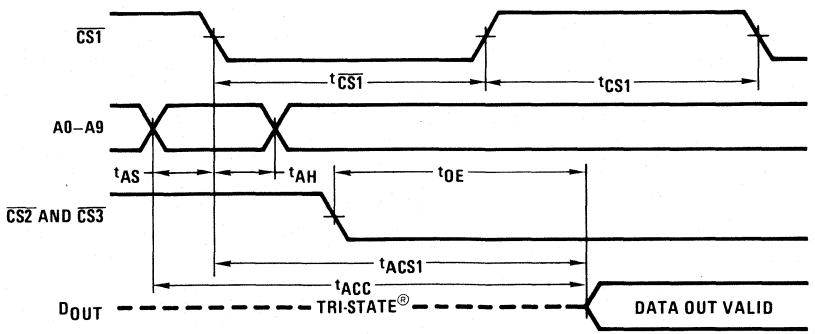
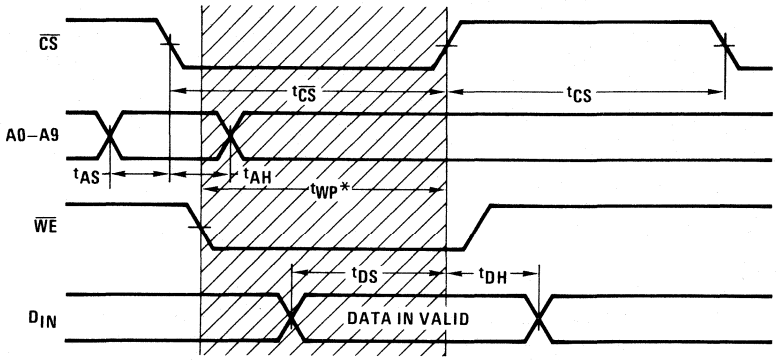


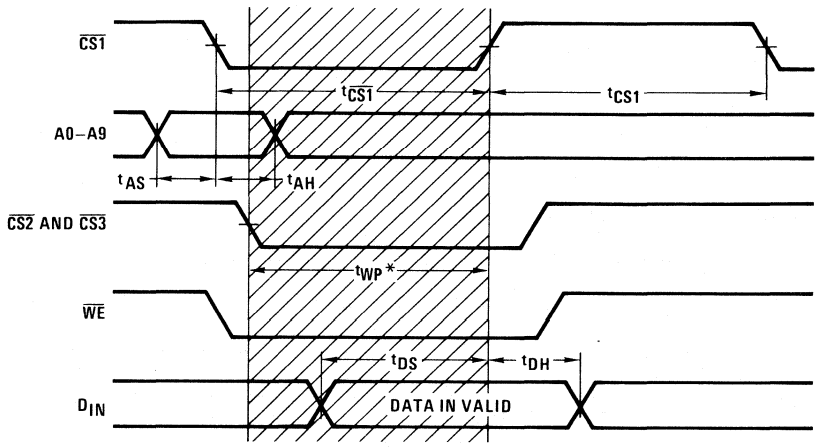
FIGURE 2b. MM54C930/MM74C930 Read Cycle

Switching Time Waveforms (Continued)



*t_{WP} (the Write Pulse width) is the time $\overline{CS}$ and $\overline{WE}$ are coincidentally low

FIGURE 3a. MM54C929/MM74C929 Write Cycle



*t_{WP} (the Write Pulse width) is the time $\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$ and $\overline{WE}$ are coincidentally low

FIGURE 3b. MM54C930/MM74C930 Write Cycle

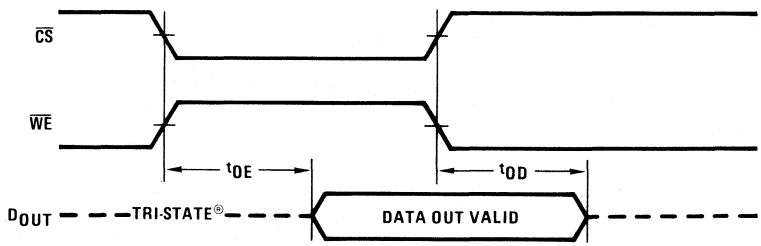


FIGURE 4a. MM54C929/MM74C929

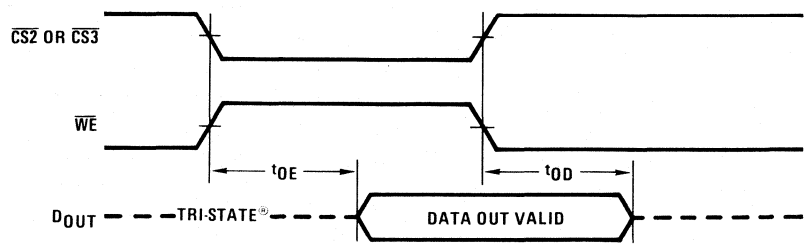
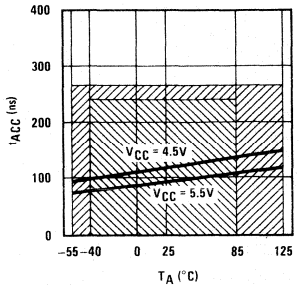


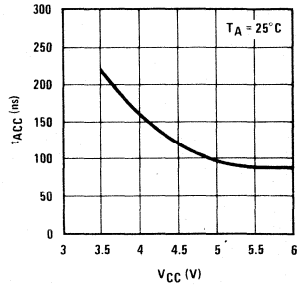
FIGURE 4b. MM54C930/MM74C930

Typical Performance Characteristics

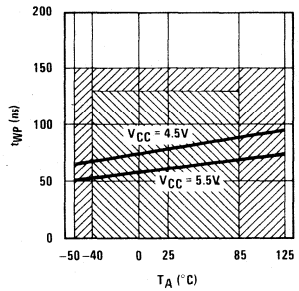
Access Time vs Ambient Temperature



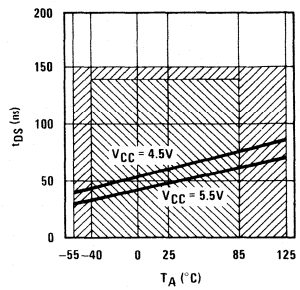
Access Time vs Power Supply Voltage



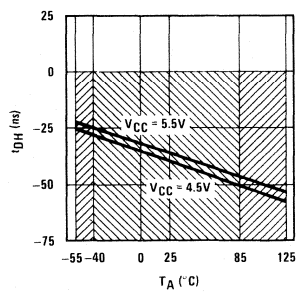
Minimum Write Pulse Width vs Ambient Temperature



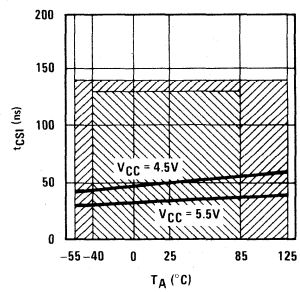
Data-In Set-Up Time vs Ambient Temperature



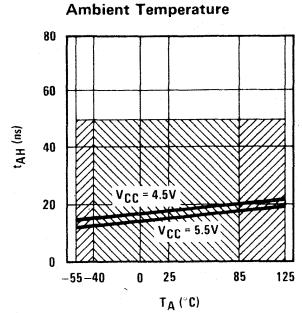
Data-In Hold Time vs Ambient Temperature



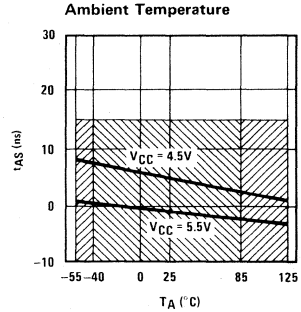
Minimum $\overline{CS}$I Pulse Width (Positive) vs Ambient Temperature



Address Hold Time vs Ambient Temperature

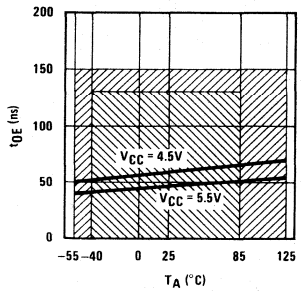


Address Set-Up Time vs Ambient Temperature

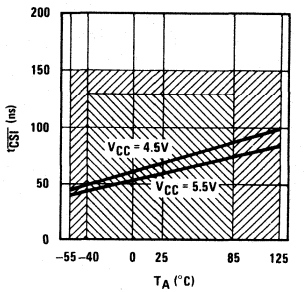


Typical Performance Characteristics (Continued)

Output Enable Time vs Ambient Temperature



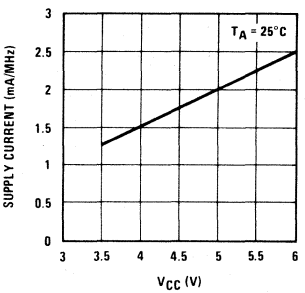
Minimum $\overline{CS1}$ Pulse Width (Negative) vs Ambient Temperature



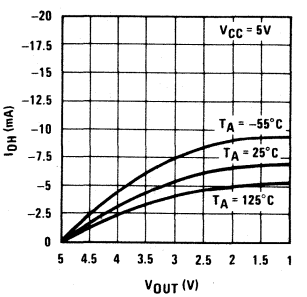
Test Limit MM54C929, MM54C930

Test Limit MM74C929, MM74C930

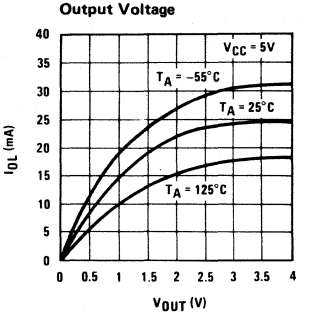
Dynamic Current vs Power Supply Voltage ($V_{IH} = V_{CC}$, $V_{IL} = 0V$)



Output Source Current vs Output Voltage



Output Sink Current vs Output Voltage



National Semiconductor

MM54C932/MM74C932 Phase Comparator

General Description

The MM74C932/MM54C932 consists of two independent output phase comparator circuits. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

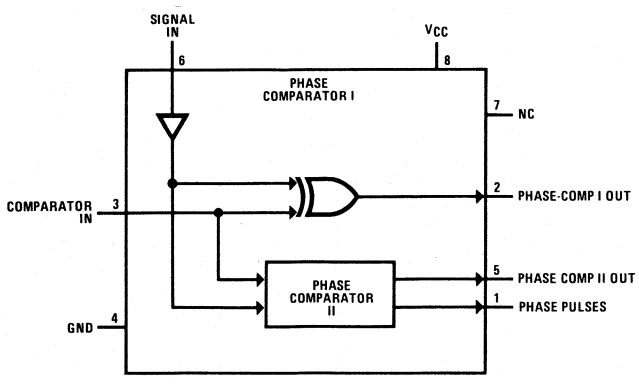
Phase comparator I, an exclusive-OR gate, provides a digital error signal (phase comp. I out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II out) and lock in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

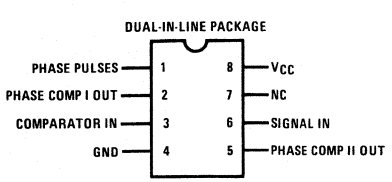
Features

- Wide supply voltage range
- Convenient mini-DIP package
- TRI-STATE® phase-comparator output (comparator II)
- 200 mV input voltage (signal in) sensitivity typical

Block Diagram



Connection Diagram



Absolute Maximum Ratings Note 1

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM54C932	−55°C to +125°C
MM74C932	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{CC} Range	3V to 15V
Absolute Maximum V_{CC}	18V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

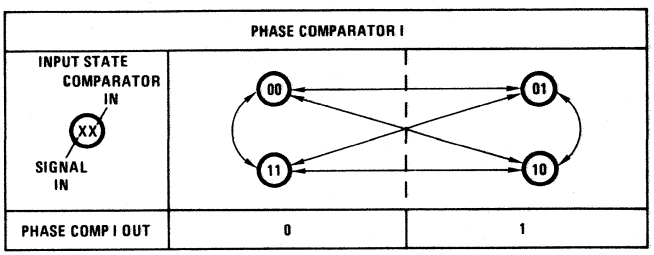
	Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Quiescent Device Current	PIN 5 = V_{CC}, PIN 8 = V_{CC}, PIN 3 = O_V				
		V_{CC} = 5V		0.005	150	μA
		V_{CC} = 10V		0.01	300	μA
		V_{CC} = 15V		0.015	600	μA
		PIN 5 = V_{CC}, PIN 8 = Open, PIN 3 = O_V				
		V_{CC} = 5V		5	205	μA
		V_{CC} = 10V		20	710	μA
		V_{CC} = 15V		50	1800	μA
V_{OL}	Low Level Output Voltage	V_{CC} = 5V		0	0.05	V
		V_{CC} = 10V		0	0.05	V
		V_{CC} = 15V		0	0.05	V
V_{OH}	High Level Output Voltage	V_{CC} = 5V	4.95	5		V
		V_{CC} = 10V	9.95	10		V
		V_{CC} = 15V	14.95	15		V
V_{IL}	Low Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V		2.25	1.5	V
		V_{CC} = 10V, V_O = 1V or 9V		4.5	3.0	V
		V_{CC} = 15V, V_O = 1.5V or 13.5V		6.25	4.0	V
V_{IH}	High Level Input Voltage Comparator and Signal	V_{CC} = 5V, V_O = 0.5V or 4.5V	3.5	2.75		V
		V_{CC} = 10V, V_O = 1V or 9V	7.0	5.5		V
		V_{CC} = 15V, V_O = 1.5V or 13.5V	11.0	8.25		V
I_{OL}	Low Level Output Current	V_{CC} = 5V, V_O = 0.4V	0.36	0.88		mA
		V_{CC} = 10V, V_O = 0.5V	0.9	2.25		mA
		V_{CC} = 15V, V_O = 1.5V	2.4	8.8		mA
I_{OH}	High Level Output Current	V_{CC} = 5V, V_O = 4.6V	−0.36	−0.88		mA
		V_{CC} = 10V, V_O = 9.5V	−0.9	−2.25		mA
		V_{CC} = 15V, V_O = 13.5V	−2.4	−8.8		mA
I_{IN}	Input Current	All Inputs Except Signal Input				
		V_{CC} = 15V, V_{IN} = 0V		-10^{-5}	−1.0	μA
		V_{CC} = 15V, V_{IN} = 15V		10^{-5}	1.0	μA
C_{IN}	Input Capacitance	Any Input, (Note 3)			7.5	pF
P_T	Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = V_{CC}/2				
		V_{CC} = 5V		0.07		mW
		V_{CC} = 10V		0.6		mW
		V_{CC} = 15V		2.4		mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Electrical Characteristics

Parameter		Conditions	Min	Typ	Mac	Units
Phase Comparators						
R_{IN}	Input Resistance Signal Input	V_{CC} = 5V	1.0	3.0		MΩ
		V_{CC} = 10V	0.2	0.7		MΩ
		V_{CC} = 15V	0.1	0.3		MΩ
	Comparator Input	V_{CC} = 5V		10^6		MΩ
		V_{CC} = 10V		10^6		MΩ
		V_{CC} = 15V		10^6		MΩ
	AC Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000pF f = 50kHz				
		V_{CC} = 5V		200	400	mV
		V_{CC} = 10V		400	800	mV
		V_{CC} = 15V		700	1400	mV

Phase Comparator State Diagrams



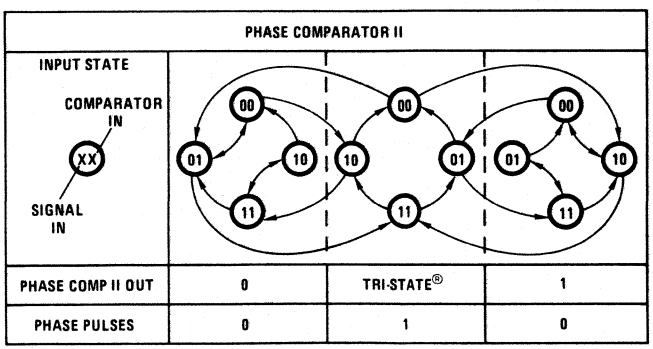


Figure 1.

Typical Waveforms

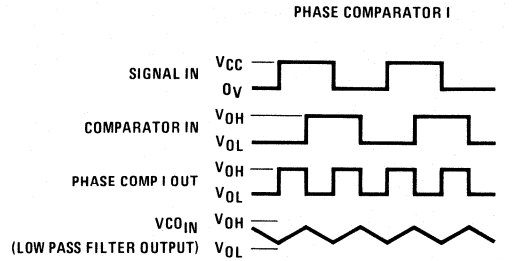


Figure 2. Typical Waveform Employing Phase Comparator I in Locked Condition

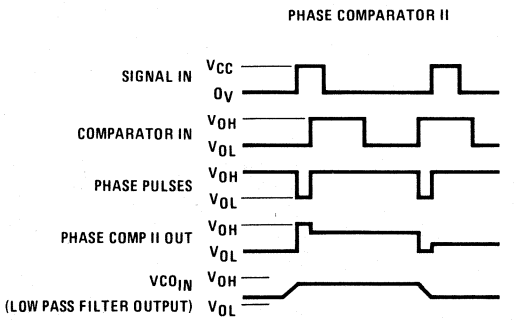
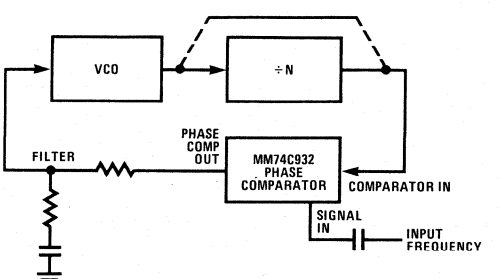


Figure 3. Typical Waveform Employing Phase Comparator II in Locked Condition

Typical Phase Locked Loop



National Semiconductor

advance information

MM54C941/MM74C941 Octal Buffers/Line Receivers/Line Drivers with TRI-STATE® Outputs

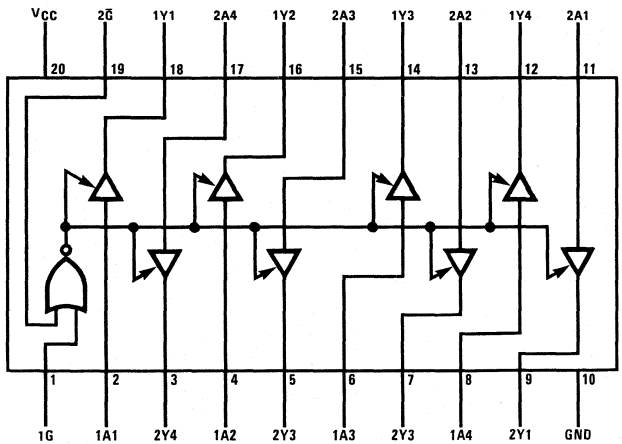
general description

These octal buffers and line drivers are monolithic complementary MOS (CMOS) integrated circuits with TRI-STATE® outputs. These outputs have been specially designed to drive highly capacitive loads such as bus-oriented systems. These devices have a fan-out of 6 low power Schottky loads.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power consumption
- TTL compatibility
- High capacitive load
- TRI-STATE® outputs
- Input protection
- 20-pin dual-in-line package

connection diagram

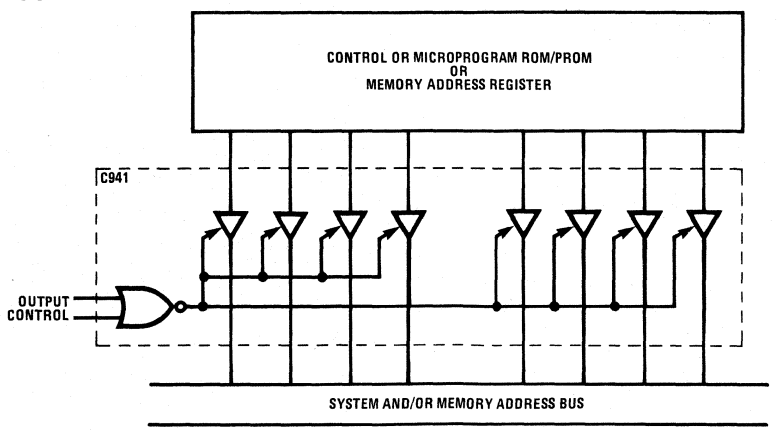


truth table

Input		Output
$1\overline{G}$	$2\overline{G}$	
0	0	1
0	0	1
0	1	X
1	0	X
1	1	X

1 = High
0 = Low
X = Don't Care
Z = TRI-STATE®

typical application



National Semiconductor

MM70C95/MM80C95, MM70C97/MM80C97 TRI-STATE® Hex Buffers
MM70C96/MM80C96, MM70C98/MM80C98 TRI-STATE® Hex Inverters

general description

These gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. The MM70C95/MM80C95 and the MM70C97/MM80C97 convert CMOS or TTL outputs to TRI-STATE outputs with no logic inversion, the MM70C96/MM80C96 and the MM70C98/MM80C98 provide the logical opposite of the input signal. The MM70C95/MM80C95 and the MM70C96/MM80C96 have common TRI-STATE controls for all six devices. The MM70C97/MM80C97 and the MM70C98/MM80C98 have two TRI-STATE controls; one for two devices and one for the other four devices.

Inputs are protected from damage due to static discharge by diode clamps to V_{CC} and GND.

features

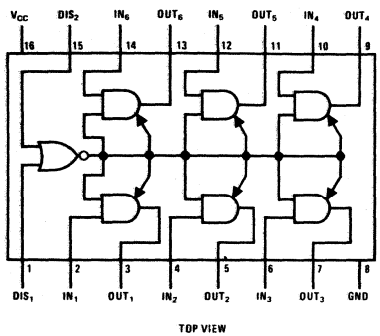
■ Wide supply voltage range	3.0V to 15V
■ Guaranteed noise margin	1.0V
■ High noise immunity	0.45 V_{CC} (typ)
■ TTL compatible	Drive 1 TTL Load

applications

■ Bus drivers	Typical propagation delay into 150 pF load is 40 ns

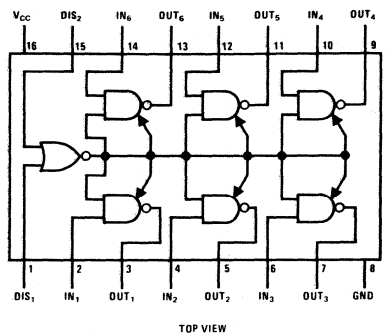
connection diagrams (Dual-In-Line and Flat Packages)

MM70C95/MM80C95



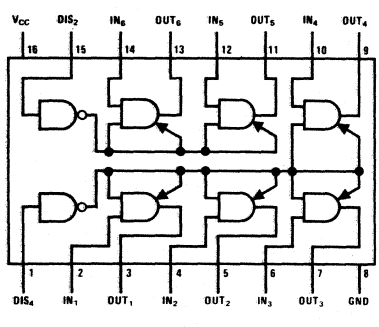
TOP VIEW

MM70C96/MM80C96



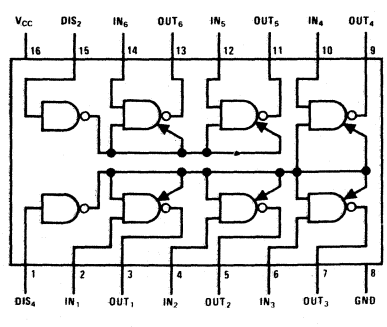
TOP VIEW

MM70C97/MM80C97



TOP VIEW

MM70C98/MM80C98



TOP VIEW

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	Input Capacitance	Any Input (Note 2)		5.0		pF
C_{OUT}	Output Capacitance TRI-STATE	Any Output (Note 2)		11.0		pF
C_{PD}	Power Dissipation Capacity	(Note 3)		60		pF
t_{pd0} t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" From Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$		60	100	ns
		$V_{CC} = 10V$		25	40	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$		70	150	ns
		$V_{CC} = 10V$		35	75	ns
t_{pd0} t_{pd1}	Propagation Delay Time to a Logical "0" or Logical "1" From Data Input to Output					
	MM70C95/MM80C95, MM70C97/MM80C97	$V_{CC} = 5V$, $C_L = 150$ pF		85	160	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		40	80	ns
	MM70C96/MM80C96, MM70C98/MM80C98	$V_{CC} = 5V$, $C_L = 150$ pF		95	210	ns
		$V_{CC} = 10V$, $C_L = 150$ pF		45	110	ns
t_{1H}, t_{0H}	Delay From Disable Input to High Impedance State, (From Logical "1" or Logical "0")	$R_L = 10k$, $C_L = 5$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		80	135	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		100	180	ns
		$V_{CC} = 10V$		70	125	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		70	125	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		90	170	ns
		$V_{CC} = 10V$		70	125	ns
t_{H1}, t_{H0}	Delay From Disable Input to Logical "1" Level (From High Impedance State)	$R_L = 10k$, $C_L = 50$ pF				
	MM70C95/MM80C95	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns
	MM70C96/MM80C96	$V_{CC} = 5V$		130	225	ns
		$V_{CC} = 10V$		60	110	ns
	MM70C97/MM80C97	$V_{CC} = 5V$		95	175	ns
		$V_{CC} = 10V$		40	80	ns
	MM70C98/MM80C98	$V_{CC} = 5V$		120	200	ns
		$V_{CC} = 10V$		50	90	ns

truth tables

MM70C95/MM80C95

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C96/MM80C96

DISABLE DIS_1	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
0	1	X	H-z
1	0	X	H-z
1	1	X	H-z

MM70C97/MM80C97

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	0
0	0	1	1
X	1	X	H-z*
1	X	X	H-z**

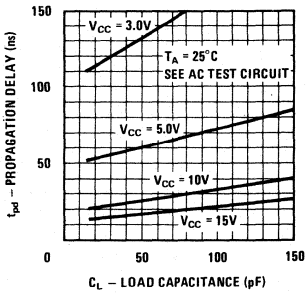
MM70C98/MM80C98

DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
0	0	0	1
0	0	1	0
X	1	X	H-z*
1	X	X	H-z**

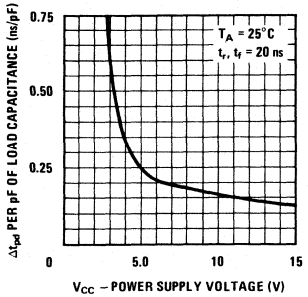
*Output 5-6 only
**Output 1-4 only
X = Irrelevant

typical performance characteristics

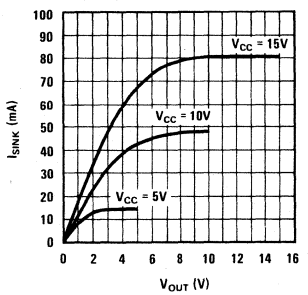
Propagation Delay vs Load Capacitance



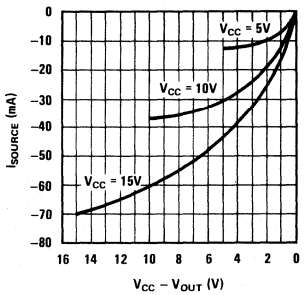
Δt_{pd}/pF vs Power Supply Voltage



N-Channel Output Drive @ 25°C

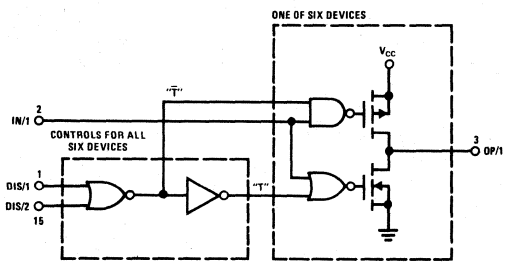


P-Channel Output Drive @ 25°C

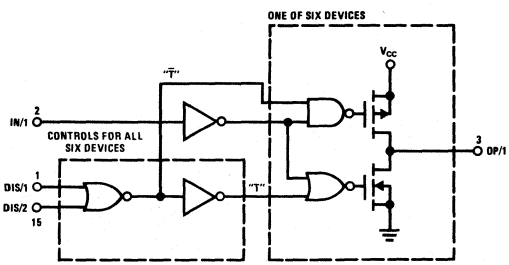


schematic diagrams

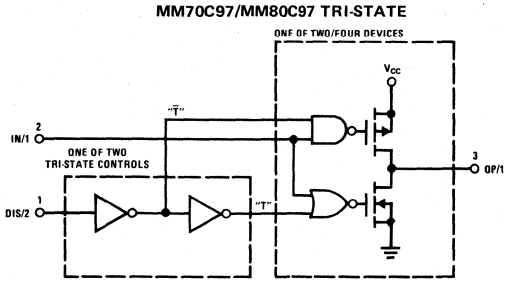
MM70C95/MM80C95 TRI-STATE



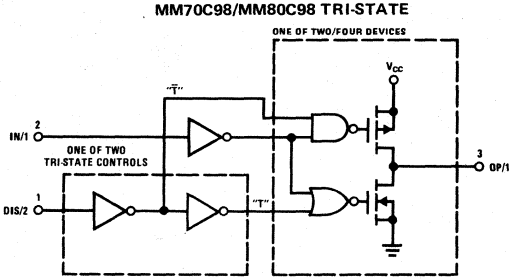
MM70C96/MM80C96 TRI-STATE



MM70C97/MM80C97 TRI-STATE

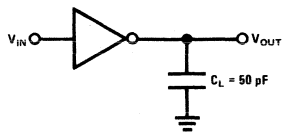


MM70C98/MM80C98 TRI-STATE

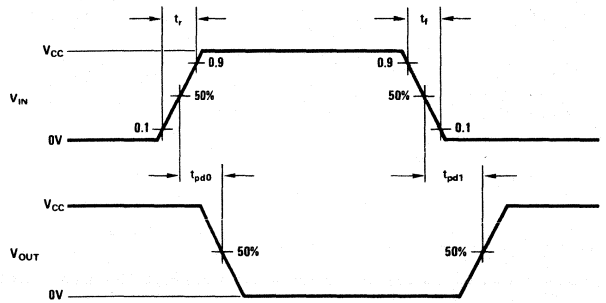


ac test circuits and switching time waveforms

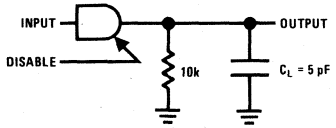
t_{pd0}, t_{pd1}



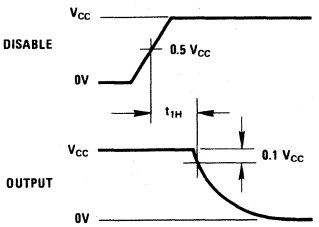
CMOS to CMOS



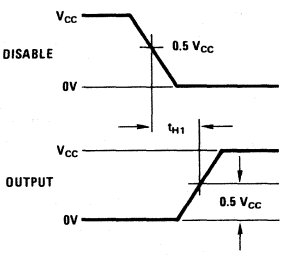
t_{1H} and t_{H1}



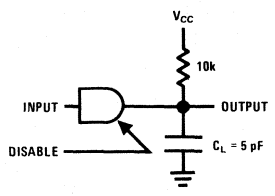
t_{1H}



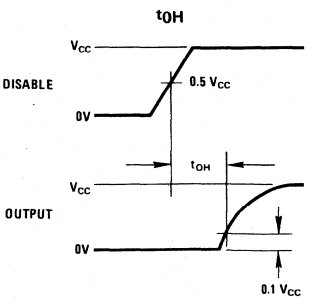
t_{H1}



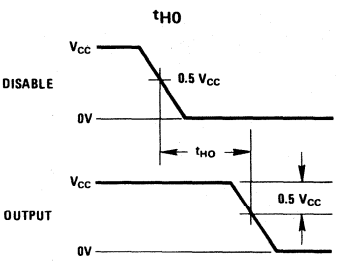
t_{0H} and t_{H0}



t_{0H}



t_{H0}



Note: Delays measured with input t_r, $t_f \leq 20$ ns

absolute maximum ratings (Note 1)

Voltage at Any Pin	0.3V to V_{CC} + 0.3V
Operating Temperature Range	
MM70CXX	−55°C to +125°C
MM80CXX	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Power Supply Voltage (V_{CC})	18V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5.0V	3.5			V
		V_{CC} = 10V	8.0			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5.0V			1.5	V
		V_{CC} = 10V			2.0	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5.0V	4.5			V
		V_{CC} = 10V	9.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5.0V			0.5	V
		V_{CC} = 10V			1.0	V
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current		−1.0	−0.005		μA
I_{OUT}	Output Current in High Impedance State	V_{CC} = 15V, V_O = 15V		0.005	1.0	μA
		V_{CC} = 15V, V_O = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.01	15	μA
TTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	MM70C V_{CC} = 4.5V	V_{CC}−1.5			V
		MM80C V_{CC} = 4.75V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	MM70C V_{CC} = 4.5V			0.8	V
		MM80C V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	MM70C V_{CC} = 4.5V, I_O = −1.6 mA	2.4			V
		MM80C V_{CC} = 4.75V, I_O = −1.6 mA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	MM70C V_{CC} = 4.5V, I_O = 1.6 mA			0.4	V
		MM80C V_{CC} = 4.75V, I_O = 1.6 mA			0.4	V
OUTPUT DRIVE CURRENT						
I_{SOURCE}	Output Source Current	V_{CC} = 5.0V, $V_{IN(1)}$ = 5.0V T_A = 25°C, V_{OUT} = 0V	−4.35			mA
I_{SOURCE}	Output Source Current	V_{CC} = 10V, $V_{IN(1)}$ = 10V T_A = 25°C, V_{OUT} = 0V	−20			mA
I_{SINK}	Output Sink Current	V_{CC} = 5.0V, $V_{IN(0)}$ = 0V T_A = 25°C. V_{OUT} = V_{CC}	4.35			mA
I_{SINK}	Output Sink Current	V_{CC} = 10V, V_{IN} = 0V T_A = 25°C, V_{OUT} = V_{CC}	20			mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

MM78C29/MM88C29 Quad Single-Ended Line Driver
MM78C30/MM88C30 Dual Differential Line Driver

general description

The MM78C30/MM88C30 is a dual differential line driver that also performs the dual four-input NAND or dual four-input AND function. The absence of a clamp diode to V_{CC} in the input protection circuitry of the MM78C30/MM88C30 allows a CMOS user to interface systems operating at different voltage levels. Thus, a CMOS digital signal source can operate at a V_{CC} voltage greater than the V_{CC} voltage of the MM78C30 line driver. The differential output of the MM78C30/MM88C30 eliminates ground-loop errors.

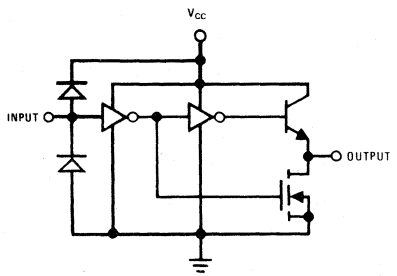
The MM78C29/MM88C29 is a non-inverting single-wire transmission line driver with a similar input protection circuit. And since the output ON resistance is a low 20Ω typ, the device can be used to drive lamps, relays, solenoids, and clock lines, besides driving data lines.

features

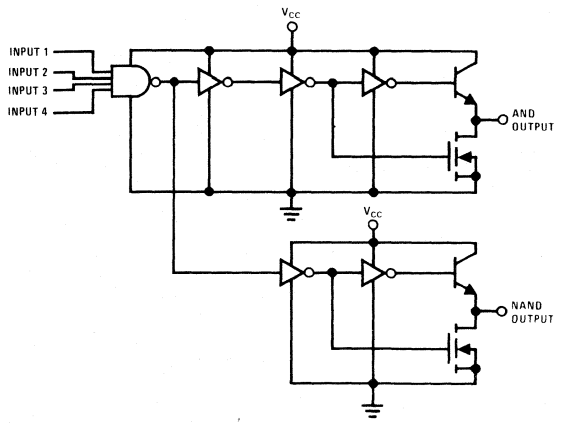
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ
■ Low output ON resistance	20Ω typ

logic and connection diagrams

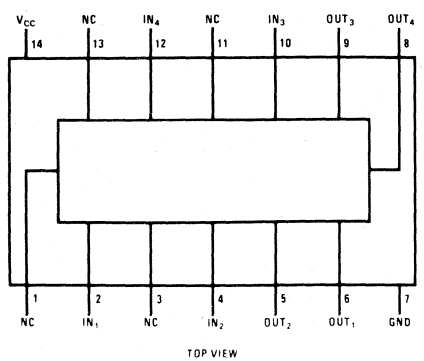
1/4 MM78C29/MM88C29



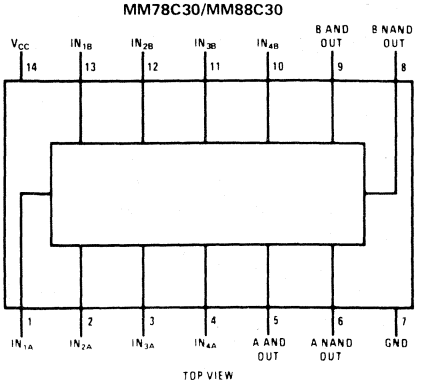
1/2 MM78C30/MM88C30



MM78C29/MM88C29



MM78C30/MM88C30



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to +16V	Absolute Maximum V_{CC}	18V
Operating Temperature Range		Average Current at V_{CC} and Ground	100 mA
MM78C29/MM78C30	−55°C to +125°C	Average Current at Output	
MM88C29/MM88C30	−40°C to +85°C	MM78C30/MM88C30	50 mA
Storage Temperature Range	−65°C to +150°C	MM78C29/MM88C29	25 mA
Package Dissipation	500 mW	Maximum Junction Temperature, T_j	150°C
Operating V_{CC} Range	3.0V to 15V	Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics Min/max limits apply across temperature range, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
CMOS TO CMOS					
Logical "1" Input Voltage ($V_{IN(1)}$)	V_{CC} = 5.0V	3.5			V
	V_{CC} = 10V	8.0			V
Logical "0" Input Voltage ($V_{IN(0)}$)	V_{CC} = 5.0V			1.5	V
	V_{CC} = 10V			2.0	V
Logical "1" Input Current ($I_{IN(1)}$)	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
Logical "0" Input Current ($I_{IN(0)}$)	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
Supply Current (I_{CC})	V_{CC} = 15V		0.05	100	μA
OUTPUT DRIVE					
Output Source Current					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.5V, T_j = 25°C	−57	−80		mA
	T_j = 125°C	−32	−50		mA
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.75V, T_j = 25°C	−47	−80		mA
	T_j = 85°C	−32	−60		mA
MM78C29/MM88C29	V_{OUT} = V_{CC} −0.8V				
MM78C30/MM88C30	$V_{CC} \geq$ 4.5V	−2	−20		mA
Output Sink Current					
MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.50V				mA
	T_j = 25°C	11	20		mA
	T_j = 125°C	8	14		
	V_{OUT} = 0.4V, V_{CC} = 10V				mA
	T_j = 25°C	22	40		mA
	T_j = 125°C	16	28		
MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V				
	T_j = 25°C	9.5	22		mA
	T_j = 85°C	8	18		mA
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C	19	40		mA
	T_j = 85°C	15.5	33		mA
Output Source Resistance					
MM78C29/MM78C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.5V, T_j = 25°C		20	28	Ω
	T_j = 125°C		32	50	Ω
MM88C29/MM88C30	V_{OUT} = V_{CC} −1.6V,				
	$V_{CC} \geq$ 4.75V, T_j = 25°C		20	34	Ω
	T_j = 85°C		27	50	Ω

dc electrical characteristics (con't)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Sink Resistance					
MM78C29/MM78C30	V_{OUT} = 0.4V, V_{CC} = 4.5V				
	T_j = 25°C		20	36	Ω
	T_j = 125°C		28	50	Ω
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C		10	18	Ω
	T_j = 125°C		14	25	Ω
MM88C29/MM88C30	V_{OUT} = 0.4V, V_{CC} = 4.75V				
	T_j = 25°C		18	41	Ω
	T_j = 85°C		22	50	Ω
	V_{OUT} = 0.4V, V_{CC} = 10V				
	T_j = 25°C		10	21	Ω
	T_j = 85°C		12	26	Ω
Output Resistance Temperature Coefficient					
Source			0.55		%/°C
Sink			0.40		%/°C
Thermal Resistance, θ_{jA}					
MM78C29/MM78C30 (D-Package)			100		°C/W
MM88C29/MM88C30 (N-Package)			150		°C/W

ac electrical characteristics T_A = 25°C, C_L = 50 pF

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time to Logical "1" or "0" (t_{pd})	*(See Figure 2)*				
MM78C29/MM88C29	V_{CC} = 5V		80	200	ns
	V_{CC} = 10V		35	100	ns
MM78C30/MM88C30	V_{CC} = 5V		110	350	ns
	V_{CC} = 10V		50	150	ns
Power Dissipation Capacitance (C_{PD})					
MM78C29/MM88C29	(Note 3)		150		pF
MM78C30/MM88C30	(Note 3)		200		pF
Input Capacitance (C_{IN})					
MM78C29/MM88C29	(Note 2)		5.0		pF
MM78C30/MM88C30	(Note 2)		5.0		pF
Differential Propagation Delay Time to Logical "1" or "0"	R_L = 100Ω, C_L = 5000 pF *(See Figure 1)*				
MM78C30/MM88C30	V_{CC} = 5V			400	ns
	V_{CC} = 10V			150	ns

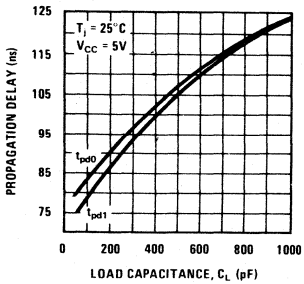
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

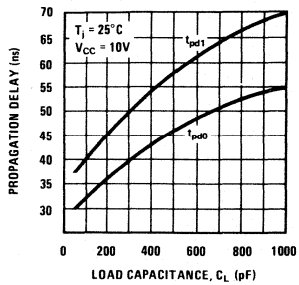
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

typical performance characteristics

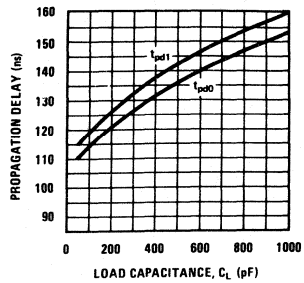
MM78C29/MM88C29
Typical Propagation Delay vs
Load Capacitance



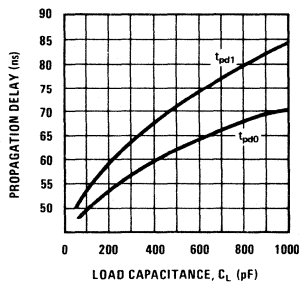
MM78C29/MM88C29
Typical Propagation Delay vs
Load Capacitance



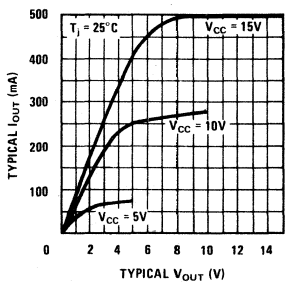
MM78C30/MM88C30
Typical Propagation Delay vs
Load Capacitance



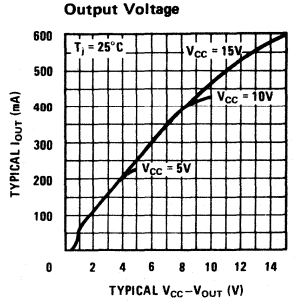
MM78C30/MM88C30
Typical Propagation Delay vs
Load Capacitance



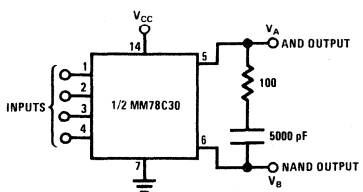
Typical Sink Current vs
Output Voltage



Typical Source Current vs
Output Voltage



ac test circuits



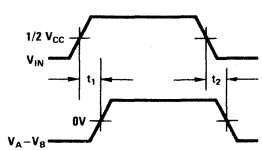
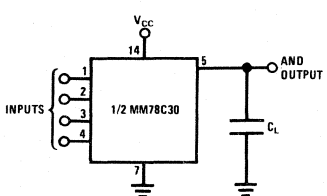


FIGURE 1.



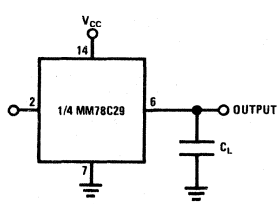
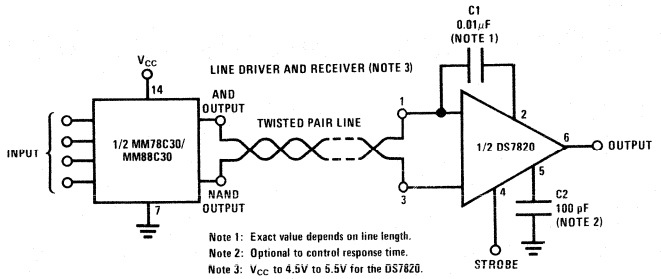


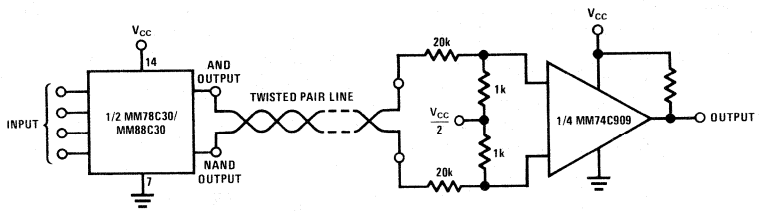
FIGURE 2.

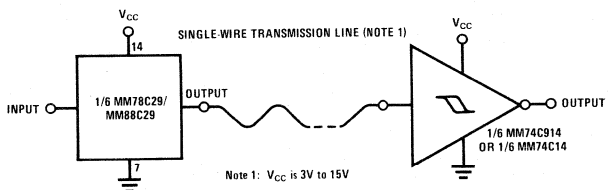
typical applications

Digital Data Transmission



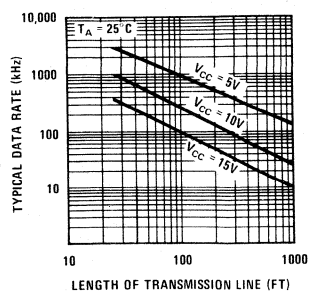
Note 1: Exact value depends on line length.
Note 2: Optional to control response time.
Note 3: V_{CC} to 4.5V to 5.5V for the DS7820.





Note 1: V_{CC} is 3V to 15V

Typical Data Rate vs Transmission Line Length



Note 1: The transmission line used was #22 gauge unshielded twisted pair (40k termination).

Note 2: The curves generated assume that both drivers are driving equal lines, and that the maximum power is 500 mW/package.

National Semiconductor

ADC0816/ADC0817 Single Chip Data Acquisition System

General Description

The ADC0816, ADC0817 (MM74C948) data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, a 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16 single-ended analog signals and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the input of the 8-bit A/D converter.

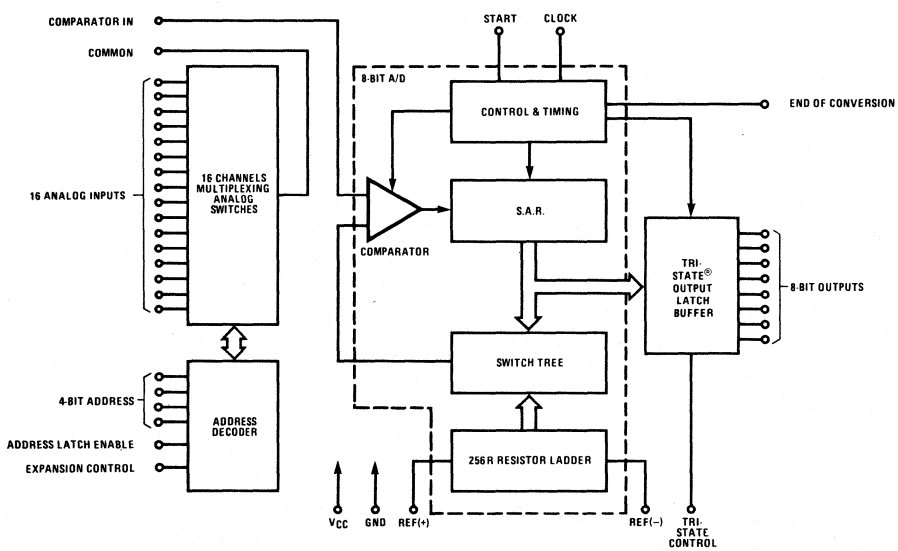
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy $\leq$ 1 LSB including quantitizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control.

Features

- Total unadjusted error $<$ ±1/2 LSB
- Linearity error $<$ ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW

Block Diagram



Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Control Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Control Inputs (Start, TRI-STATE, Clock, ALE, ADD A, ADD B, ADD C, ADD D, Expansion Control)	−0.3V to + 15V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (at 25°C)	500 mW
Operating V_{CC} Range	4.5V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C unless otherwise noted, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	Clock Frequency = 500 kHz		300	1000	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V			3	μA
		V_O = 0	−3			μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic, *(Figure 2)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 2)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage, *(Figure 2)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors, *(Figure 3)*.

Note 7: Quantization error is the ±1/2 LSB uncertainty caused by the converter's finite resolution, *(Figure 3)*.

Note 8: Absolute Accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance, *(Figure 3)*.

Note 9: Supply rejection relates to the ability of an ADC to maintain accuracy as the supply voltage varies. The supply and $V_{REF(+)}$ are varied together and the change in accuracy is measured with respect to full-scale.

Note 10: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence, *(Figure 5)*.

DC Electrical Characteristics (Continued)

ANALOG MULTIPLEXER

ADC0816, ADC0817 $-40°C \leq T_A \leq +85°C$ unless otherwise noted

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
R_{ON}	Analog Multiplexer ON Resistance	(Any Selected Channel) $T_A = 25°C$, $R_L = 10k$		1.5	3 6	kΩ kΩ
ΔR_{ON}	Δ ON Resistance Between Any 2 Channels	(Any Selected Channel) $R_L = 10k$		75		Ω
$I_{OFF(+)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 5V$, $T_A = 25°C$		10	200	nA
$I_{OFF(-)}$	OFF Channel Leakage Current	$V_{CC} = 5V$, $V_{IN} = 0$, $T_A = 25°C$	−200	−10		nA

CONVERTER SECTION

$V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$, $V_{IN} = V_{COMPARATOR\ IN}$, $f_c = 640$ kHz

ADC0816CCN $-40°C \leq T_A \leq +85°C$ unless otherwise noted

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/4	±1/2	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	$T_A = 25°C$		±1/4	±1/2	LSB
	(Note 6)		±1/4	±3/4	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	$T_A = 25°C$		±3/4	±1	LSB
	(Note 8)		±3/4	±1 1/4	LSB

ADC0817CCN $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution		8			Bits
Non-Linearity	(Note 3)		±1/2	±1	LSB
Zero Error	(Note 4)		±1/4	±1/2	LSB
Full-Scale Error	(Note 5)		±1/4	±1/2	LSB
Total Unadjusted Error	(Note 6)		±1/2	±1	LSB
Quantization Error	(Note 7)			±1/2	LSB
Absolute Accuracy	(Note 8)		±1	±1 1/2	LSB

ADC0816CCN $-40°C \leq T_A \leq +85°C$
ADC0817CCN $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Rejection	$4.75V \leq V_{CC} = V_{REF(+)} \leq 5.25V$, (Note 9)		0.05	0.15	%/V
Comparator Input Current	$f_c = 640$ kHz, (Note 10)	−2	±0.5	2	μA
Ladder Resistance	From Ref(+) to Ref(−)	1	4.5		kΩ

DC Electrical Characteristics (Continued)

DESIGN GUIDELINES

ADC0816CCN, ADC0817CCN

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{LAD}	Voltage Across Ladder	From Ref(+) to Ref(−)	0.512	5.12	5.25	V
$V_{REF(+)}$	Voltage, Top of Ladder	Measured at Ref(+)		V_{CC}	V_{CC}+0.1	V
$\frac{V_{REF(+)} + V_{REF(-)}}{2}$	Voltage, Center of Ladder	Measured at $R_{LADDER}/2$	$\frac{V_{CC}}{2}$−0.1	$\frac{V_{CC}}{2}$	$\frac{V_{CC}}{2}$+0.1	V
$V_{REF(-)}$	Voltage, Bottom of Ladder	Measured at Ref(−)	−0.1	0		V

AC Electrical Characteristics

ADC0816CCN, ADC0817CCN $T_A = 25°C$, $V_{CC} = V_{REF(+)} = 5V$, $V_{REF(-)} = GND$

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{WS}	Start Pulse Width	*(Figure 5)*	200	100		ns
t_{WALE}	Minimum ALE Pulse Width	*(Figure 5)*	200	100		ns
t_s	Address Set-Up Time	*(Figure 5)*	50	25		ns
t_H	Address Hold Time	*(Figure 5)*	50	25		ns
t_D	Analog MUX Delay Time From ALE	Common Tied to Comparator In, $R_S + R_{ON} \leq 5\ k\Omega$, $C_L = 10\ pF$		1	2.5	μs
t_{H1}, t_{H0}	TRI-STATE Control to Q Logic State	$C_L = 50\ pF$		125	250	ns
t_{1H}, t_{0H}	TRI-STATE Control to Hi-Z	$C_L = 10\ pF$, $R_L = 10k$		125	250	ns
t_C	Conversion Time	$f_C = 640\ kHz$, *(Figure 5)*	90	100	114	μs
f_C	Clock Frequency		10	640	1200	kHz
t_{EOC}	EOC Delay Time	*(Figure 5)*	1		8	Clock Periods
C_{IN}	Input Capacitance	At Control Inputs At MUX Inputs		10 5	15 7.5	pF pF
C_{OUT}	TRI-STATE Output Capacitance	At TRI-STATE Outputs, (Note 11)		5	7.5	pF

Note 11: Capacitance guaranteed by periodic testing.

Note 12: The outputs of the data register are updated one clock cycle before the rising edge of EOC.

Timing Diagram

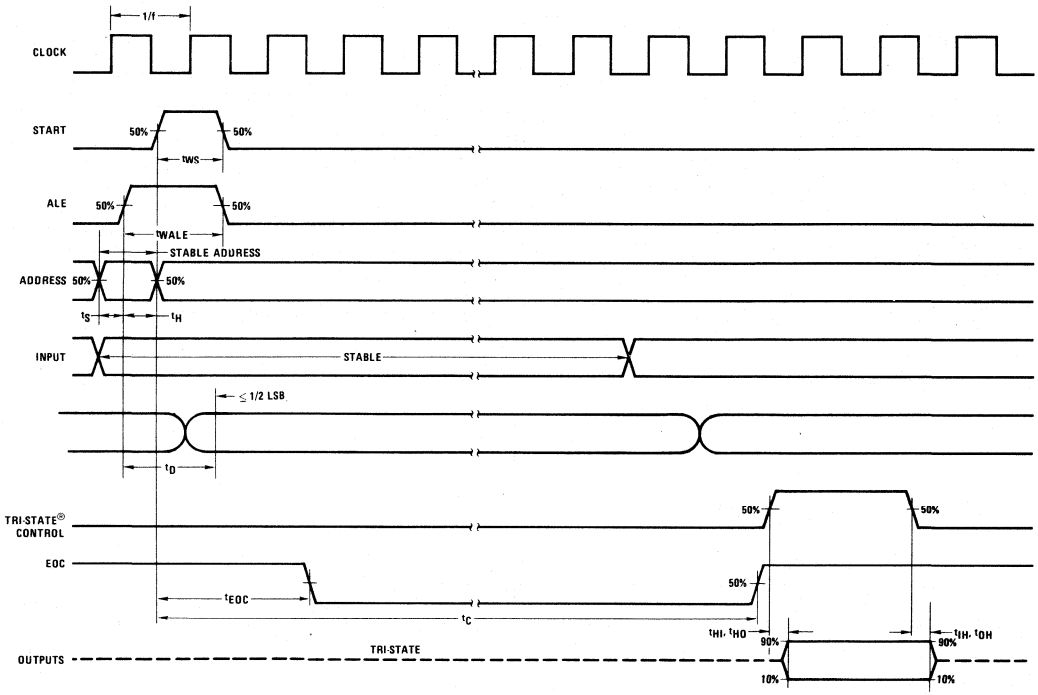


FIGURE 5

Typical Performance Characteristics

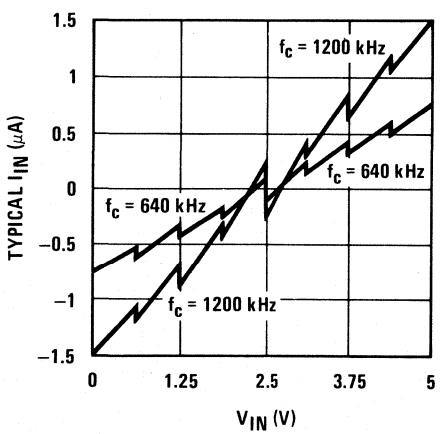


FIGURE 6. Comparator I_{IN} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

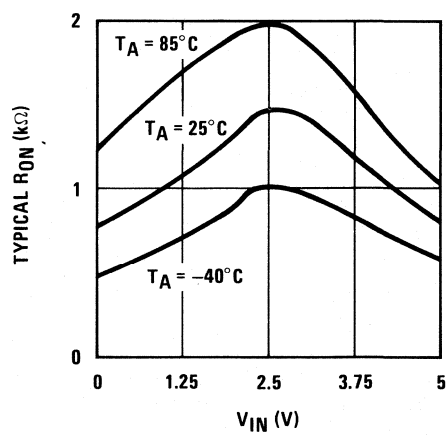


FIGURE 7. Multiplexer R_{ON} vs V_{IN} ($V_{CC} = V_{REF} = 5V$)

Functional Description

Multiplexer: The device contains a 16-channel single-ended analog signal multiplexer. A particular input channel is selected by using the address decoder. Table I shows the input states for the address line and the expansion control line to select any channel. The address is latched into the decoder on the low-to-high transition of the address latch enable signal.

Additional single-ended analog signals can be multiplexed to the A/D converter by disabling all the multiplexer inputs. The additional external signals are connected to the comparator input and the device ground. Additional signal conditioning (i.e., prescaling, sample and hold, instrumentation amplification, etc.) may also be added between the analog input signal and the comparator input.

TABLE I

SELECTED ANALOG CHANNEL	ADDRESS LINE				EXPANSION CONTROL
	D	C	B	A	
IN0	L	L	L	L	H
IN1	L	L	L	H	H
IN2	L	L	H	L	H
IN3	L	L	H	H	H
IN4	L	H	L	L	H
IN5	L	H	L	H	H
IN6	L	H	H	L	H
IN7	L	H	H	H	H
IN8	H	L	L	L	H
IN9	H	L	L	H	H
IN10	H	L	H	L	H
IN11	H	L	H	H	H
IN12	H	H	L	L	H
IN13	H	H	L	H	H
IN14	H	H	H	L	H
IN15	H	H	H	H	H
All Channels OFF	X	X	X	X	L

X = don't care

CONVERTER CHARACTERISTICS

The Converter

The heart of this single chip data acquisition system is its 8-bit analog-to-digital converter. The converter is designed to give fast, accurate, and repeatable conversions over a wide range of temperatures. The converter is partitioned into 3 major sections: the 256R ladder network, the successive approximation register, and the comparator. The converter's digital outputs are positive true.

The 256R ladder network approach *(Figure 1)* was chosen over the conventional R/2R ladder because of its inherent monotonicity, which guarantees no missing digital codes. Monotonicity is particularly important in closed loop feedback control systems. A non-monotonic relationship can cause oscillations that will be catastrophic for the system. Additionally, the 256R network does not cause load variations on the reference voltage.

The bottom resistor and the top resistor of the ladder network in *Figure 1* are not the same value as the remainder of the network. The difference in these resistors causes the output characteristic to be symmetrical with the zero and full-scale points of the transfer curve. The first output transition occurs when the analog signal has reached +1/2 LSB and succeeding output transitions occur every 1 LSB later up to full-scale.

The successive approximation register (SAR) performs 8 iterations to approximate the input voltage. For any SAR type converter, n-iterations are required for an n-bit converter. *Figure 2* shows a typical example of a 3-bit converter. In the ADC0816, ADC0817, the approximation technique is extended to 8 bits using the 256R network.

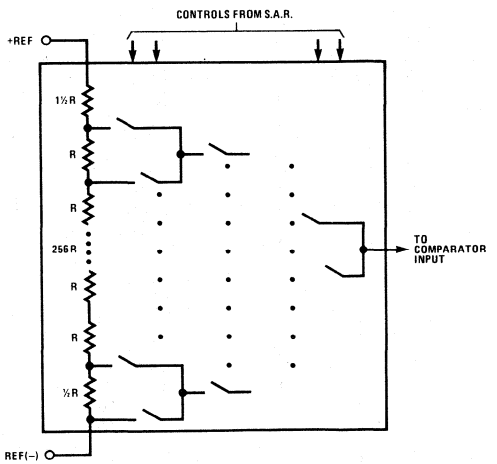


FIGURE 1. Resistor Ladder and Switch Tree

Functional Description (Continued)

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start conversion (SC) pulse. The conversion is begun on the falling edge of the start conversion pulse. A conversion in process will be interrupted by receipt of a new start conversion pulse. Continuous conversion may be accomplished by tying the end-of-conversion (EOC) output to the SC input. If used in this mode, an external start conversion pulse should be applied after power up. End-of-conversion will go low between 1 and 8 clock pulses after the rising edge of start conversion.

The most important section of the A/D converter is the comparator. It is this section which is responsible for the ultimate accuracy of the entire converter. It is also the comparator drift which has the greatest influence on the repeatability of the device. A chopper-stabilized comparator provides the most effective method of satisfying all the converter requirements.

The chopper-stabilized comparator converts the DC input signal into an AC signal. This signal is then fed through a high gain AC amplifier and has the DC level restored. This technique limits the drift component of the amplifier since the drift is a DC component which is not passed by the AC amplifier. This makes the entire A/D converter extremely insensitive to temperature, long term drift and input offset errors.

Figure 4 shows a typical error curve for the ADC0816 as measured using the procedures outlined in AN-179. The characteristic is generated with the analog input signal applied to the comparator input.

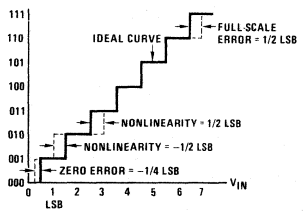


FIGURE 2. 3-Bit A/D Transfer Curve

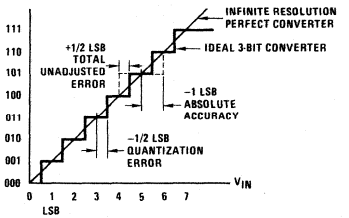


FIGURE 3. 3-Bit A/D Absolute Accuracy Curve

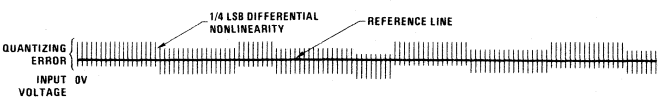
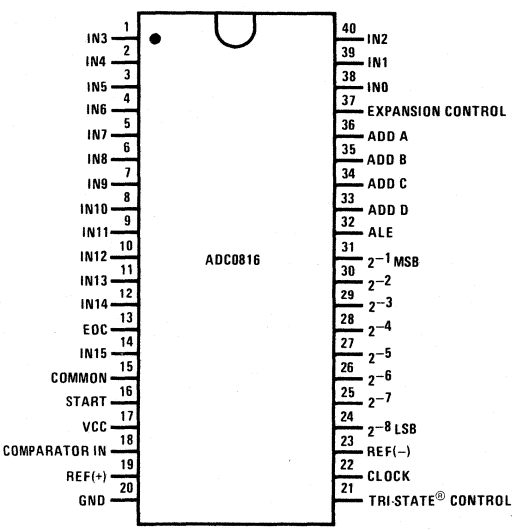


FIGURE 4. Typical Error Curve

Connection Diagram

Dual-In-Line Package



TOP VIEW

Applications Information

OPERATION

Ratiometric Conversion

The ADC0816, ADC0817 is designed as a complete Data Acquisition System (DAS) for ratiometric conversion systems. In ratiometric systems, the physical variable being measured is expressed as a percentage of full-scale which is not necessarily related to an absolute standard. The voltage input to the ADC0816 is expressed by the equation

$$\frac{V_{IN}}{V_{fs} - V_z} = \frac{D_X}{D_{MAX} - D_{MIN}} \quad (1)$$

V_{IN} = Input voltage into the ADC0816
V_{fs} = Full-scale voltage
V_z = Zero voltage
D_X = Data point being measured
D_{MAX} = Maximum data limit
D_{MIN} = Minimum data limit

A good example of a ratiometric transducer is a potentiometer used as a position sensor. The position of the wiper is directly proportional to the output voltage which is a ratio of the full-scale voltage across it. Since the data is represented as a proportion of full-scale, reference requirements are greatly reduced, eliminating a large source of error and cost for many applications. A major advantage of the ADC0816, ADC0817 is that the input voltage range is equal to the supply range so the transducers can be connected directly across the supply and their outputs connected directly into the multiplexer inputs, *(Figure 8)*.

Ratiometric transducers such as potentiometers, strain gauges, thermistor bridges, pressure transducers, etc., are suitable for measuring proportional relationships; however, many types of measurements must be referred to an absolute standard such as voltage or current. This means a system reference must be used which relates the full-scale voltage to the standard volt. For example, if $V_{CC} = V_{REF} = 5.12V$, then the full-scale range is divided into 256 standard steps. The smallest standard step is 1 LSB which is then 20 mV.

Resistor Ladder Limitations

The voltages from the resistor ladder are compared to the selected input 8 times in a conversion. These voltages are coupled to the comparator via an analog switch tree which is referenced to the supply. The voltages at the top, center and bottom of the ladder must be controlled to maintain proper operation.

The top of the ladder, Ref(+), should not be more positive than the supply, and the bottom of the ladder Ref(−) should not be more negative than ground. The center of the ladder voltage must also be near the center of the supply because the analog switch tree changes from N-channel switches to P-channel switches. These limitations are automatically satisfied in ratiometric systems and can be easily met in ground referenced systems.

Figure 9 shows a ground referenced system with a separate supply and reference. In this system, the supply must be trimmed to match the reference voltage. For instance, if a 5.12V reference is used, the supply should be adjusted to the same voltage within 0.1V.

The ADC0816 needs less than a milliamp of supply current so developing the supply from the reference is readily accomplished. In *Figure 10* a ground referenced system is shown which generates the supply from the reference. The buffer shown can be an op amp of sufficient drive to supply the milliamp of supply current and the desired bus drive, or if a capacitive bus is driven by the outputs a large capacitor will supply the transient supply current as seen in *Figure 11*. The LM301 is overcompensated to insure stability when loaded by the 10 μF output capacitor.

The top and bottom ladder voltages cannot exceed V_{CC} and ground, respectively, but they can be symmetrically less than V_{CC} and greater than ground. The center of the ladder voltage should always be near the center of the supply. The sensitivity of the converter can be increased, (i.e., size of the LSB steps decreased) by using a symmetrical reference system. In *Figure 12*, a 2.5V reference is symmetrically centered about $V_{CC}/2$ since the same current flows in identical resistors. This system with a 2.5V reference allows the LSB bit to be half the size of a 5V reference system.

Converter Equations

The transition between adjacent codes N and N + 1 is given by:

$$V_{IN} = V_{REF(+)} \left[\frac{N}{256} + \frac{1}{512} \right] \pm V_{TUE} \quad (2)$$

The center of an output code N is given by:

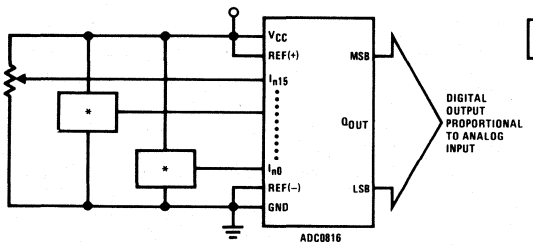
$$V_{IN} = V_{REF(+)} \left[\frac{N}{256} \right] \pm V_{TUE} \quad (3)$$

The output code N for an arbitrary input are the integers within the range:

$$N = \frac{V_{IN}}{V_{REF(+)}} \times 256 \pm \text{Absolute Accuracy} \quad (4)$$

where: V_{IN} = Voltage at comparator input
$V_{REF(+)}$ = Voltage at Ref(+)
$V_{REF(-)}$ = GND
V_{TUE} = Total unadjusted error voltage(typically $V_{REF(+)}/512$)

Applications Information (Continued)

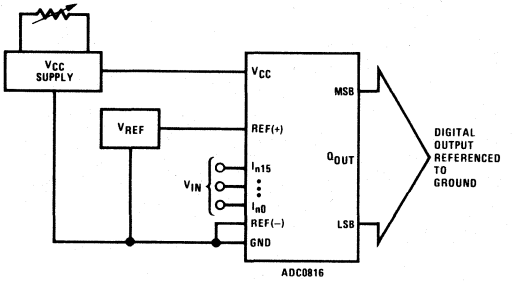


$$D_{OUT} = \frac{V_{IN}}{V_{REF}} = \frac{V_{IN}}{V_{CC}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

*Ratiometric transducers

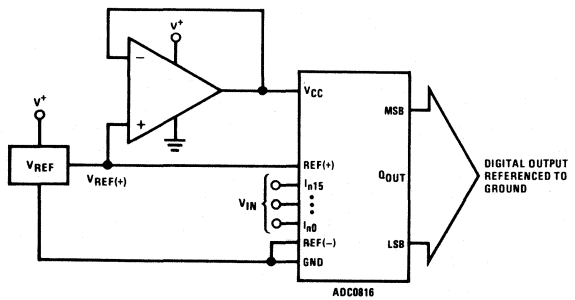
FIGURE 8. Ratiometric Conversion System



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 9. Ground Referenced Conversion System Using Trimmed Supply



$$D_{OUT} = \frac{V_{IN}}{V_{REF}}$$

$4.75V \leq V_{CC} = V_{REF} \leq 5.25V$

FIGURE 10. Ground Referenced Conversion System with Reference Generating V_{CC} Supply

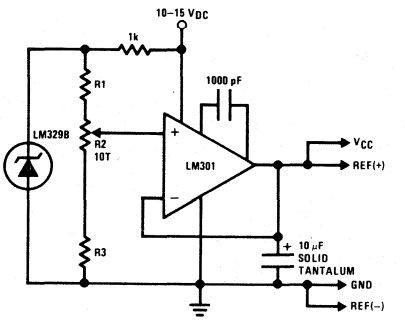
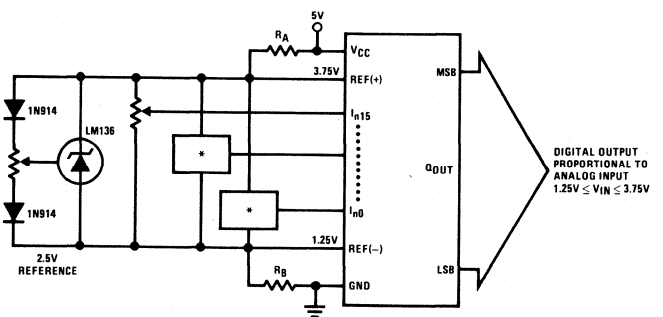


FIGURE 11. Typical Reference and Supply Circuit

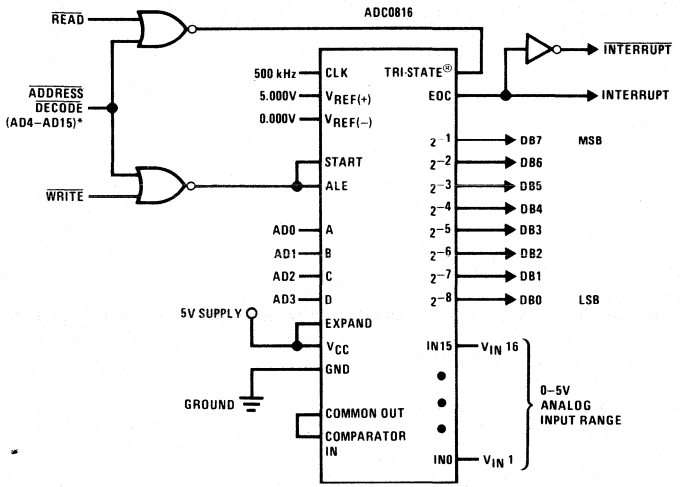


$R_A = R_B$

*Ratiometric transducers

FIGURE 12. Symmetrically Centered Reference

Typical Application



*Address latches needed for 8085 and SC/MP interfacing the ADC0816 to a microprocessor

MICROPROCESSOR INTERFACE TABLE

PROCESSOR	$\overline{\text{READ}}$	$\overline{\text{WRITE}}$	INTERRUPT (COMMENT)
8080	$\overline{\text{MEMR}}$	$\overline{\text{MEMW}}$	INTR (Thru RST Circuit)
8085	$\overline{\text{RD}}$	$\overline{\text{WR}}$	INTR (Thru RST Circuit)
Z–80	$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{INT}}$ (Thru RST Circuit, Mode 0)
SC/MP	NRDS	NWDS	SA (Thru Sense A)
6800	VMA · ϕ2 · R/W	VMA · ϕ2 · $\overline{\text{R/W}}$	$\overline{\text{IRQA}}$ or $\overline{\text{IRQB}}$ (Thru PIA)

National Semiconductor

ADD3501 3½ Digit DVM with Multiplexed 7-Segment Output

general description

The ADD3501 (MM74C935-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3501 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or –OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included on all 4 versions of this product.

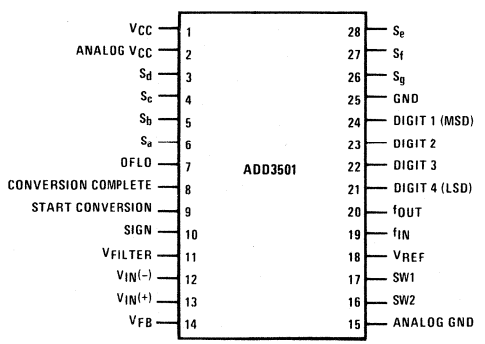
features

- Operates from single 5V supply
- Converts 0V to ±1.999V
- Multiplexed 7-segment
- Drives segments directly
- No external precision component necessary
- Accuracy specified over temperature
- Medium speed – 200ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or –OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

connection diagram



absolute maximum rating (Note 1)

Voltage at Any Pin	$-0.3V$ to $V_{CC} + 0.3V$
Operating Temperature Range (T_A)	$-40°C$ to $+85°C$
Package Dissipation at $T_A = 25°C$	800mW
derate at $\theta_{JA(MAX)} = 125°C/Watt$ above $T_A = 25°C$	
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	$-65°C$ to $+150°C$

electrical characteristics $4.75V \leqslant V_{CC} \leqslant 5.25V$, $-40°C \leqslant T_A \leqslant +85°C$, unless otherwise specified.

ADD3501

PARAMETER		CONDITIONS	MIN	TYP (2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage		$V_{CC}-1.5$			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs except Digit Outputs)	$I_O = 1.1$ mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	$I_O = 0.7$ mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	$I_O = 50$ mA @ $T_J = 25°C$ $V_{CC} = 5V$ $I_O = 30$ mA @ $T_J = 100°C$	$V_{CC}-1.6$ $V_{CC}-1.6$	$V_{CC}-1.3$ $V_{CC}-1.3$		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs except Segment Outputs)	$I_O = 500\mu A$ (Digit Outputs) $I_O = 360\mu A$ (Conv. Complete, +/–, Oflo Outputs)	$V_{CC}-0.4$			V
I_{SOURCE}	Output Source Current (Digit Outputs)	$V_{OUT} = 1.0V$	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	$V_{IN} = 1.5V$			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	$V_{IN} = 0V$	–1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			$f_{IN}/64,512$		conv./sec
f_{MUX}	Digit Mux Rate			$f_{IN}/256$		Hz
t_{BLANK}	Inter Digit Blanking Time			$1/(32f_{MUX})$		sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

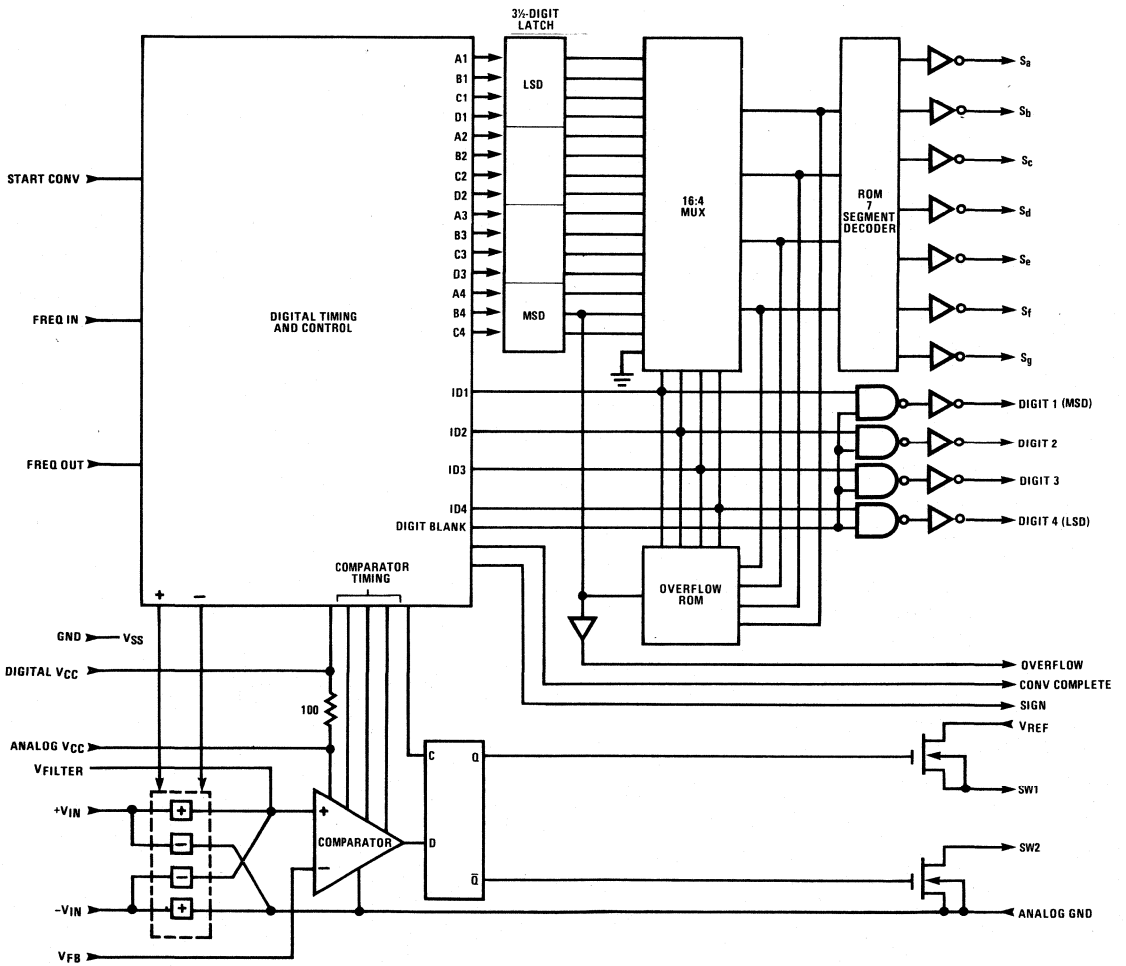
Note 2: All typicals given for $T_A = 25°C$.

electrical characteristics ADD3501

t_C = 5 conversions/second, 0°C ≤ T_A ≤ 70°C, unless otherwise specified.

Non-Linearity	V_{IN} = 0 - 2V Full Scale V_{IN} = 0 - 200mV Full Scale	-0.05	±0.025	+0.05	% of full scale
Quantization Error		-1		+0	counts
Offset Error, V_{IN} = 0V		-0.5	+1.5	+3	mV
Rollover Error		-0		+0	counts
Analog Input Current (V_{IN}+, V_{IN}-)	T_A = 25°C	-5	±0.5	+5	nA

block diagram



ADD3501 3½-Digit DVM Block Diagram

theory of operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time V_{FB} will start discharging toward 0V with a time constant R_1C_1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\left(\frac{T_{ON}}{T_{ON} + T_{OFF}}\right) = V_{REF}(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

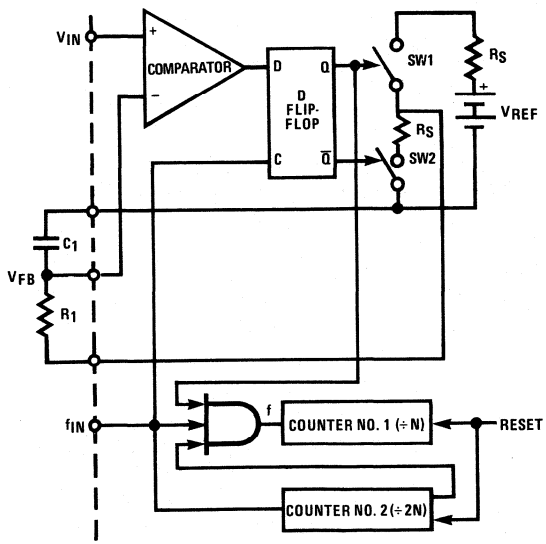
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3501, N = 2000.

schematic diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic
Pulse Modulation A/D Converter

general information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 64,512 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADD3501 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ and the minimum time is 256 x $1/f_{IN}$.

timing waveforms

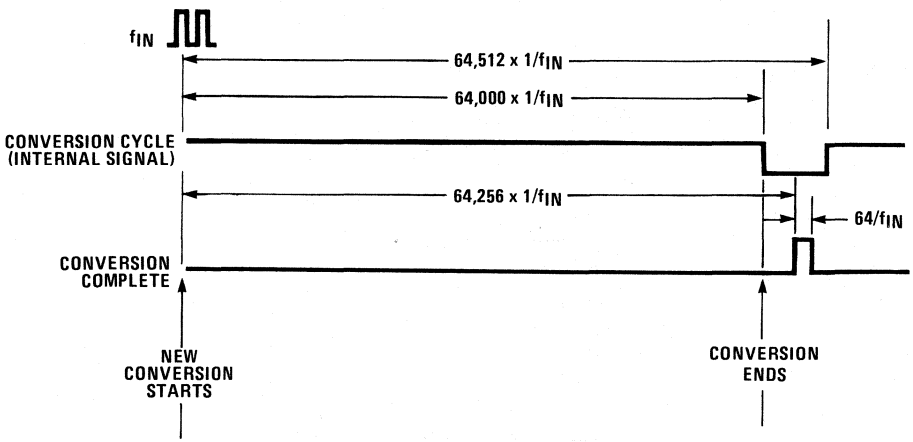


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

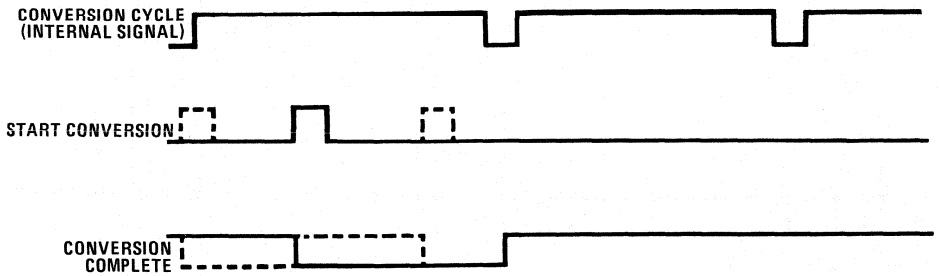


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3501 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3501 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators both function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it. The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0V to 1.999V operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 6.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0nA of leakage current will cause 0.1mV error ($1.0 \times 10^{-9}A \times 100k\Omega = 0.1mV$). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.

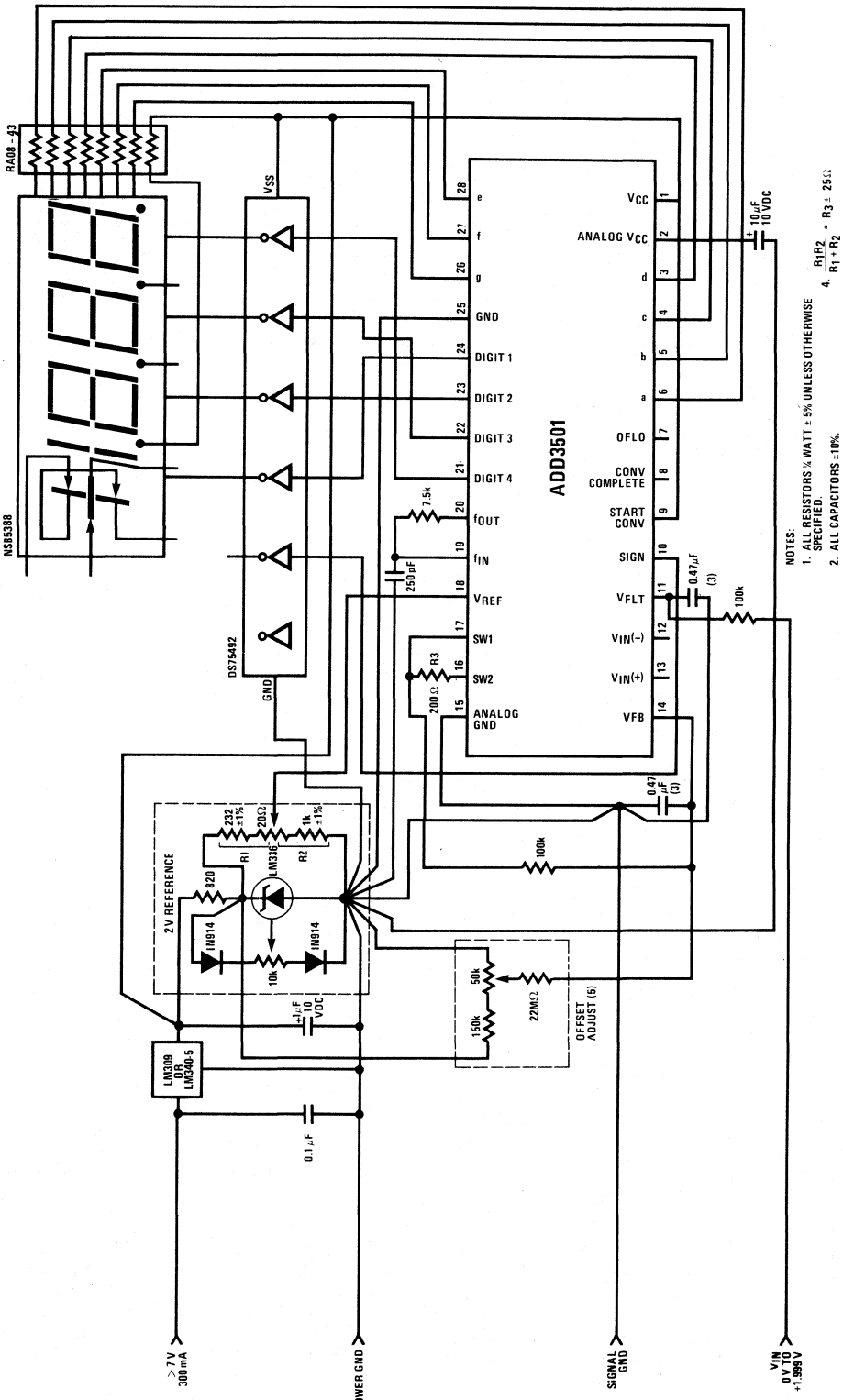
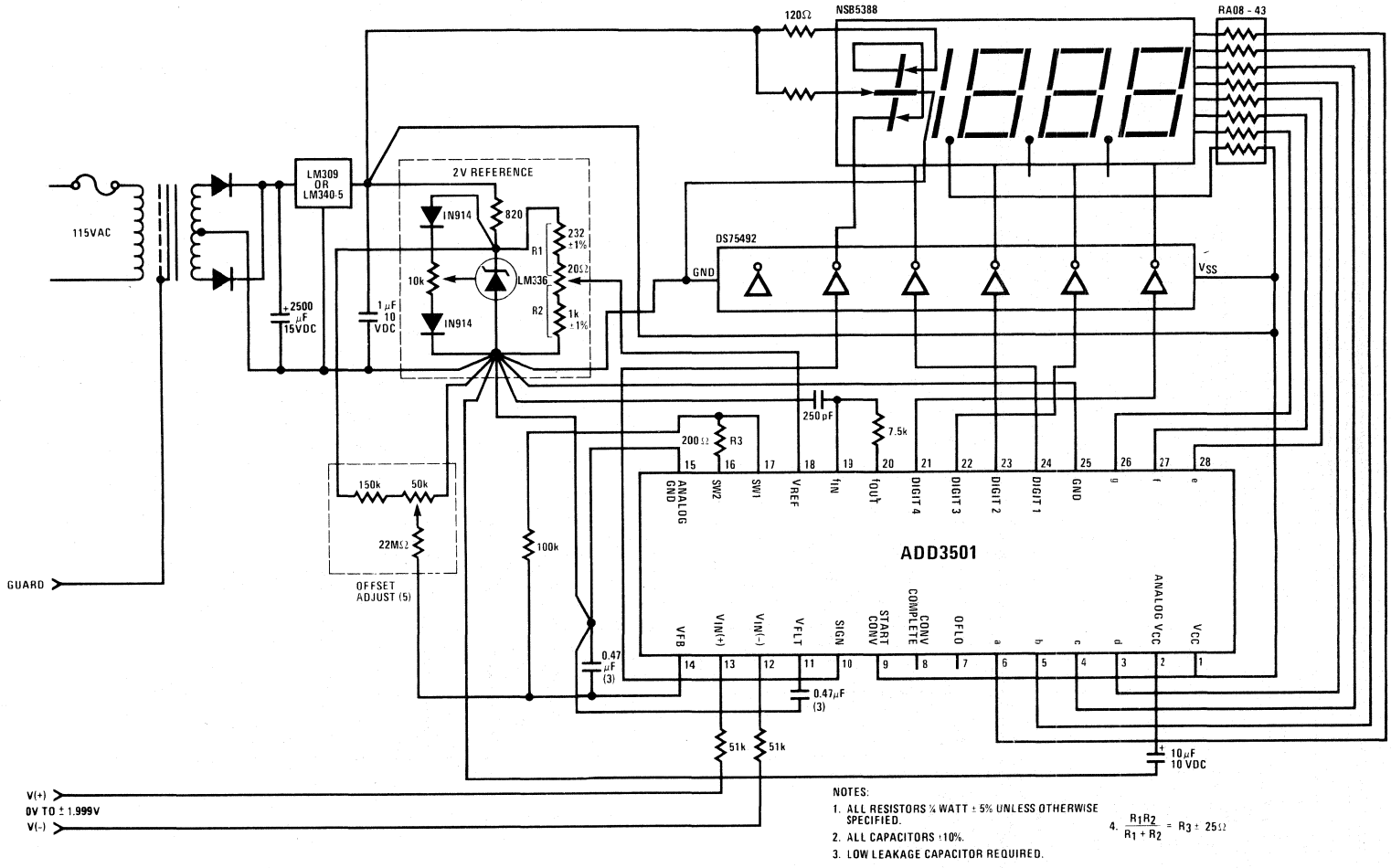


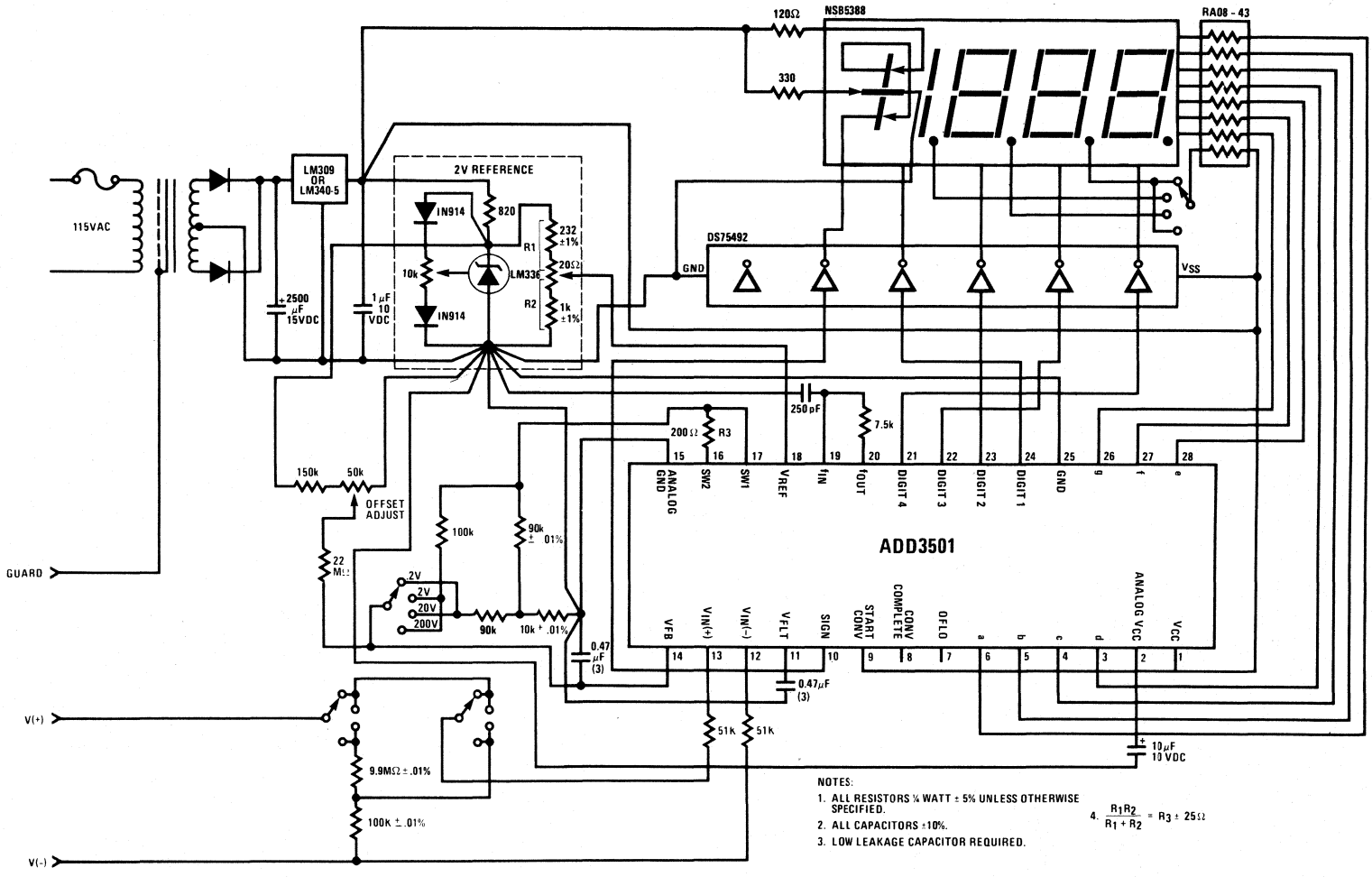
Figure 4. 3½-Digit DPM, +1.999 Volts Full Scale



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 5. 3½-Digit DPM, ±1.999 Volts Full Scale



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 6. 3½-Digit DVM, Four Decade, ±0.2 V, ±2 V, ±20 V and ±200 V Full Scale

National Semiconductor

ADC3511 3½-Digit Microprocessor Compatible A/D Converter
ADC3711 3¾-Digit Microprocessor Compatible A/D Converter

General Description

The ADC3511 and ADC3711 (MM74C937-1, MM74C938-1) monolithic A/D converter circuits are manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and indicated on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available.

The ADC3511 and ADC3711 have been designed to provide addressed BCD data and are intended for use with microprocessors and other digital systems. BCD digits are selected on demand via 2 Digit Select (D0, D1) inputs. Digit Select inputs are latched by a low-to-high transition on the Digit Latch Enable (DLE) input and will remain latched as long as DLE remains high. A start conversion input and a conversion complete output are included on both the ADC3511 and the ADC3711.

Features

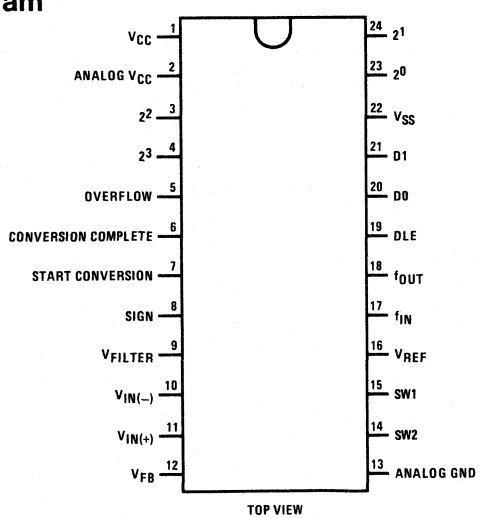
- Operates from single 5V supply
- ADC3511 converts 0 to ±1999 counts
- ADC3711 converts 0 to ±3999 counts
- Addressed BCD outputs
- No external precision components necessary
- Easily interfaced to microprocessors or other digital systems
- Medium speed—200 ms/conversion
- TTL compatible
- Internal clock set with RC network or driven externally
- Overflow indicated by hex "EEEE" output reading as well as an overflow output

Applications

- Low cost analog-to-digital converter
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers

Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	500 mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics ADC3511CC, ADC3711CC

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage (Except f_{IN})		V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage (Except f_{IN})				1.5	V
$V_{IN(1)}$	Logical "1" Input Voltage (f_{IN})		V_{CC}−0.6			V
$V_{IN(0)}$	Logical "0" Input Voltage (f_{IN})				0.6	V
$V_{OUT(1)}$	Logical "1" Output Voltage (Except 2^0, 2^1, 2^2, 2^3)	I_O = 360μA	V_{CC}−0.4			V
$V_{OUT(1)}$	Logical "1" Output Voltage (2^0, 2^1, 2^2, 2^3)	I_O = 360μA	V_{CC}−1.0			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.4	V
$I_{IN(1)}$	Logical "1" Input Current (SC, DLE, D0, D1)	V_{IN} = V_{CC}		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (SC, DLE, D0, D1)	V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	All Outputs Open		0.5	5.0	mA

AC Electrical Characteristics ADC3511CC, ADC3711CC

V_{CC} = 5V; T_A = 25°C; C_L = 50 pF; t_r = t_f = 20 ns; unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
f_{OSC}	Oscillator Frequency			0.6/RC		Hz
f_{IN}	Clock Frequency		100		640	kHz
f_{CONV}	Conversion Rate	ADC3511CC	f_{IN}/64,512			conversions/sec
		ADC3711CC	f_{IN}/129,024			conversions/sec
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns
t_{pd0}, t_{pd1}	Propagation Delay D0, D1, to 2^0, 2^1, 2^2, 2^3	DLE = 0V		2.0	5.0	μs
t_{pd0}, t_{pd1}	Propagation Delay DLE to 2^0, 2^1, 2^2, 2^3			2.0	5.0	μs
$t_{SET\text{-}UP}$	Set-Up Time D0, D1, to DLE	t_{HOLD} = 0 ns		100	200	ns
t_{PWDLE}	Minimum Pulse Width Digit Latch Enable (Low)			100	200	ns

Converter Characteristics

ADC3511CC, ADC3711CC $4.75V \leq V_{CC} \leq 5.25V$; $-40^{\circ}C \leq T_A \leq +85^{\circ}C$, f_C = 5 conv./sec (ADC3511CC); 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	V_{IN} = 0–2V Full Scale V_{IN} = 0–200 mV Full Scale	−0.05	±0.025	+0.05	% of Full-Scale (Note 3)
	Quantization Error		−1		+0	Counts
	Offset Error	V_{IN} = 0V	−0.5	+1.0	+3.0	mV (Note 4)
	Rollover Error		−0		+0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	$T_A = 25^{\circ}C$	−5	±1	+5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

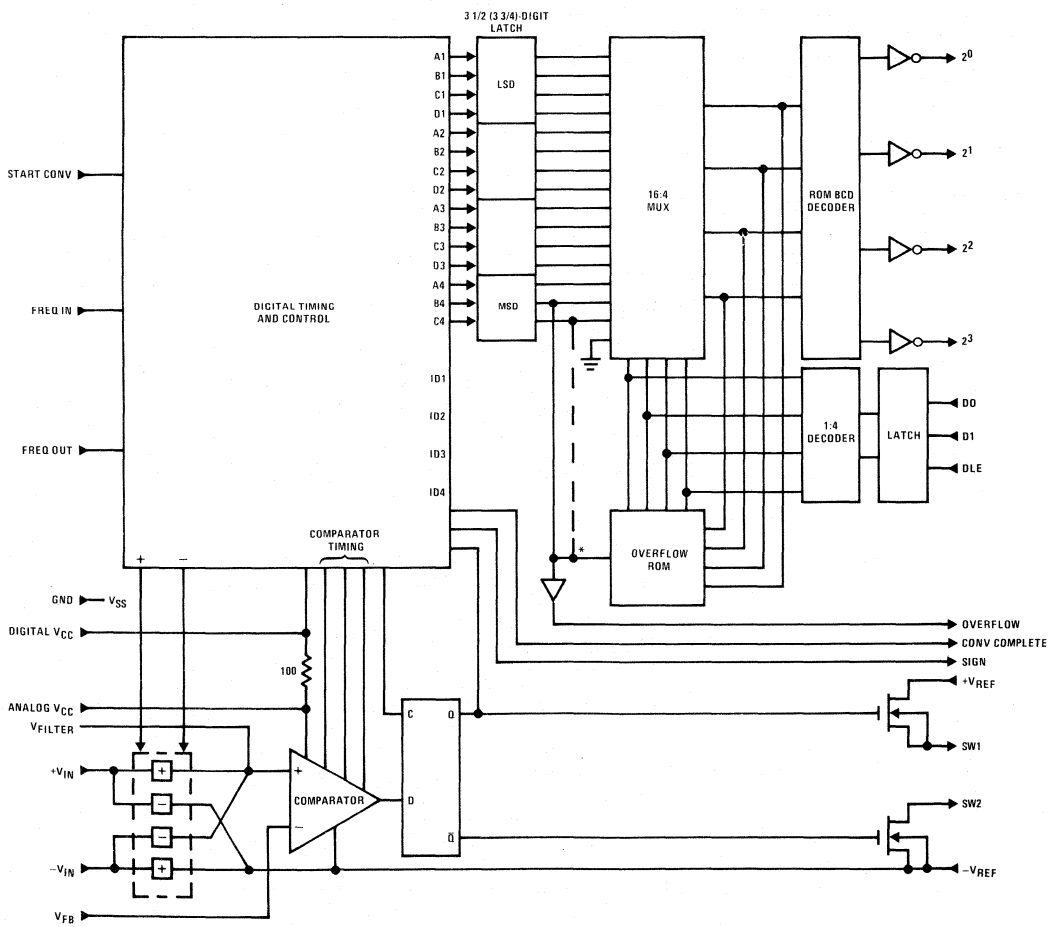
Note 2: All typicals are given for $T_A = 25^{\circ}C$.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore 0.025% of full-scale = 1/2 count and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 count.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

Block Diagram

ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D)



Applications Information

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure 1.* The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level V_{OUT} = 0V. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

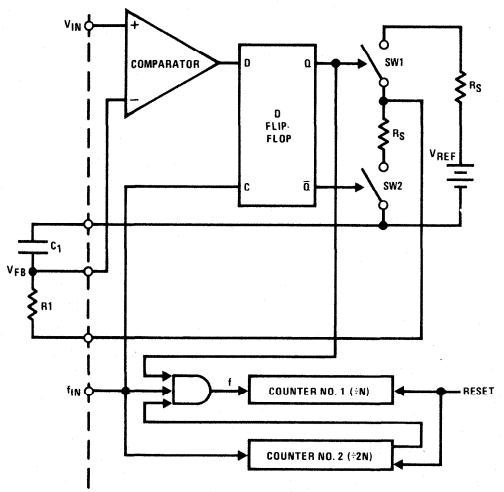
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{(count)} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.

For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in counter no. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE 1. Analog Loop Schematic Pulse Modulation A/D Converter

Applications Information (Continued)

GENERAL INFORMATION

The timing diagram, shown in *Figure 2,* gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the digit latches are updated at a rate equal to 64,512 x $1/f_{IN}$ for the ADC3511, or 129,024 for the ADC3711.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the digit latches. This information will remain in the digit latches until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 64 x $1/f_{IN}$ on the ADC3511, or 128 x $1/f_{IN}$ on the ADC3711.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way. Internally the ADC3511 and ADC3711 are always continuously converting the analog voltage present at their inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the digit latches.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in *Figure 3,* the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 64,512 x $1/f_{IN}$ (129,024 x $1/f_{IN}$ for the ADC3711) and the minimum time is 256 x $1/f_{IN}$ (512 x $1/f_{IN}$ for the ADC3711).

SYSTEM DESIGN CONSIDERATIONS

The ADC3511 and ADC3711 have reduced the problem of high resolution, high accuracy analog-to-digital conversion to nearly the level of simplicity, economy, and compactness usually associated with digital logic circuitry. However, they are truly high precision analog devices, and require the same kind of design considerations given to all analog circuits. While great care has been taken in the design of the ADC3511 and ADC3711 to make their application as easy as possible, in order to utilize them to their full performance potential, good grounding, power supply distribution, decoupling, and regulation techniques should be exercised.

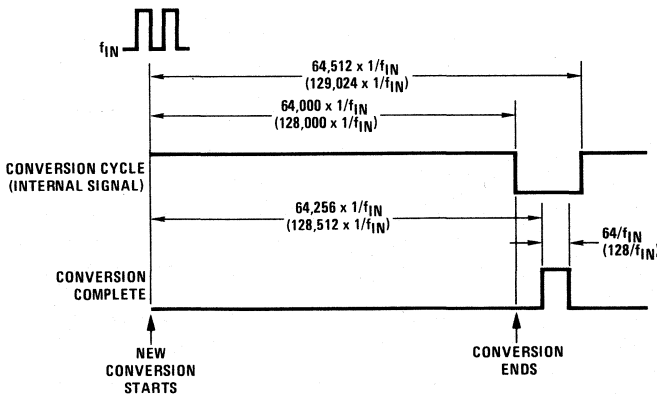


FIGURE 2. Conversion Cycle Timing Diagram for Free Running Operation (Times Shown in Parentheses are for the ADC3711)

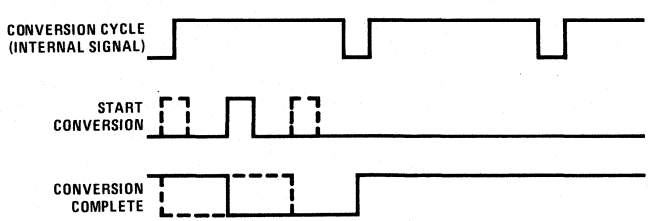


FIGURE 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Truth Table

DIGIT SELECT INPUTS			SELECTED DIGIT
DLE	D1	D0	
L	L	L	Digit 0 (LSD)
L	L	H	Digit 1
L	H	L	Digit 2
L	H	H	Digit 3 (MSD)
H	X	X	Unchanged

L = Low logic level
H = High logic level
X = Irrelevant logic level

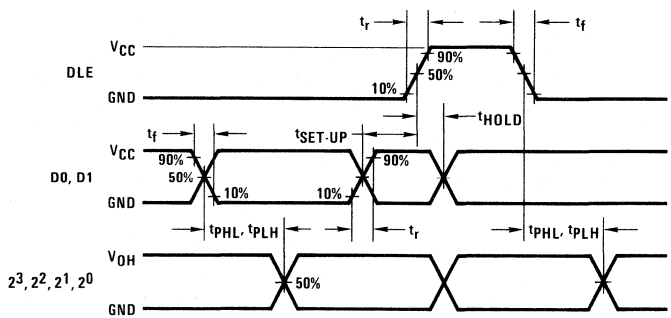
The value of the Selected Digit is presented at the 2^3, 2^2, 2^1 and 2^0 outputs in BCD format.

Note 1: If the value of a digit changes while it is selected, that change *will* be reflected at the outputs.

Note 2: An overflow condition will be indicated by a high level on the OVERFLOW output (pin 5) and E16 in all digits.

Note 3: The sign of the input voltage, when these devices are operated in the bipolar mode, is indicated by the SIGN output (pin 8). A high level indicates a positive voltage, a low level a negative.

Timing Diagrams



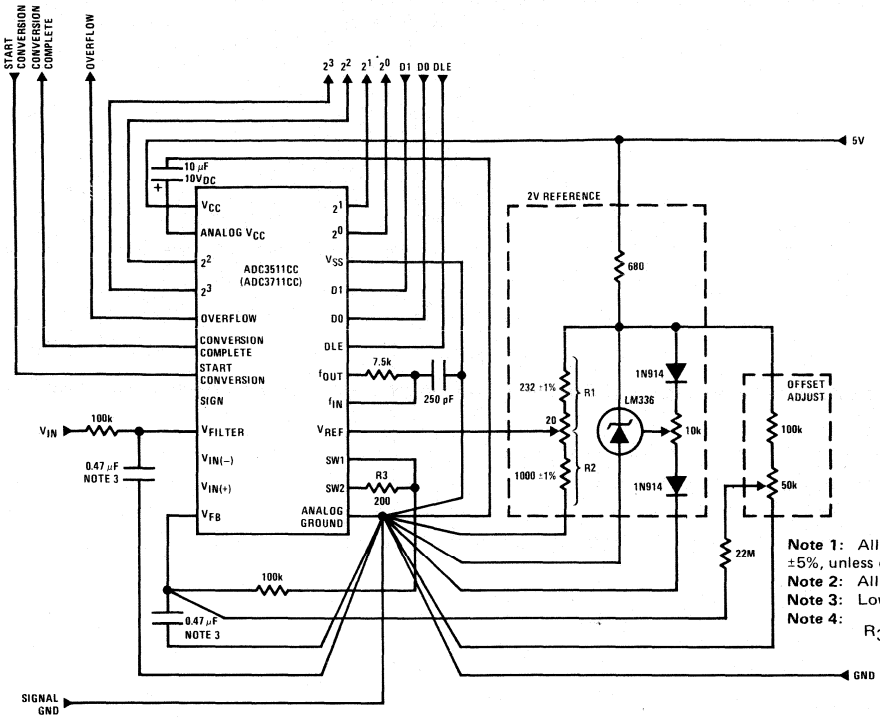
Typical Applications

Figure 4 shows the ADC3511 and ADC3711 connected to convert 0 to +2.000 volts full scale operating from a non-isolated power supply. (Note that the ADC3511 converts 0 to +1999 counts full scale, while the ADC3711 converts 0 to +3999 counts full scale.) In this configuration the SIGN output (pin 8) should be ignored. Higher voltages can, of course, be converted by placing fixed dividers in the inputs, while lower voltages can be converted by placing fixed dividers in the feedback loop, as shown in *Figure 6*.

Figures 5 and 6 show systems operating with isolated supplies that will convert both polarities of inputs. 60 Hz common-mode noise can become a problem in these configurations, so shielded transformers have been shown in the figures. The necessity for, and the type of shielding needed depends on the performance requirements, and the actual applications.

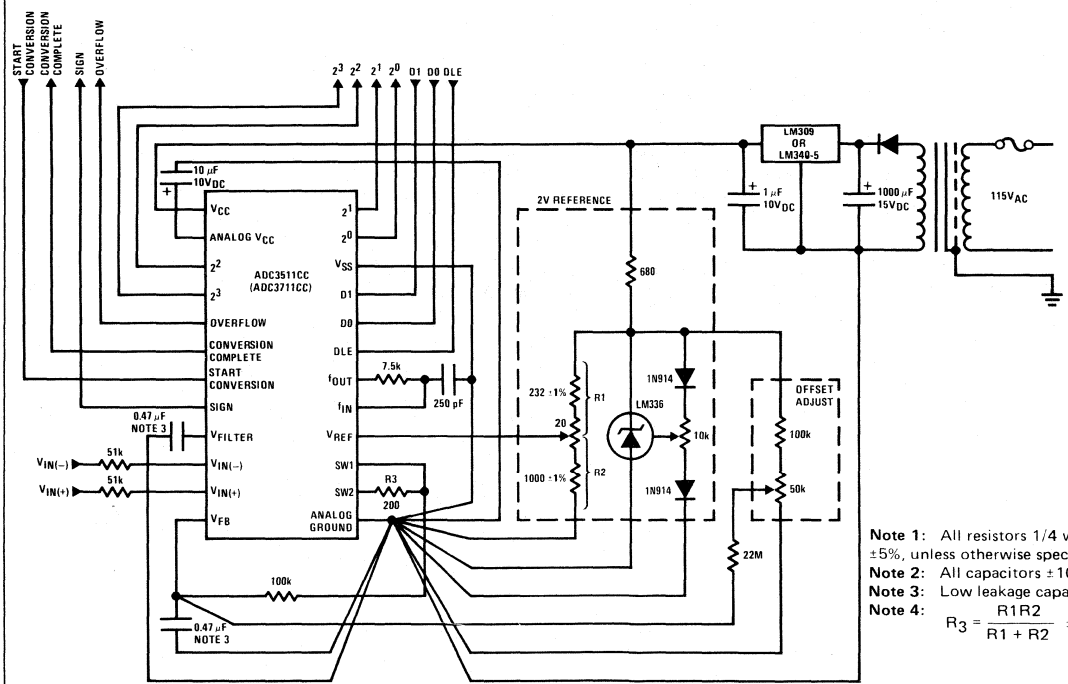
The filter capacitors connected to V_{FB} (pin 12) and V_{FILTER} (pin 11) should be of a low leakage variety. In the examples shown every 1.0 nA of leakage will cause approximately 0.1 mV error (1.0×10^{-9}A x 100 kΩ = 0.1 mV). If the currents in both capacitors are exactly equal however, little error will result since the source impedances driving both capacitors are approximately matched.

Typical Applications (Continued)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4:
$$R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$$

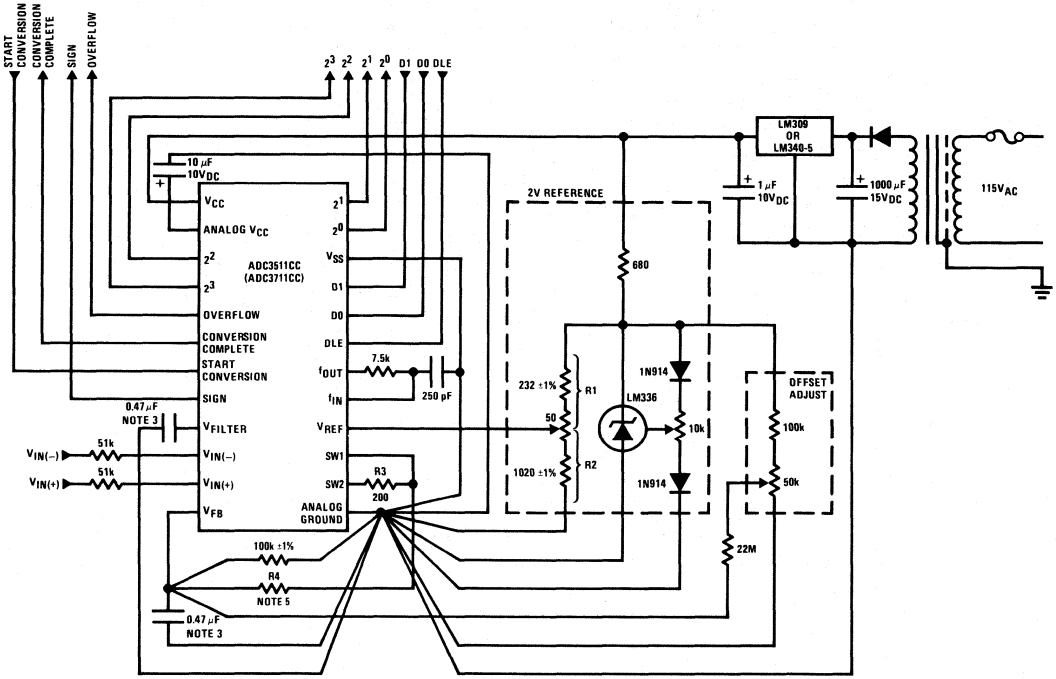
FIGURE 4. 3 1/2-Digit A/D; +1999 Counts, +2.000 Volts Full Scale
(3 3/4-Digit A/D; +3999 Counts, +2.000 Volts Full Scale)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4:
$$R_3 = \frac{R1R2}{R1 + R2} \pm 25\Omega.$$

FIGURE 5. 3 1/2-Digit A/D; ±1999 Counts, ±2.000 Volts Full Scale
(3 3/4-Digit A/D; ±3999 Counts, ±2.000 Volts Full Scale)

Typical Applications (Continued)



Note 1: All resistors 1/4 watt, and ±5%, unless otherwise specified.
Note 2: All capacitors ±10%.
Note 3: Low leakage capacitor.
Note 4:
$$R_3 = \frac{R1R2}{R1 + R2} \pm 50\Omega.$$
Note 5: R4 = 900k ±1% for the ADC3511CC, 200.0 mV Full-Scale.
R4 = 400k ±1% for the ADC3711CC, 400.0 mV Full-Scale.

FIGURE 6. 3 1/2-Digit A/D; ±1999 Counts, ±200.0 mV Full Scale (3 3/4-Digit A/D; ±3999 Counts, ±400.0 mV Full-Scale)

National Semiconductor

ADD3701 3¾ Digit DVM with Multiplexed 7-Segment Output

General Description

The ADD3701 (MM74C936-1) monolithic DVM circuit is manufactured using standard complementary MOS (CMOS) technology. A pulse modulation analog-to-digital conversion technique is used and requires no external precision components. In addition, this technique allows the use of a reference voltage that is the same polarity as the input voltage.

One 5 V (TTL) power supply is required. Operating with an isolated supply allows the conversion of positive as well as negative voltages. The sign of the input voltage is automatically determined and output on the sign pin. If the power supply is not isolated, only one polarity of voltage may be converted.

The conversion rate is set by an internal oscillator. The frequency of the oscillator can be set by an external RC network or the oscillator can be driven from an external frequency source. When using the external RC network, a square wave output is available. It is important to note that great care has been taken to synchronize digit multiplexing with the A/D conversion timing to eliminate noise due to power supply transients.

The ADD3701 has been designed to drive 7-segment multiplexed LED displays directly with the aid of external digit buffers and segment resistors. Under condition of overrange, the overflow output will go high and the display will read +OFL or −OFL, depending on whether the input voltage is positive or negative. In addition to this, the most significant digit is blanked when zero.

A start conversion input and a conversion complete output are included.

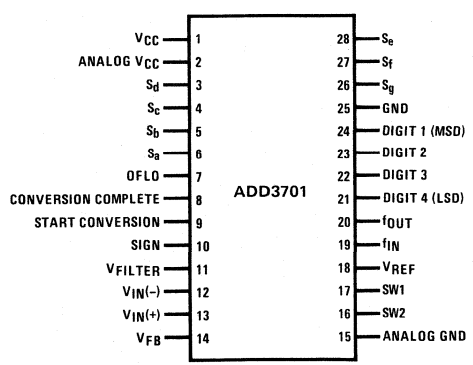
Features

- Operates from single 5 V supply
- Converts 0 to ±3999 counts
- Multiplexed 7-segment
- Drives segments directly
- No external precision components necessary
- Accuracy specified over temperature
- Medium speed — 400 ms/conversion
- Internal clock set with RC network or driven externally
- Overrange indicated by +OFL or −OFL display reading and OFLO output
- Analog inputs in applications shown can withstand ±200 Volts

Applications

- Low cost digital power supply readouts
- Low cost digital multimeters
- Low cost digital panel meters
- Eliminate analog multiplexing by using remote A/D converters
- Convert analog transducers (temperature, pressure, displacement, etc.) to digital transducers
- Indicators and displays requiring readout up to 3999 counts

Connection Diagram



Absolute Maximum Ratings (Note 1)

Voltage at Any Pin except Start Conversion	−0.3V to V_{CC} + 0.3V
Voltage at Start Conversion	−0.3V to +15.0V
Operating Temperature Range (T_A)	−40°C to +85°C
Package Dissipation at T_A = 25°C	800mW
Operating V_{CC} Range	4.5V to 6.0V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature Range	−65°C to +150°C

Electrical Characteristics ADD3701

4.75V ≤ V_{CC} ≤ 5.25V, −40°C ≤ T_A ≤ +85°C, unless otherwise specified.

Parameter		Conditions	Min	Typ[2]	Max	Units
$V_{IN(1)}$	Logical "1" Input Voltage		V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage				1.5	V
$V_{OUT(0)}$	Logical "0" Output Voltage (All Digital Outputs Except Digit Outputs)	I_O = 1.1 mA			0.4	V
$V_{OUT(0)}$	Logical "0" Output Voltage (Digit Outputs)	I_O = 0.7 mA			0.4	V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Segment Outputs)	I_O = 50 mA @ T_J = 25°C V_{CC}=5V I_O = 30 mA @ T_J = 100°C	V_{CC} − 1.6 V_{CC} − 1.6	V_{CC} − 1.3 V_{CC} − 1.3		V V
$V_{OUT(1)}$	Logical "1" Output Voltage (All Digital Outputs Except Segment Outputs)	I_O = 500 μA (Digit Outputs) I_O = 360 μA (Conv. Complete, +/−, OFLO Outputs)	V_{CC} − 0.4			V
I_{SOURCE}	Output Source Current (Digit Outputs)	V_{OUT} = 1.0 V	2.0			mA
$I_{IN(1)}$	Logical "1" Input Current (Start Conversion)	V_{IN} = 15 V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (Start Conversion)	V_{IN} = 0 V	−1.0			μA
I_{CC}	Supply Current	Segments and Digits Open		0.5	10	mA
	Oscillator Frequency			0.6/RC		kHz
f_{IN}	Clock Frequency		100		640	kHz
f_C	Conversion Rate			f_{IN}/129,024		conv./sec
f_{MUX}	Digit Mux Rate			f_{IN}/512		Hz
t_{BLANK}	Inter Digit Blanking Time			1/(32 f_{MUX})		seconds
t_{SCPW}	Start Conversion Pulse Width		200		DC	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals given for T_A = 25° C.

Note 3: Full scale = 4000 counts; therefore 0.025% of full scale = 1 count and 0.05% of full scale = 2 counts.

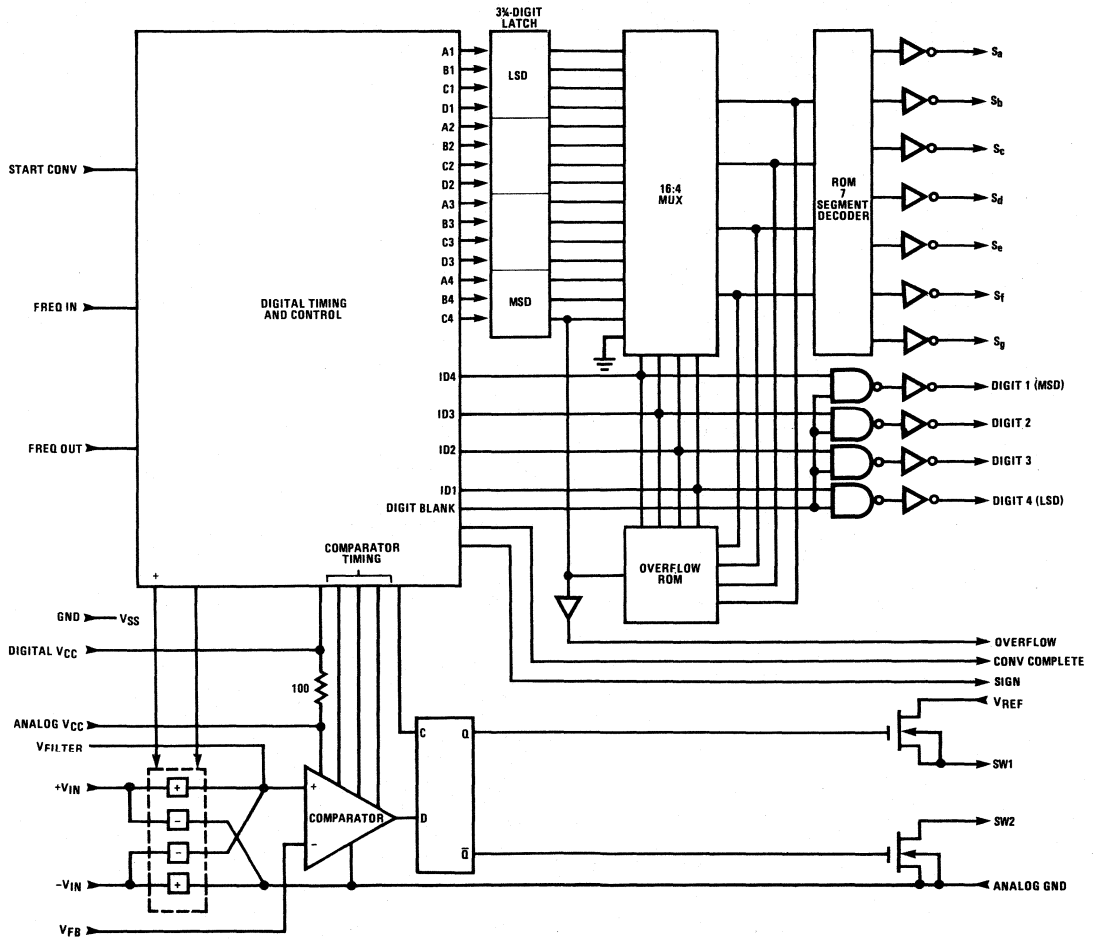
Note 4: For 2.000 Volts full scale, 1 mV = 2 counts.

Electrical Characteristics ADD3701

t_C = 2.5 conversions/second, $0°C \leq T_A \leq +70°C$, unless otherwise specified.

Parameter	Conditions	Min	Typ[2]	Max	Units
Non-Linearity of Output Reading	V_{IN} = 0-2 V Full Scale V_{IN} = 0-200 mV Full Scale	-0.05	±0.025	+0.05	% full scale (Note 3)
Quantization Error		-1		+0	counts
Offset Error, V_{IN} = 0 V		-0.5	+1.5	+3	mV (Note 4)
Rollover Error		-0		+0	counts
Analog Input Current ($V_{IN}+$, $V_{IN}-$)	$T_A = 25°C$	-5	±1	+5	nA

Block Diagram



ADD3701 3¾-Digit DVM Block Diagram

Theory of Operation

A schematic for the analog loop is shown in figure 1. The output of SW1 is either at V_{REF} or zero volts, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0\,V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and Q outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500 V. If the Q output of the D flip-flop is high then V_{OUT} will equal V_{REF} (2.000 V) and V_{FB} will charge toward 2 V with a time constant equal to R_1C_1. At some time V_{FB} will exceed 0.500 V and the comparator output will switch to 0 V. At the next clock rising edge the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0 V. At this time V_{FB} will start discharging toward 0 V with a time constant R_1C_1. When V_{FB} is less than 0.5 V the comparator output will switch high. On the rising edge of the next clock the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0 V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF}\,\frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF}\,(\text{duty cycle})$$

The lowpass filter will pass the DC value and then:

$$V_{FB} = V_{REF}\,(\text{duty cycle})$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF}\,(\text{duty cycle})$$

or

$$\frac{V_{IN}}{V_{REF}} = (\text{duty cycle})$$

The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = (\text{duty cycle}) \times (\text{clock})$$

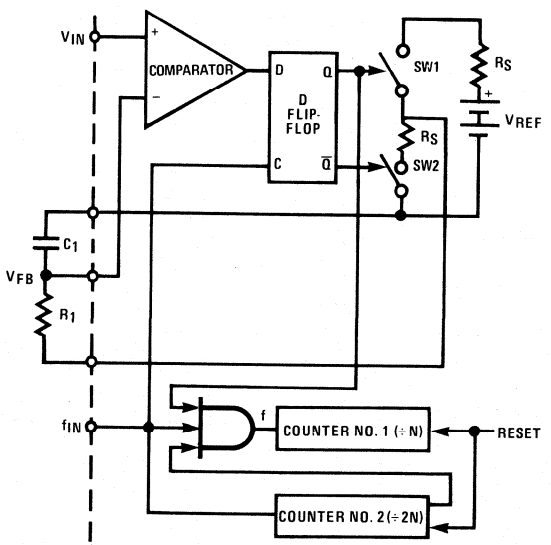
Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$(\text{count}) = \frac{f}{(\text{clock})/N} = \frac{(\text{duty cycle}) \times (\text{clock})}{(\text{clock})/N}$$

$$= \frac{V_{IN}}{V_{REF}} \times N$$

For the ADD3701 N = 4000.

Schematic Diagram



$V_{IN} = V_{FB} = V_{REF} \times (\text{duty cycle})$

$f = (\text{duty cycle}) \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{(\text{duty cycle}) \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

Figure 1. Analog Loop Schematic Pulse Modulation A/D Converter

General Information

The timing diagram, shown in figure 2, gives operation for the free running mode. Free running operation is obtained by connecting the Start Conversion input to logic "1" (V_{CC}). In this mode the analog input is continuously converted and the display is updated at a rate equal to 129,024 x $1/f_{IN}$.

The rising edge of the Conversion Complete output indicates that new information has been transferred from the internal counter to the display latch. This information will remain in the display latch until the next low-to-high transition of the Conversion Complete output. A logic "1" will be maintained on the Conversion Complete output for a time equal to 128 x $1/f_{IN}$.

Figure 3 gives the operation using the Start Conversion input. It is important to note that the Start Conversion input and Conversion Complete output do not influence the actual analog-to-digital conversion in any way.

Internally the ADD3701 is always continuously converting the analog voltage present at its inputs. The Start Conversion input is used to control the transfer of information from the internal counter to the display latch.

An RS latch on the Start Conversion input allows a broad range of input pulse widths to be used on this signal. As shown in figure 3, the Conversion Complete output goes to a logic "0" on the rising edge of the Start Conversion pulse and goes to a logic "1" some time later when the new conversion is transferred from the internal counter to the display latch. Since the Start Conversion pulse can occur at any time during the conversion cycle, the amount of time from Start Conversion to Conversion Complete will vary. The maximum time is 129,024 x $1/f_{IN}$ and the minimum time is 512 x $1/f_{IN}$.

Timing Waveforms

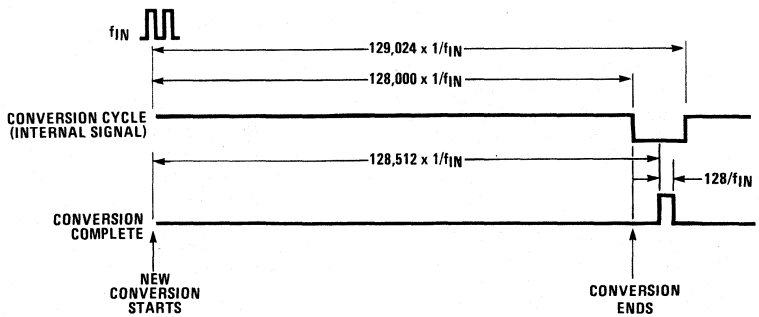


Figure 2. Conversion Cycle Timing Diagram for Free Running Operation

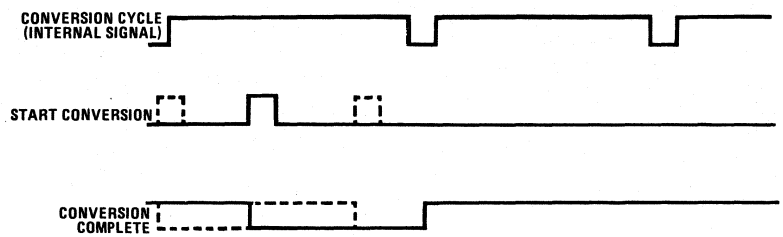


Figure 3. Conversion Cycle Timing Diagram Operating with Start Conversion Input

Applications

SYSTEM DESIGN CONSIDERATIONS

Perhaps the most important thing to consider when designing a system using the ADD3701 is power supply noise on the V_{CC} and ground lines. Because a single power supply is used and currents in the 300 mA range are being switched, good circuit layout techniques cannot be overemphasized. Great care has been exercised in the design of the ADD3701 to minimize these problems but poor printed circuit layout can negate these features.

Figures 4, 5, and 6 show schematics of DVM systems. An attempt has been made to show, on these schematics, the proper distribution for ground and V_{CC}. To help isolate digital and analog portions of the circuit, the analog V_{CC} and ground have been separated from the digital V_{CC} and ground. Care must be taken to eliminate high current from flowing in the analog V_{CC} and ground wires. The most effective method of accomplishing this is to use a single ground point and a single V_{CC} point where all wires are brought together. In addition to this the conductors must be of sufficient size to prevent significant voltage drops.

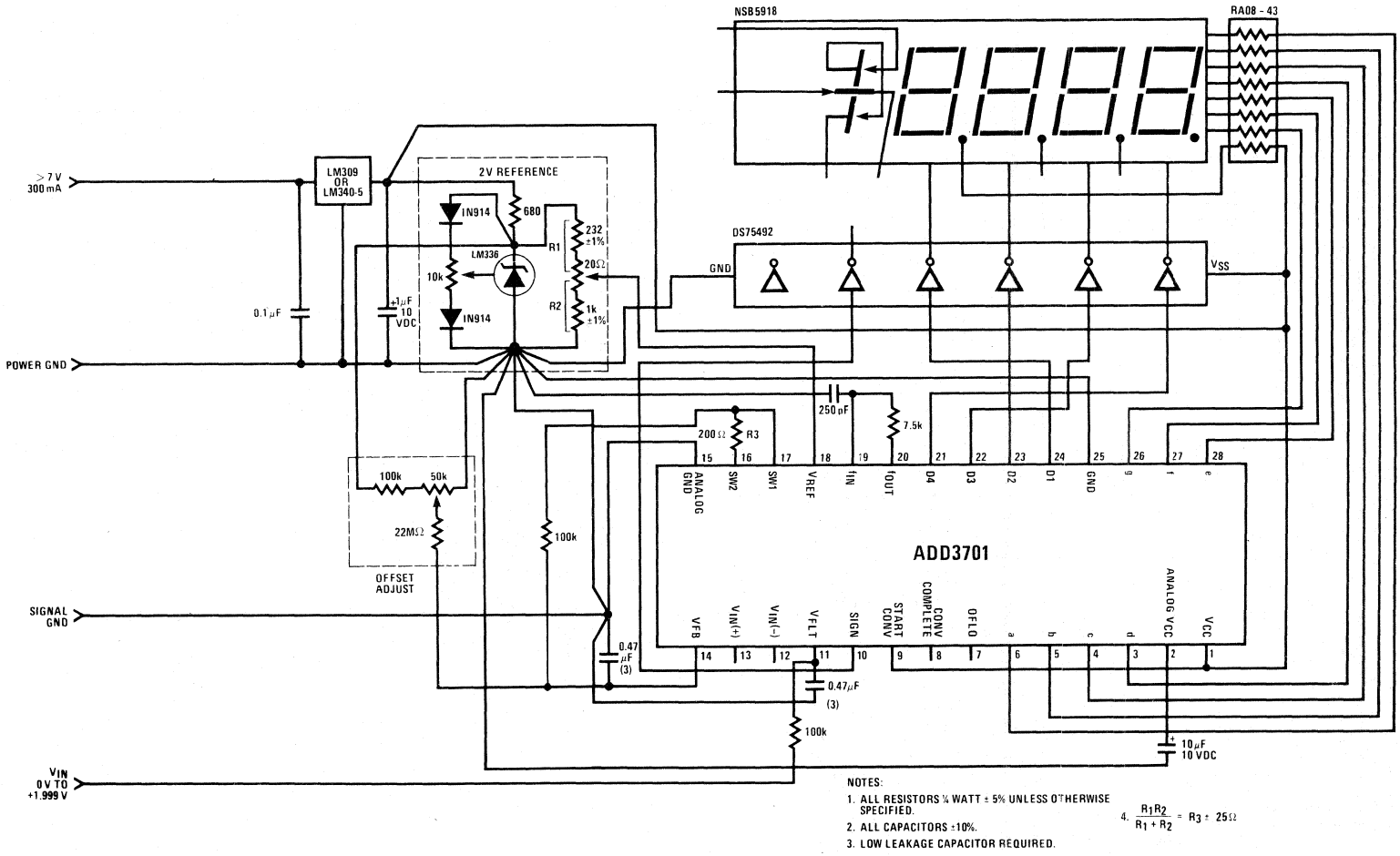
To prevent switching noise from causing jitter problems, a voltage regulator with good high frequency response is necessary. The LM309 and the LM340-5 voltage regulators all function well and are shown in figures 4, 5, and 6. Adding more filtering than is shown will in general increase the jitter rather than decrease it.

The most important characteristic of transients on the V_{CC} line is the duration of the transient and not its amplitude.

Figure 4 shows a DPM system which converts 0 to +3.999 counts operating from a non-isolated power supply. In this configuration the sign output could be + (logic "1") or – (logic "0") and it should be ignored. Higher voltages could be converted by placing a fixed divider on the input; lower voltages could be converted by placing a fixed divider on the feedback, as shown in figure 5.

Figures 5 and 6 show systems operating with an isolated supply that will convert positive and negative inputs. 60 Hz common mode input becomes a problem in this configuration and a transformer with an electrostatic shield between primary and secondary windings is shown. The necessity for using a shielded transformer depends on the performance requirements and the actual application.

The filter capacitors connected to V_{FB} (pin 14) and V_{FLT} (pin 11) should be low leakage. In the application examples shown every 1.0 nA of leakage current will cause 0.1 mV error (1.0×10^{-9} A x 100 kΩ = 0.1 mV). If the leakage current in both capacitors is exactly the same no error will result since the source impedances driving them are matched.



NOTES:

1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1R_2}{R_1+R_2} = R_3 \pm 25\Omega$

Figure 4. 3¾-Digit DPM, +3.999 Count Full Scale

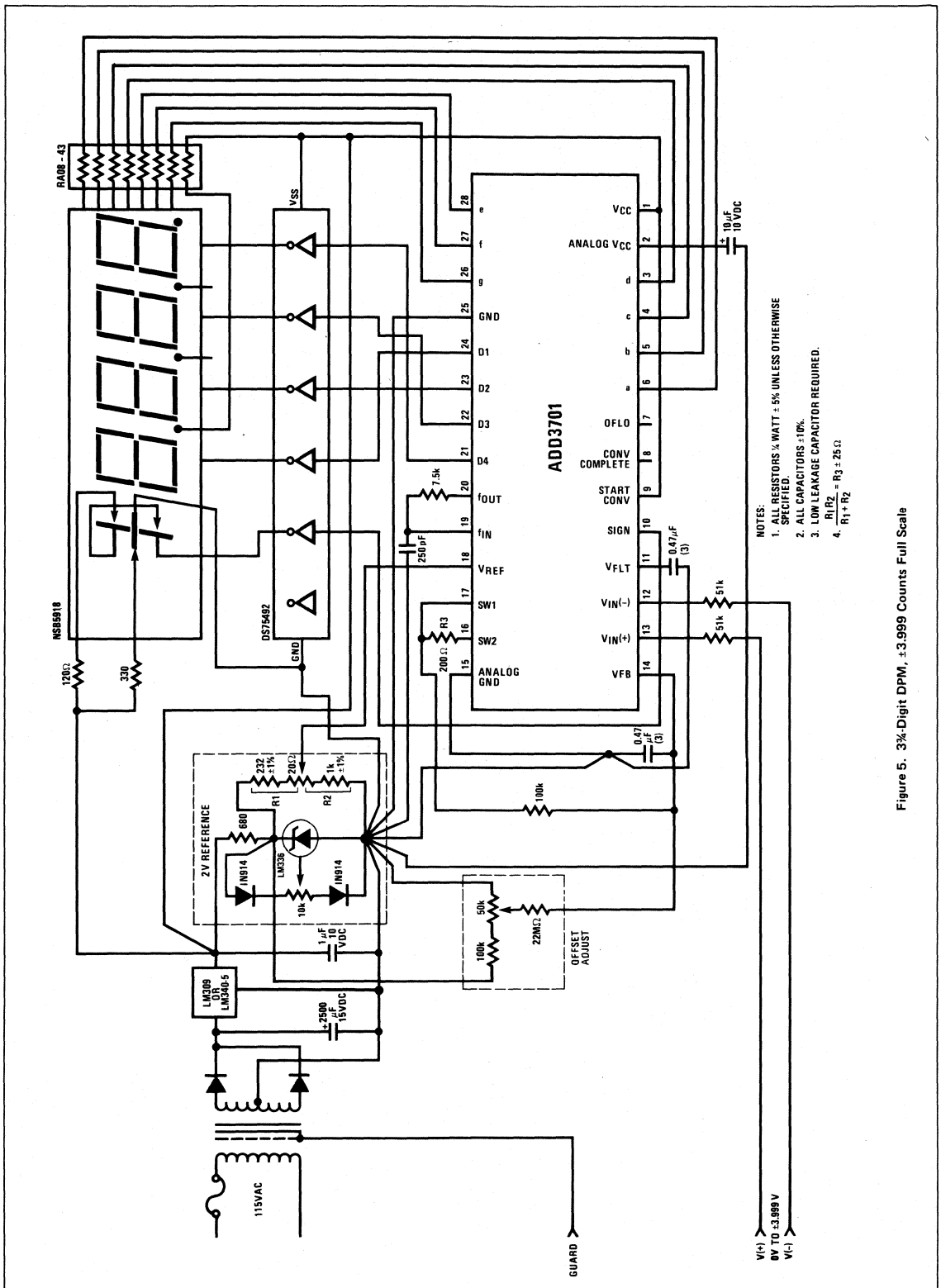
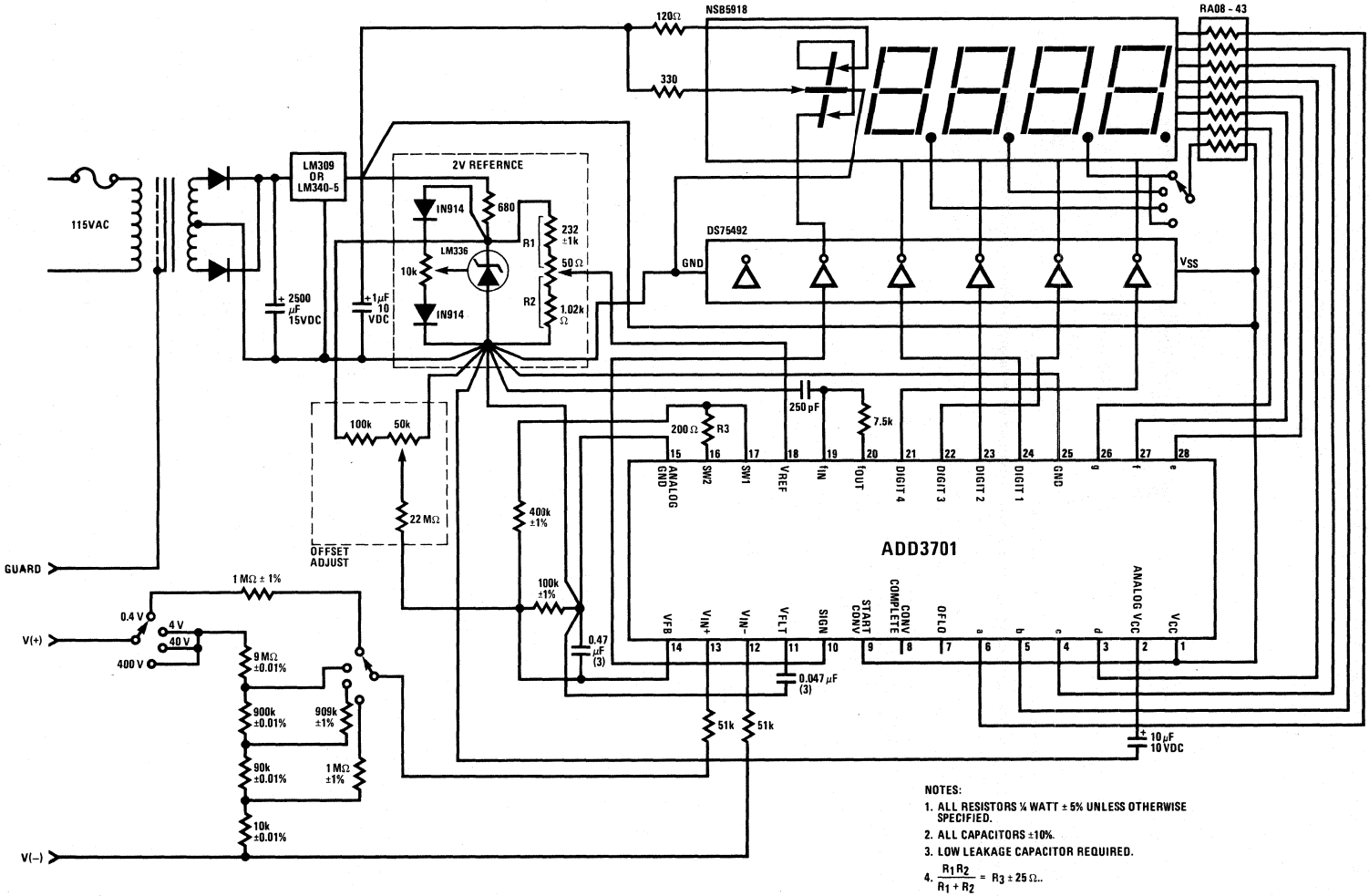


Figure 5. 3¾-Digit DPM, ±3.999 Counts Full Scale



NOTES:
1. ALL RESISTORS ¼ WATT ± 5% UNLESS OTHERWISE SPECIFIED.
2. ALL CAPACITORS ±10%.
3. LOW LEAKAGE CAPACITOR REQUIRED.
4. $\frac{R_1 R_2}{R_1 + R_2} = R_3 \pm 25\,\Omega$.

Figure 6. 3¾-Digit DVM, Four Decade, ±0.4V, ±4V, ±40V, and ±400V Full Scale

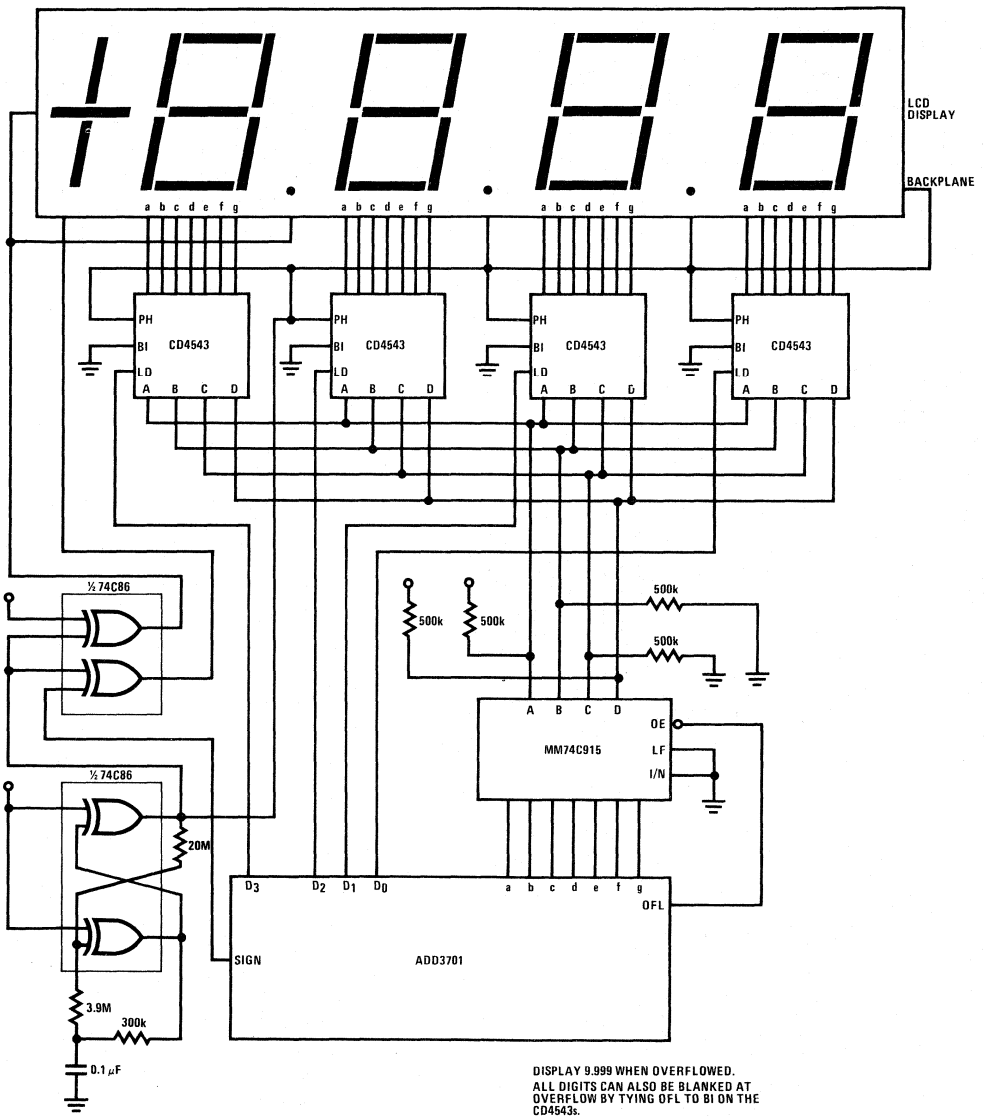


Figure 7. ADD3701 Driving Liquid Crystal Display

CD4000B Series

National Semiconductor

CD4000M/CD4000C Dual 3-Input NOR Gate Plus Inverter

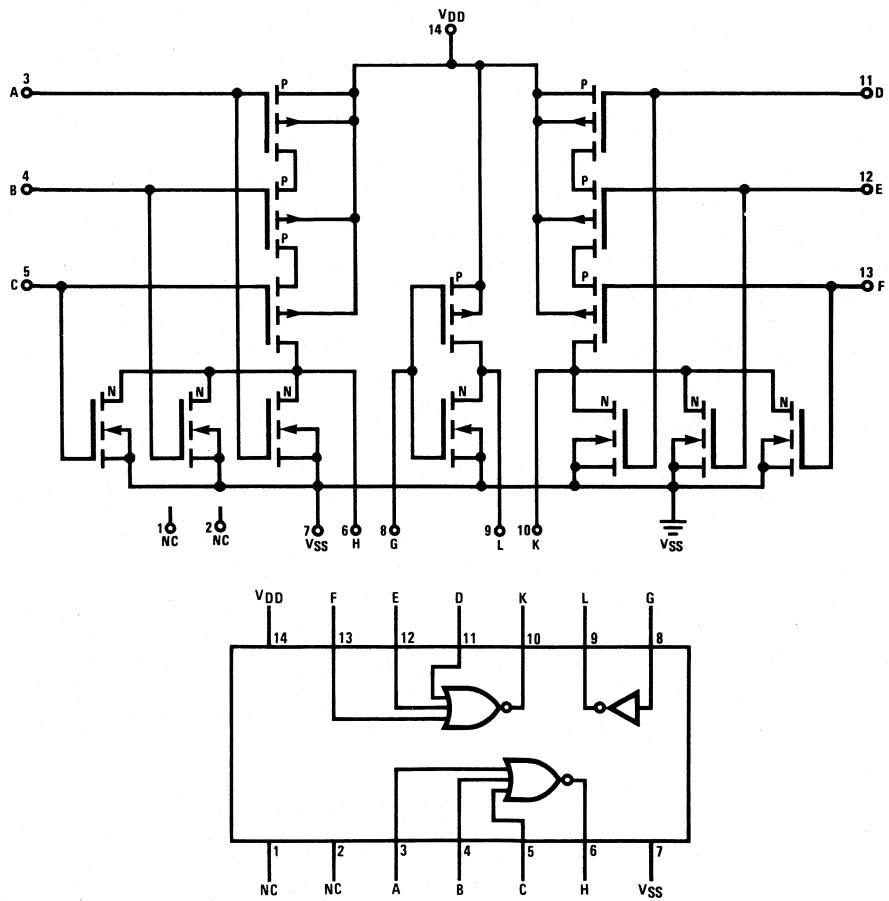
general description

The CD4000M/CD4000C is a monolithic complementary MOS (CMOS) dual 2-input NOR gate plus an inverter. N- and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

features

■ Wide supply voltage range	3.0 V to 15 V
■ Low power	10 nW (typical)
■ High noise immunity	0.45 V_{DD} typical

schematic and connection diagrams



absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} −0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
CD4000M	−55°C to +125°C
CD4000C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3 V to V_{SS} + 15 V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics—CD4000M (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		0.05			0.05		3	μA
		V_{DD} = 10 V		0.1			0.1		6	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.5		1.5			1.4		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.4		1.5			1.5		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.5		0.4			0.28		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.1		0.9			0.65		mA
I_{DP}	High Level Output Current	V_{DD} = 5 V, V_O = 2.5 V	−0.62		−0.5			−0.35		mA
		V_{DD} = 10 V, V_O = 9.5 V	−0.62		−0.5			−0.35		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−1.0		−0.1	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		1.0		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

Note 3: For the NOR gates V_{NH} and V_{NL} are tested at each input while all other inputs are at V_{SS}.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics— CD4000M T_A = +25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5 V		40	50	ns
		V_{DD} = 10 V		20	40	ns
t_{PLH}	Propagation Delay Time, Low to High Level	V_{DD} = 5 V		50	95	ns
		V_{DD} = 10 V		25	45	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5 V		50	125	ns
		V_{DD} = 10 V		20	70	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5 V		70	175	ns
		V_{DD} = 10 V		35	75	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		35		pF

dc electrical characteristics— C4000C (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		0.5			0.5		15	μA
		V_{DD} = 10 V		5			5		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
		V_{DD} = 10 V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
		V_{DD} = 10 V	9.95		9.95			9.95		V
V_{NL}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.5		1.5			1.4		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	3.0		3.0			2.9		V
V_{NH}	Noise Immunity (Note 3)	V_{DD} = 5 V, V_O = 1.4 V or 3.6 V	1.4		1.5			1.5		V
		V_{DD} = 10 V, V_O = 2.8 V or 7.2 V	2.9		3.0			3.0		V
I_{DN}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.35		0.3			0.24		mA
		V_{DD} = 10 V, V_O = 0.5 V	0.72		0.6			0.48		mA
I_{DP}	High Level Output Current	V_{DD} = 5 V, V_O = 2.5 V	−0.35		−0.3			−0.24		mA
		V_{DD} = 10 V, V_O = 9.5 V	−0.3		−0.25			−0.2		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.1		1.0	μA

ac electrical characteristics— CD4000C T_A = +25°C, C_L = 15 pF, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High to Low Level	V_{DD} = 5 V		40	80	ns
		V_{DD} = 10 V		20	55	ns
t_{PLH}	Propagation Delay Time, Low to High Level	V_{DD} = 5 V		50	120	ns
		V_{DD} = 10 V		25	65	ns
t_{THL}	Transition Time, High to Low Level	V_{DD} = 5 V		50	200	ns
		V_{DD} = 10 V		20	115	ns
t_{TLH}	Transition Time, Low to High Level	V_{DD} = 5 V		70	300	ns
		V_{DD} = 10 V		35	125	ns
C_I	Input Capacitance	Any Input		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		35		pF

National Semiconductor

CD4001M/CD4001C Quadruple 2-Input NOR Gate

general description

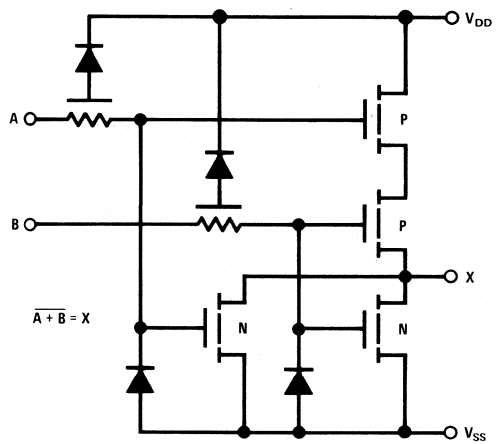
The CD4001M/CD4001C is a monolithic complementary MOS (CMOS) quadruple two-input NOR gate integrated circuit. N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions.

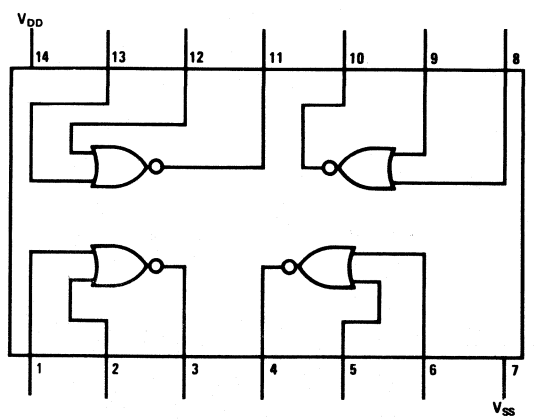
All inputs are protected against static discharge and latching conditions.

features

- Wide supply voltage range — 3V to 15V
- Low power — 10 nW (typ)
- High noise immunity — 0.45 V_{DD} (typ)

schematic and connection diagrams





TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4001M	−55°C to +125°C
CD4001C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4001M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.05		0.001	0.05			3	μA
	V_{DD} = 10V			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			0.25		0.005	0.25			15	μW
	V_{DD} = 10V			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
	V_{DD} = 10V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V, V_I = V_{SS}, I_O = 0A	4.99			4.99	5		4.95			V
	V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V, I_O = 0A	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V, I_O = 0A	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.5			0.40	1		0.28			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.1			0.9	2.5		0.65			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−0.62			−0.5	−2		−0.35			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.62			−0.5	−1		−0.35			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4001C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.5		0.005	0.5			15	μA
	V_{DD} = 10V			5		0.005	5			30	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			2.5		0.025	2.5			75	μW
	V_{DD} = 10V			50		0.05	50			300	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
	V_{DD} = 10V, V_I = V_{DD}, I_O = 0A			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V, V_I = V_{SS}, I_O = 0A	4.99			4.99	5		4.95			V
	V_{DD} = 10V, V_I = V_{SS}, I_O = 0A	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V, I_O = 0A	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V, I_O = 0A	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V, I_O = 0A	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V, I_O = 0A	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.35			0.3	1		0.24			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−0.35			−0.3	−2		−0.24			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.3			−0.25	−1		−0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4001M

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5V$ $V_{DD} = 10V$		35 25	50 40	ns ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5V$ $V_{DD} = 10V$		35 25	65 40	ns ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5V$ $V_{DD} = 10V$		65 35	125 70	ns ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5V$ $V_{DD} = 10V$		65 35	175 75	ns ns
Input Capacitance (C_I)	Any Input		5		pF

ac electrical characteristics CD4001C

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5V$ $V_{DD} = 10V$		35 25	80 55	ns ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5V$ $V_{DD} = 10V$		35 25	120 65	ns ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5V$ $V_{DD} = 10V$		65 35	200 115	ns ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5V$ $V_{DD} = 10V$		65 35	300 125	ns ns
Input Capacitance (C_I)	Any Input		5		pF

National Semiconductor

CD4001BM/CD4001BC Quad 2-Input NOR Buffered B Series Gate
CD4011BM/CD4011BC Quad 2-Input NAND Buffered B Series Gate

general description

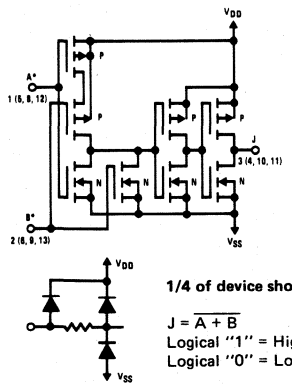
These quad gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

features

- Low power TTL compatability, fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range

schematic and connection diagrams



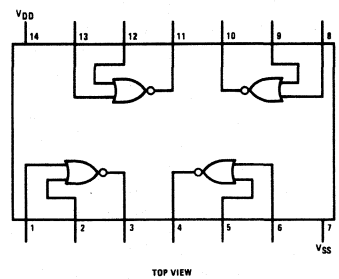
1/4 of device shown

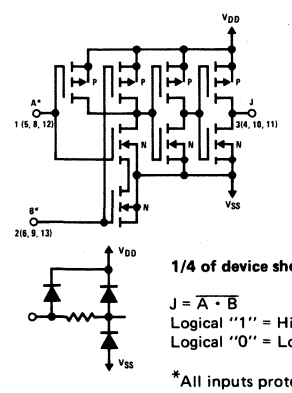
$J = \overline{A + B}$

Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4001BC/CD4001BM
Dual-In-Line and Flat Package





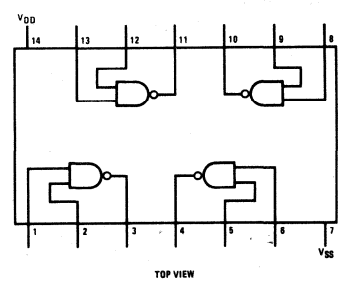
1/4 of device shown

$J = \overline{A \cdot B}$

Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4011BC/CD4011BM
Dual-In-Line and Flat Package



absolute maximum ratings (Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4001BM, CD4011BM	−55°C to +125°C
CD4001BC, CD4011BC	−40°C to +85°C

dc electrical characteristics CD4001BM, CD4011BM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C		+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V		0.50		0.005	0.50		15	μA
		V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

dc electrical characteristics CD4001BC, CD4011BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics CD4001BC, CD4001BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical temperature coefficient is 0.3%/°C.

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	110	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

ac electrical characteristics CD4011BC, CD4011BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF, R_L = 200k. Typical Temperature Coefficient is 0.3%/°C.

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay, High-to-Low Level	V_{DD} = 5V	120	250	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	35	70	ns
t_{PLH}	Propagation Delay, Low-to-High Level	V_{DD} = 5V	85	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	14		pF

typical performance characteristics

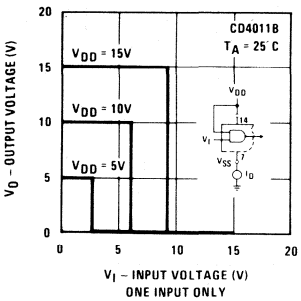


FIGURE 1. Typical Transfer Characteristics

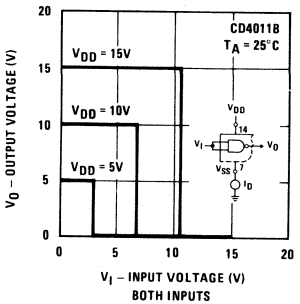


FIGURE 2. Typical Transfer Characteristics

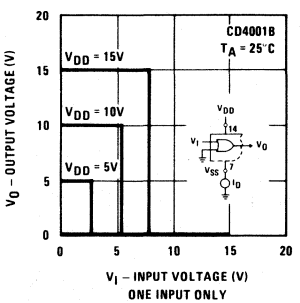


FIGURE 3. Typical Transfer Characteristics

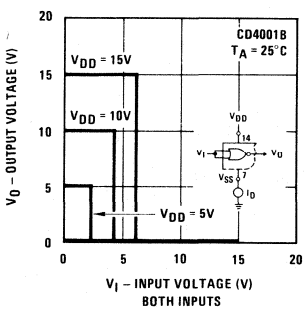


FIGURE 4. Typical Transfer Characteristics

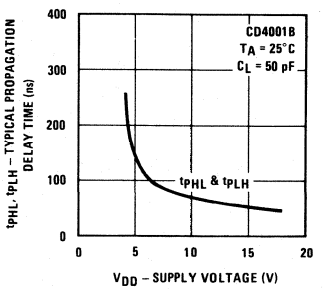


FIGURE 5

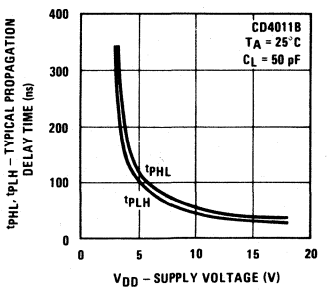


FIGURE 6

typical performance characteristics (cont)

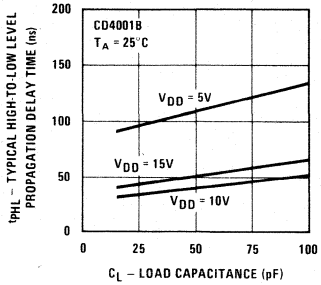


FIGURE 7

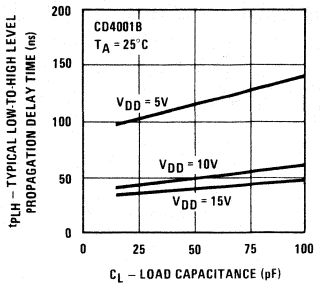


FIGURE 8

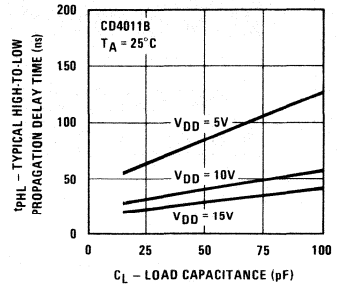


FIGURE 9

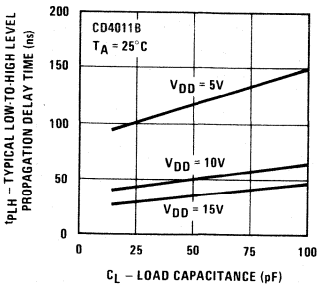


FIGURE 10

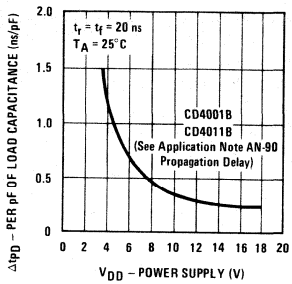


FIGURE 11

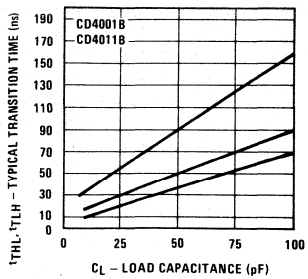


FIGURE 12

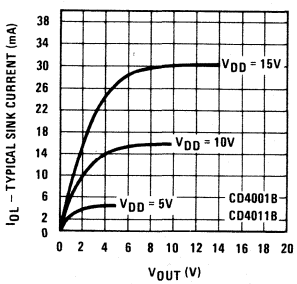


FIGURE 13

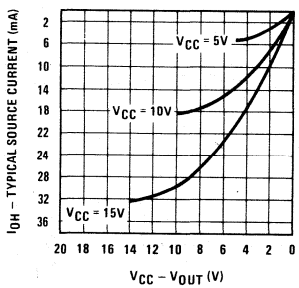


FIGURE 14

National Semiconductor

CD4002M/CD4002C Dual 4-Input NOR Gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

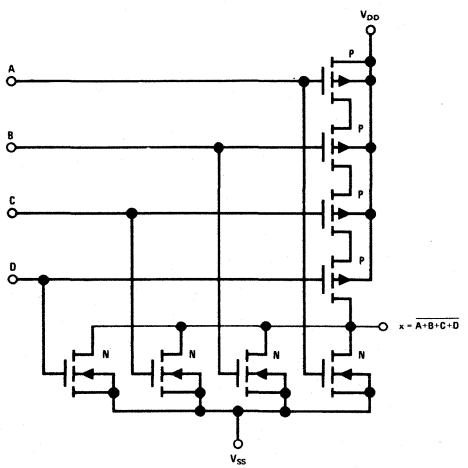
features

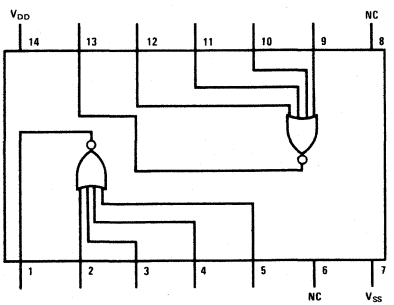
- Wide supply voltage range 3V to 15V
- Low power 10 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

schematic and connection diagrams





TOP VIEW

Voltage at Any Pin (Note 1)		V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range	CD40XXM	–55°C to +125°C
	CD40XXC	–40°C to +85°C
Storage Temperature Range		–65°C to +150°C
Package Dissipation		500mW
Lead Temperature (Soldering, 10 seconds)		300°C
Operating V_{DD} Range		V_{SS} + 3V to V_{SS} + 15V

electrical characteristics

CHARACTERISTICS	TEST CONDITIONS VOLTS		LIMITS														UNITS
			CD4002M							CD4002C							
			–55°C		+25°C			+125°C		–40°C		+25°C			+85°C		
	V_O	V_{DD}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current (I_L)		5		0.5		0.001	0.05		3		0.5		0.005	0.5		15	μA
		10		0.1		0.001	0.1		6		5		0.005	5		30	μA
Quiescent Device Dissipation/Package (P_D)		5		0.25		0.005	0.25		15		2.5		0.025	2.5		75	μW
		10		1		0.01	1		60		50		0.05	50		300	μW
Output Voltage Low Level (V_{OL})		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
High Level (V_{OH})		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
		10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
Noise Immunity (V_{NI}) (All Inputs)	>3.5	5	1.5		1.5	2.25		1.4		1.5		1.5	2.25		1.4		V
	>7.0	10	3		3	4.5		2.9		3		3	4.5		2.9		V
(V_{NH})	<1.5	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
	<3.0	10	2.9		3	4.5		3		2.9		3	4.5		3		V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$ 0.4	5	0.5		0.40			0.28		0.35		0.3	1		0.24		mA
	$V_I = V_{DD}$ 0.5	10	1.1		0.9			0.65		0.72		0.6	2.5		0.48		mA
P-Channel (I_DP)	$V_I = V_{SS}$ 2.5	5	–0.62		–0.5			–0.35		–0.35		–0.3	–2		–0.24		mA
	$V_I = V_{SS}$ 9.5	10	–0.62		–0.5			–0.35		–0.3		–0.25	–1		–0.2		mA
Input Current (I_I)						10							10				pA

Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		CD4002M			CD4002C			
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time:	5	–	35	50	–	35	80	ns
Low-to-High Level (t_{PLH})	10	–	25	40	–	25	55	
High-to-Low Level (t_{PHL})	5	–	35	50	–	35	120	ns
	10	–	25	40	–	25	65	
Transition Time:	5	–	65	125	–	65	200	ns
Low-to-High Level (t_{TLH})	10	–	35	70	–	35	115	
High-to-Low Level (t_{THL})	5	–	65	175	–	65	300	ns
	10	–	35	75	–	35	125	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

National Semiconductor

CD4006M/CD4006C 18-Stage Static Shift Register

general description

The CD4006M/CD4006C 18-stage static shift register is comprised of four separate shift register sections, two sections of four stages and two sections of five stages. Each section has an independent data input. Outputs are available at the fourth stage and the fifth stage of each section. A common clock signal is used for all stages. Data is shifted to the next stage on the negative-going transition of the clock. Through appropriate connections of inputs and outputs, multiple register sections of 4, 5, 8 and 9 stages or single register section of 10, 12, 13, 14, 16, 17, and 18 stages can be implemented using one package.

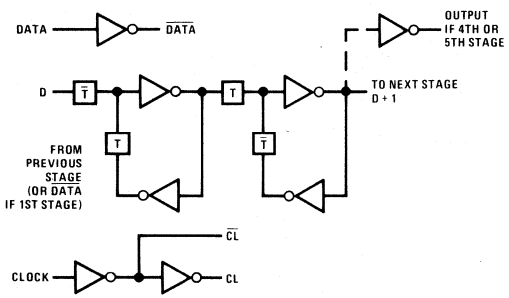
features

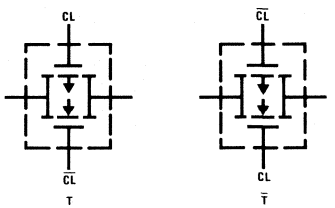
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low clock input capacitance	6 pF typ
■ Medium speed operation	10 MHz typ with V_{DD} = 10V
■ Low power	
■ Fully static operation	

applications

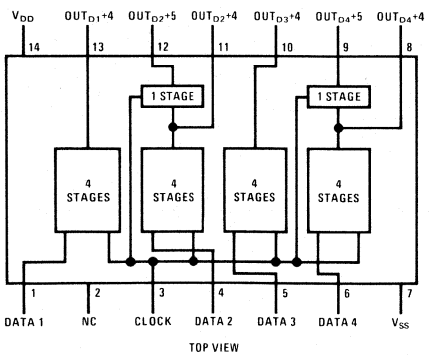
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industry control
- Remote metering
- Computers

logic diagrams





connection diagram



TOP VIEW

truth table

D	CL$^{\Delta}$	D+1
0	⌐	0
1	⌐	1
X	⌐	NC

X = Don't care
Δ = Level change
NC = No change

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4006M	−55°C to +125°C
CD4006C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4006M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.01	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			2.5		0.05	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99				4.99	5	4.95			V
	V_{DD} = 10V	9.99				9.99	10	9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.155			0.125	0.25		0.085			mA
	V_{DD} = 10V, V_O = 0.5V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.125			−0.1	−0.15		−0.07			mA
	V_{DD} = 10V, V_O = 9.5V	−0.25			−0.2	−0.3		−0.14			mA
Input Current (I_I)	Any Input					10					pA

dc electrical characteristics CD4006C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5		0.03	5			70	μA
	V_{DD} = 10V			10		0.05	10			140	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5.0V			25		0.15	25			350	μW
	V_{DD} = 10V			100		0.5	100			1400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V, V_O = 0.5V	0.072			0.06	0.25		0.048			mA
	V_{DD} = 10V, V_O = 0.5V	0.15			0.125	0.5		0.10			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V, V_O = 4.5V	−0.06			−0.05	−0.15		−0.04			mA
	V_{DD} = 10V, V_O = 9.5V	−0.12			−0.1	−0.3		−0.08			mA
Input Current (I_I)	Any Input					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics

CD4006M at $T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

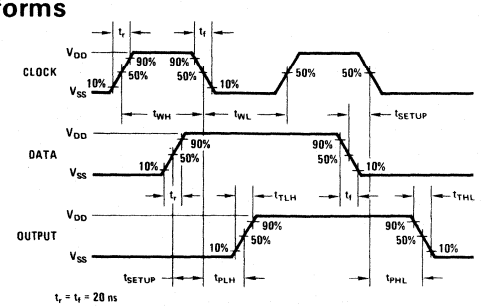
PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5.0V$		180	400	ns
	$V_{DD} = 10V$		80	200	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5.0V$		150	400	ns
	$V_{DD} = 10V$		60	200	ns
Minimum Clock Pulse Width ($T_{WL} = T_{WH}$)	$V_{DD} = 5.0V$		100	500	ns
	$V_{DD} = 10V$		50	200	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			5	μs
Set-Up Time	$V_{DD} = 5.0V$		50	80	ns
	$V_{DD} = 10V$		25	40	ns
Maximum Clock Frequency (f_{cl})	$V_{DD} = 5.0V$	1	5		MHz
	$V_{DD} = 10V$	2.5	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

ac electrical characteristics CD4006C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	$V_{DD} = 5.0V$		180	500	ns
	$V_{DD} = 10V$		80	250	ns
Transition Time ($t_{TLH} = t_{THL}$)	$V_{DD} = 5.0V$		150	400	ns
	$V_{DD} = 10V$		60	250	ns
Minimum Clock Pulse Width ($T_{WH} = T_{WL}$)	$V_{DD} = 5.0V$		100	830	ns
	$V_{DD} = 10V$		50	250	ns
Clock Rise and Fall Time ($t_{rCl} = t_{fCl}$)*	$V_{DD} = 5.0V$			15	μs
	$V_{DD} = 10V$			5	μs
Set-Up Time	$V_{DD} = 5.0V$		50	100	ns
	$V_{DD} = 10V$		25	50	ns
Maximum Clock Frequency (f_{cl})	$V_{DD} = 5.0V$	0.6	5		MHz
	$V_{DD} = 10V$	2	10		MHz
Input Capacitance (C_I)	Data Input		5		pF
	Clock Input		6		pF

*If more than one unit is cascaded t_{rCl} should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output stage for the estimated capacitive load.

switching time waveforms



National Semiconductor

CD4007M/CD4007C Dual Complementary Pair Plus Inverter

general description

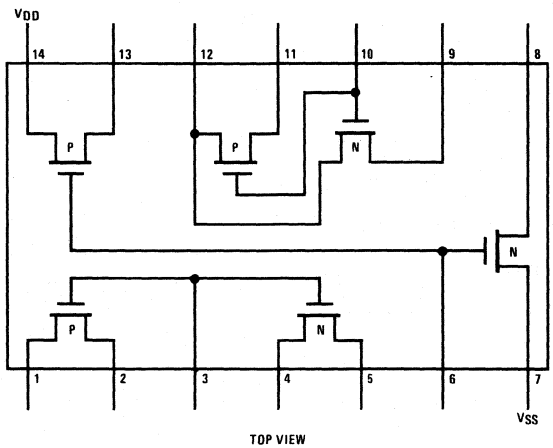
The CD4007M/CD4007C consists of three complementary pairs of N-channel and P-channel enhancement mode MOS transistors suitable for series/shunt applications. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

For proper operation the voltages at all pins must be constrained to be between V_{SS} − 0.3V and V_{DD} + 0.3V at all times.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{CC} typ

connection diagram



TOP VIEW

Note: All P-channel substrates are connected to V_{DD} and all N-channel substrates are connected to V_{SS}.

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4007M	−55°C to +125°C
CD4007C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4007M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.05		0.001	0.05			3	μA
	V_{DD} = 10V			0.1		0.001	0.1			6	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			0.25		0.005	0.25			15	μW
	V_{DD} = 10V			1		0.01	1			60	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.75			0.6	1		0.4			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.6			1.3	2.5		0.95			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.75			−1.4	−4		−1			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−1.35			−1.1	−2.5		−0.75			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4007C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			0.5		0.005	0.5			15	μA
	V_{DD} = 10V			1		0.005	1			30	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			2.5		0.025	2.5			75	μW
	V_{DD} = 10V			10		0.05	10			300	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL}) (All Inputs)	V_{DD} = 5V, V_O = 3.6V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 7.2V	3			3	4.5		2.9			V
Noise Immunity (V_{NH}) (All Inputs)	V_{DD} = 5V, V_O = 0.95V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 2.9V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.4V, V_I = V_{DD}	0.35			0.3	1		0.24			mA
	V_{DD} = 10V, V_O = 0.5V, V_I = V_{DD}	1.2			1	2.5		0.8			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 2.5V, V_I = V_{SS}	−1.3			−1.1	−4		−0.9			mA
	V_{DD} = 10V, V_O = 9.5V, V_I = V_{SS}	−0.65			−0.55	−2.5		−0.45			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4007M

T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

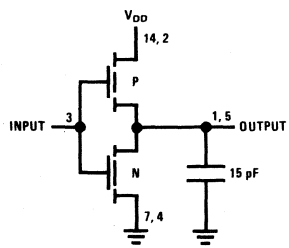
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	60	ns
	V_{DD} = 10V		20	40	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	75	ns
	V_{DD} = 10V		30	40	ns
Input Capacitance (C_I)	Any Input		5		pF

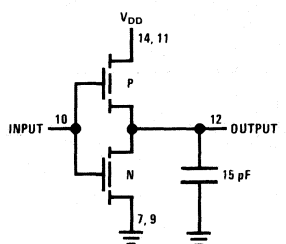
ac electrical characteristics CD4007C

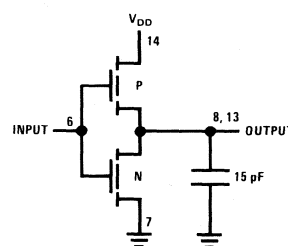
T_A = 25°C and C_L = 15 pF and input rise and fall times = 20 ns. Typical temperature coefficient for all values of V_{DD} = 0.3%/°C.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time ($t_{PLH} = t_{PHL}$)	V_{DD} = 5V		35	75	ns
	V_{DD} = 10V		20	50	ns
Transition Time ($t_{TLH} = t_{THL}$)	V_{DD} = 5V		50	100	ns
	V_{DD} = 10V		30	50	ns
Input Capacitance (C_I)	Any Input		5		pF

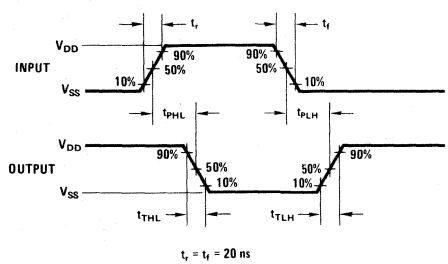
ac test circuits







switching time waveforms



$t_r = t_f$ = 20 ns

National Semiconductor

CD4008BM/CD4008BC 4-Bit Full Adder

general description

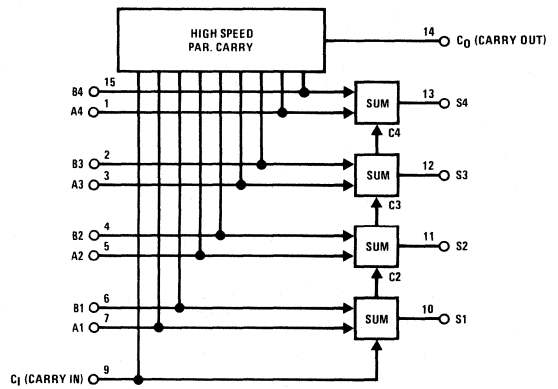
The CD4008B types consist of four full-adder stages with fast look-ahead carry provision from stage to stage. Circuitry is included to provide a fast "parallel-carry-out" bit to permit high-speed operation in arithmetic sections using several CD4008B's. CD4008B inputs include the four sets of bits to be added, A1 to A4 and B1 to B4, in addition to the "Carry In" bit from a previous section. CD4008B outputs include the four sum bits, S1 and S4, in addition to the high-speed "parallel-carry-out" which may be utilized at a succeeding CD4008B section.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and Gnd.

features

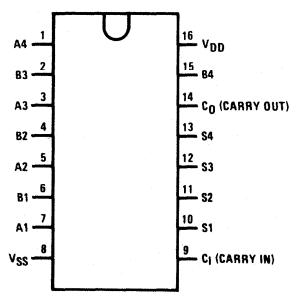
- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 4 sum outputs plus parallel look-ahead carry-output
- Quiescent current specified to 15V
- Maximum input leakage of 1μA at 15V (full package temperature range)

block diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

A_i	B_i	C_i	C0	SUM
0	0	0	0	0
1	0	0	0	1
0	1	0	0	1
1	1	0	1	0
0	0	1	0	1
1	0	1	1	0
0	1	1	1	0
1	1	1	1	1

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4008BM	−55°C to +125°C
CD4008BC	−40°C to +85°C

dc electrical characteristics CD4008BM (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
	V_{DD} = 10V		10		0.5	10		300	μA
	V_{DD} = 15V		20		1.0	20		600	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.35		−0.14		mA
	V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.8		−0.35		mA
	V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4008BC (Note 2)

PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
	V_{DD} = 10V		40		1	40		300	μA
	V_{DD} = 15V		80		5	80		600	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
	V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

dc electrical characteristics (con't) CD4008BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.35		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.8		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3			−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3			0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, input t_r, t_f = 20 ns, unless otherwise specified.

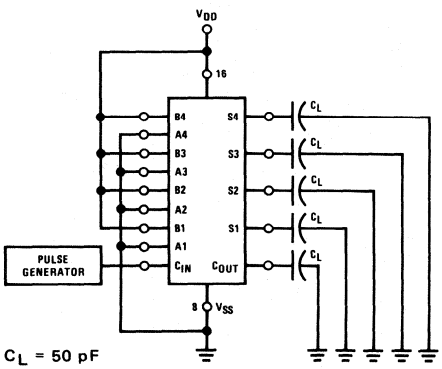
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time					
	Sum In to Sum Out	V_{DD} = 5V		425	750	ns
		V_{DD} = 10V		170	250	ns
		V_{DD} = 15V		125	190	ns
	Carry In to Sum Out	V_{DD} = 5V		320	650	ns
		V_{DD} = 10V		125	225	ns
		V_{DD} = 15V		95	175	ns
	Sum In to Carry Out	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	200	ns
		V_{DD} = 15V		90	160	ns
	Carry In to Carry Out	V_{DD} = 5V		130	245	ns
		V_{DD} = 10V		60	105	ns
		V_{DD} = 15V		45	80	ns
	Carry In to Carry Out	C_L = 15 pF				
		V_{DD} = 5V		100	175	ns
		V_{DD} = 10V		45	75	ns
		V_{DD} = 15V		35	60	ns
t_{THL}	High-to-Low Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Transition Time	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
C_{IN}	Average Input Capacitance			5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Note 3		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

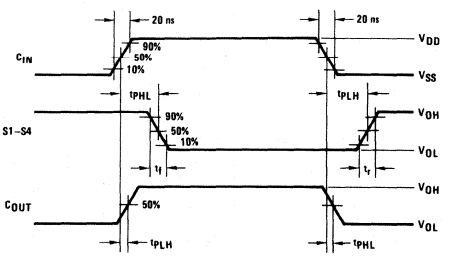
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

ac test circuit and switching time waveforms



C_L = 50 pF



National Semiconductor

CD4009M/CD4009C Hex Buffers (Inverting)
CD4010M/CD4010C Hex Buffers (Non-Inverting)

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge. These gates may be used as hex buffers, CMOS to DTL or TTL interface or as CMOS current drivers. Conversion ranges are from 3 to 15 volts providing $V_{CC} \leq V_{DD}$.

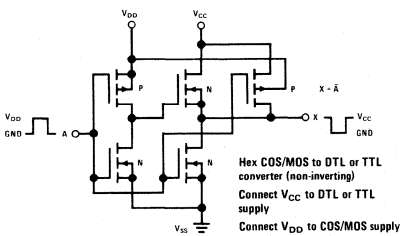
features

- Wide supply voltage range 3V to 15V
- Low power 100 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)
- High current sinking capability 8 mA (min) at VO = 0.5V and V_{DD} = 10V

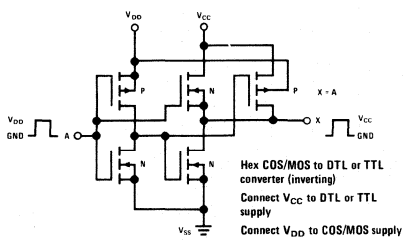
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial controls
- Remote metering
- Computers

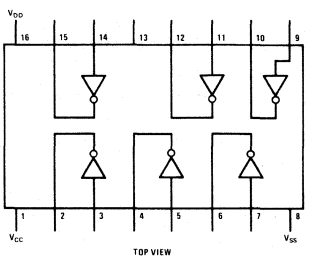
schematic and connection diagrams



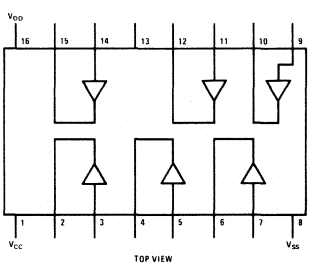
CD4009M/CD4009C



CD4010M/CD4010C



TOP VIEW



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD40XXM	–55°C to +125°C
CD40XXC	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Package Dissipation	500mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

dc electrical characteristics

CHARACTERISTICS	TEST CONDITIONS VOLTS		LIMITS														UNITS
			CD40XXM							CD40XXC							
			–55°C		+25°C			+125°C		–40°C		+25°C			+125°C		
	V_O	V_{DD}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current		5		0.3		0.01	0.3		20		3		0.03	3		42	μA
(I_L)		10		0.5		0.01	0.5		30		5		0.05	5		70	μA
Quiescent Device		5		1.5		0.05	1.5		100		15		0.15	15		210	μW
Dissipation/Package (P_D)		10		5		0.1	5		300		50		0.5	50		700	μW
Output Voltage		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
Low Level (V_{OL})		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
High Level (V_{OH})		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
		10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
Noise Immunity (All Inputs)																	
(V_{NL}) CD4009M	$V_O \geqslant 4.0$	5	1		1	2.25		0.9		1		1	2.25		0.9		V
	$V_O \geqslant 8.0$	10	2		2	4.5		1.9		2		2	4.5		1.9		V
(V_{NL}) CD4010M	$V_O \geqslant 1.5$	5	1.6		1.5	2.25		1.4		1.6		1.5	2.25		1.4		V
	$V_O \geqslant 3.0$	10	3.2		3	4.5		2.9		3.2		3	4.5		2.9		V
(V_{NH})	$V_O \geqslant 3.5$	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
	$V_O \geqslant 7.0$	10	2.9		3	4.5		3		2.9		3	4.5		3		V
Output Drive Current	0.4	5	3.75		3	4		2.1		3.6		3			2.4		mA
N-Channel (I_DN)	0.5	10	10		8	10		5.6		9.6		8			6.4		mA
P-Channel (I_DP)	2.5	5	–1.85		–1.25	–1.75		–0.9		–1.5		–1.25			–1		mA
	9.5	10	–0.9		–0.6	–0.8		–0.4		–0.72		–0.6			–0.48		mA
Input Current (I_I)						10							10				pA

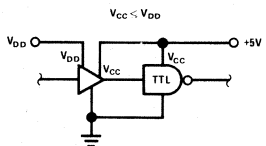
Note 1: This device should not be connected to circuits with the power on because high transient voltage may cause permanent damage.

ac electrical characteristics at T_A = 25°C and C_L = 15 pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTIC	TEST CONDITIONS		LIMITS						UNITS
			CD40XXM			CD40XXC			
		V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time:									
High-to-Low Level (t_{PHL})	$V_{CC} = V_{DD}$	5	–	15	55		15	70	
		10	–	10	30		10	40	ns
	V_{DD} = 10V								
	V_{CC} = 5V		–	10	25	–	10	35	
Low-to-High Level (t_{PLH})		5	–	50	80	–	50	100	
	$V_{CC} = V_{DD}$	10	–	25	55	–	25	70	ns
	V_{DD} = 10V								
	V_{CC} = 5V		–	15	30	–	15	40	
Transition Time:									
High-to-Low Level (t_{THL})	$V_{CC} = V_{DD}$	5	–	20	45	–	20	60	ns
		10	–	16	40	–	16	50	
Low-to-High Level (t_{TLH})		5	–	80	125	–	80	160	
	$V_{CC} = V_{DD}$	10	–	50	100	–	50	120	ns
Input Capacitance (C_I)	Any Input		–	5	–	–	5	–	pF

typical applications



National Semiconductor

CD4011M/CD4011C Quad 2-Input NAND Gate
CD4012M/CD4012C Dual 4-Input NAND Gate
CD4023M/CD4023C Triple 3-Input NAND Gate

general description

These NAND gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No DC power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

features

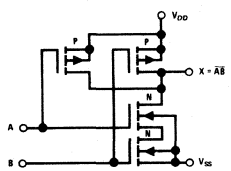
- Wide supply voltage range 3V to 15V
- Low power 10 nW (typical)
- High noise immunity 0.45 V_{DD} (typical)

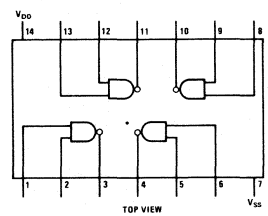
applications

- Automotive
- Data Terminals
- Instrumentation
- Medical Electronics
- Alarm System
- Industrial Controls
- Remote Metering
- Computers

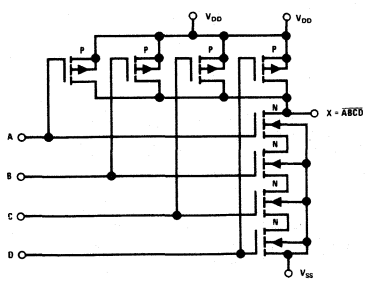
schematic and connection diagrams

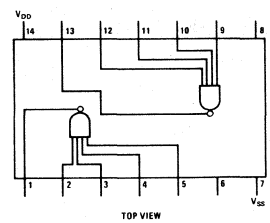
CD4011M/CD4011C SCHEMATIC



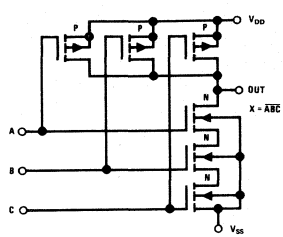


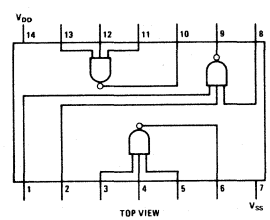
CD4012M/CD4012C SCHEMATIC





CD4023M/CD4023C SCHEMATIC





absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD40XXM	−55°C to +125°C
CD40XXC	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500mW
Lead Temperature (Soldering, 10 seconds)	300°C
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V

dc electrical characteristics

CHARACTERISTICS	TEST COND. VOLTS		LIMITS														UNITS
			CD40XXM							CD40XXC							
			−55°C		+25°C			+125°C		−40°C		+25°C			+85°C		
	V_O	V_{DD}	MIN	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX	
Quiescent Device Current (I_L)		5		0.05		0.001	0.05		3		0.5		0.005	0.5		15	μA
		10		0.1		0.001	0.1		6		5		0.005	5		30	μA
Quiescent Device Dissipation/Package (P_D)		5		0.25		0.005	0.25		15		2.5		0.025	2.5		75	μW
		10		1		0.01	1		60		50		0.05	50		300	μW
Output Voltage Low Level (V_{OL})		5		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
		10		0.01		0	0.01		0.05		0.01		0	0.01		0.05	V
High Level (V_{OH})		5	4.99		4.99	5		4.95		4.99		4.99	5		4.95		V
		10	9.99		9.99	10		9.95		9.99		9.99	10		9.95		V
Noise Immunity (All Inputs) (V_{NL})	⩾3.5	5	1.5		1.5	2.25		1.4		1.5		1.5	2.25		1.4		V
	⩾7.0	10	3		3	4.5		2.9		3		3	4.5		2.9		V
(V_{NH})	⩽1.5	5	1.4		1.5	2.25		1.5		1.4		1.5	2.25		1.5		V
	⩽3.0	10	2.9		3	4.5		3		2.9		3	4.5		3		V
Output Drive Current N-Channel (I_DN)	0.5	5	0.31		0.25	0.5		0.175		0.145		0.12	0.5		0.95		mA
	0.5	10	0.63		0.5	0.6		0.35		0.3		0.25	0.6		0.2		mA
P-Channel (I_DP)	4.5	5	−0.31		−0.25	−0.5		−0.175		−0.145		−0.12	−0.5		0.095		mA
	9.5	10	−0.75		−0.6	−1.2		−0.4		−0.35		−0.3	−1.2		−0.24		mA
Input Current (I_I)						10							10				pA

ac electrical characteristics @ T_A = 25°C and C_L = 15pF

Typical Temperature Coefficient for all values of V_{DD} = 0.3%/°C

CHARACTERISTICS	TEST CONDITIONS	LIMITS						UNITS
		CD40XXM			CD40XXC			
	V_{DD} (VOLTS)	MIN	TYP	MAX	MIN	TYP	MAX	
Propagation Delay Time: Low-to-High Level (t_{PLH})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
High-to Low Level (t_{PHL})	5	–	50	75	–	50	100	ns
	10	–	25	40	–	25	50	
Transition Time: Low-to-High Level (t_{TLH})	5	–	75	100	–	75	125	ns
	10	–	40	60	–	40	75	
High-to-Low Level (t_{THL})	5	–	75	125	–	75	150	ns
	10	–	50	75	–	50	100	
Input Capacitance (C_I)	Any Input	–	5	–	–	5	–	pF

National Semiconductor

CD4013BM/CD4013BC Dual D Flip-Flop

general description

The CD4013B dual D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P channel enhancement transistors. Each flip-flop has independent data, set, reset, and clock inputs and "Q" and "$\overline{Q}$" outputs. These devices can be used for shift register applications, and by connecting "$\overline{Q}$" output to the data input, for counter and toggle applications. The logic level present at the "D" input is transferred to the Q output during the positive-going transition of the clock pulse. Setting or resetting is independent of the clock and is accomplished by a high level on the set or reset line respectively.

features

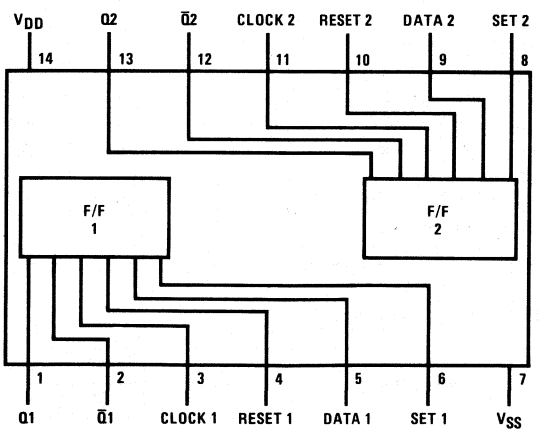
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm system
- Industrial electronics
- Remote metering
- Computers

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

CL↑	D	R	S	Q	$\overline{Q}$
⌐¯	0	0	0	0	1
⌐¯	1	0	0	1	0
¯⌐	x	0	0	Q	$\overline{Q}$
x	x	1	0	0	1
x	x	0	1	1	0
x	x	1	1	1	1

No change
↑ = Level change
x = Don't care case

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4013BM	−55°C to +125°C
CD4013BC	−40°C to +85°C

dc electrical characteristics CD4013BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4013BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

dc electrical characteristics (con't) CD4013BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

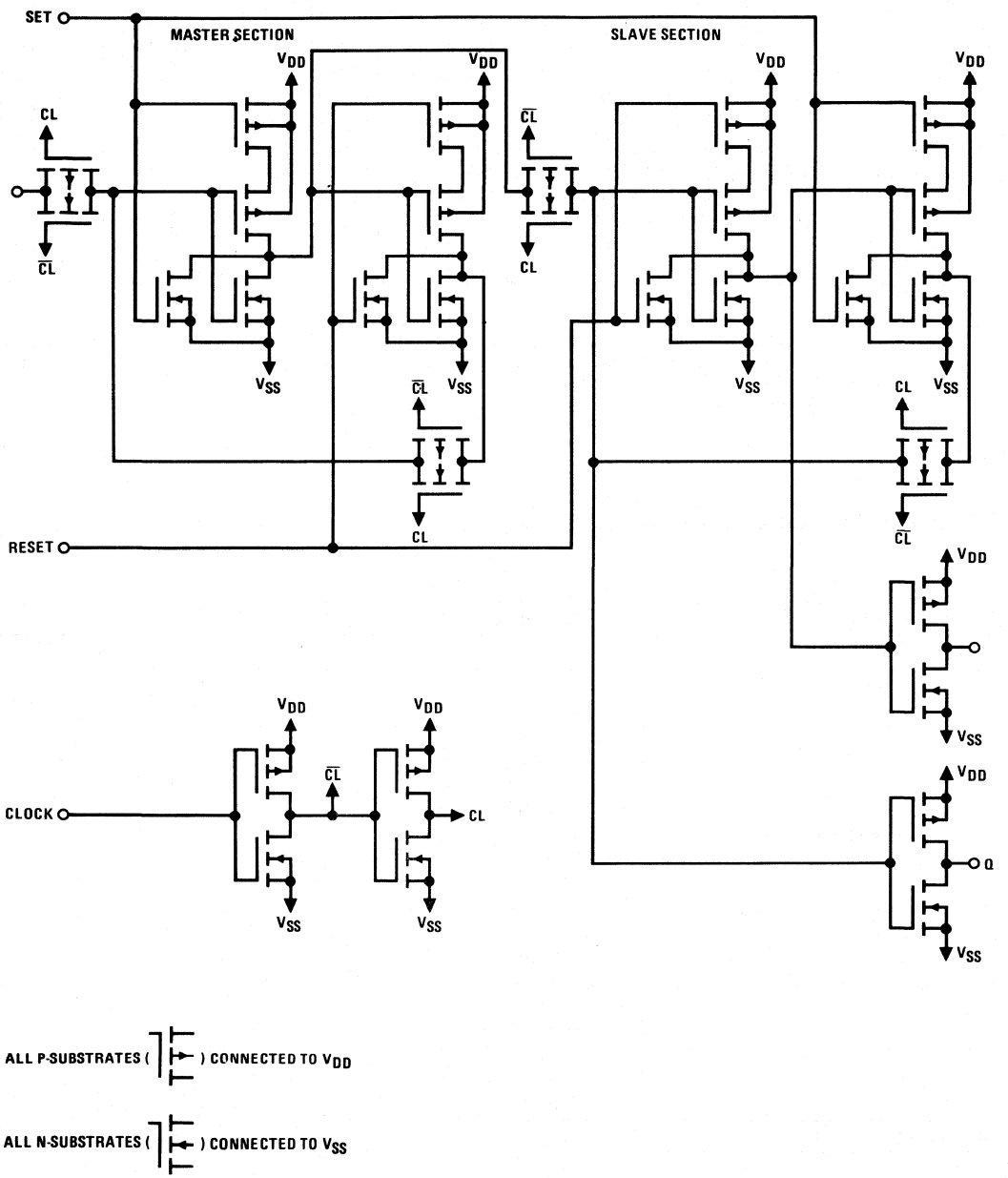
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

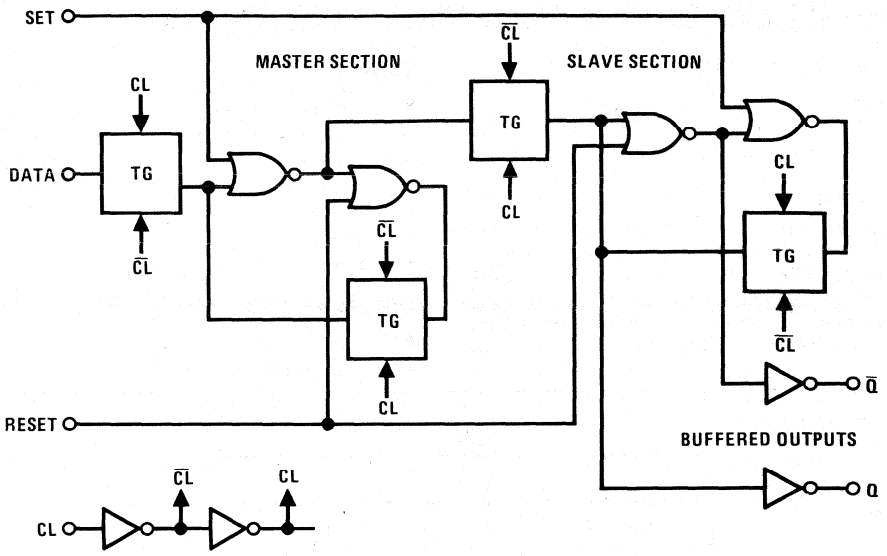
ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, or	Propagation Delay Time	V_{DD} = 5V		200	350	ns
t_{PLH}		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	120	ns
t_{THL}, or	Transition Time	V_{DD} = 5V		100	200	ns
t_{TLH}		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, or	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
t_{WH}		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		20	40	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
SET AND RESET OPERATION						
$t_{PHL(R)}$,	Propagation Delay Time	V_{DD} = 5V		150	300	ns
$t_{PLH(S)}$		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		45	90	ns
$t_{WH(R)}$,	Minimum Set and Reset	V_{DD} = 5V		90	180	ns
$t_{WH(S)}$	Pulse Width	V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

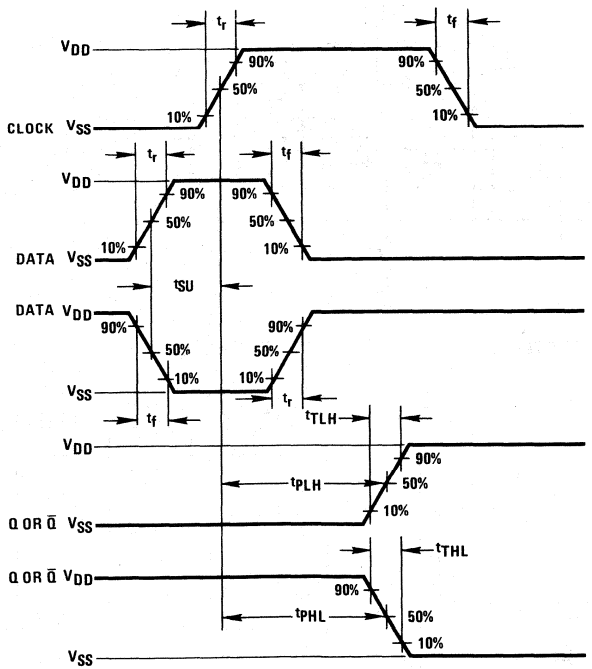
schematic diagram



logic diagram



switching time waveforms



National Semiconductor

CD4014M/CD4014C 8-Stage Static Shift Register

general description

The CD4014M/CD4014C is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control input is in the logical "1" state, data is jammed into each stage of the register synchronously with the positive transition of the clock.

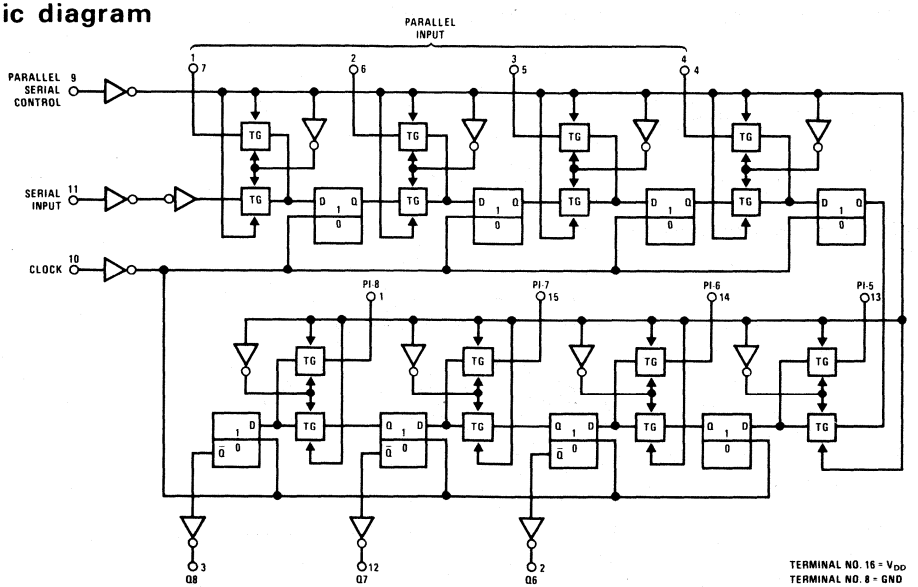
features

- Synchronous operation
- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Medium speed operation — 5 MHz typ
  clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation
- Low power

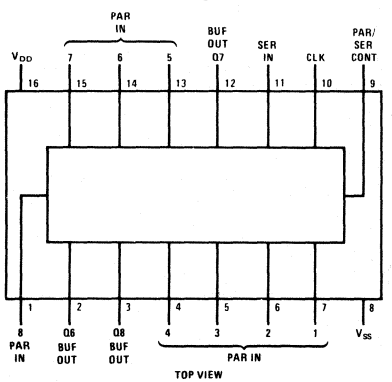
applications

- Parallel to serial conversion
- General purpose register

logic diagram



connection diagram



truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
⌐	X	1	0	0	0	0	
⌐	X	1	1	0	1	0	
⌐	X	1	0	1	0	1	
⌐	X	1	1	1	1	1	
⌐	0	0	X	X	0	$Q_{n\,1}$	
⌐	1	0	X	X	1	$Q_{n\,1}$	
⌙	X	X	X	X	Q1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4014M	−55°C to +125°C
CD4014C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4014M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	μA
	V_{DD} = 10V			10		1	10			600	μA
Quiescent Device Dissipation	V_{DD} = 5V			25		2.5	25			1,500	μW
Package (P_D)	V_{DD} = 10V			100		10	100			6,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.1			−0.08	−0.16		−0.055			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4014C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1,400	μA
Quiescent Device Dissipation	V_{DD} = 5V			250		2.5	250			3,500	μW
Package (P_D)	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.06			−0.05	−0.16		−0.04			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4014M

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	350	ns
	V_{DD} = 10V		50	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	2.5		MHz
	V_{DD} = 10V	3	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

ac electrical characteristics CD4014C

PARAMETERS	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	1,000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	2.5		MHz
	V_{DD} = 10V	2.5	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

National Semiconductor

CD4015M/CD4015C Dual 4-Bit Static Shift Register

general description

The CD4015M/CD4015C consist of two identical, independent, 4-stage serial-input/parallel-output registers. Each register has independent "Clock" and "Reset" inputs as well as a single serial "Data" input. "Q" outputs are available from each of the four stages on both registers. All register stages are D-type, master-slave flip-flops. The logic level present at the data input is transferred into the first register stage and shifted over one stage at each positive-going clock transition. Resetting of all stages is accomplished by a high level on the reset line. Register expansion to 8 stages using one CD4015M/CD4015C package, or to more than 8 stages using additional CD4015M/CD4015C is possible. All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

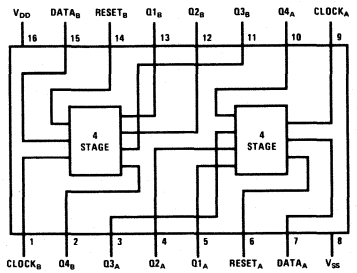
features

- Wide supply voltage range — 3.0V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Medium speed operation — 9 MHz (typ) clock rate at $V_{DD} - V_{SS} = 10V$
- Fully static operation

applications

- Serial-input/parallel-output data queueing
- Serial to parallel data conversion
- General purpose register

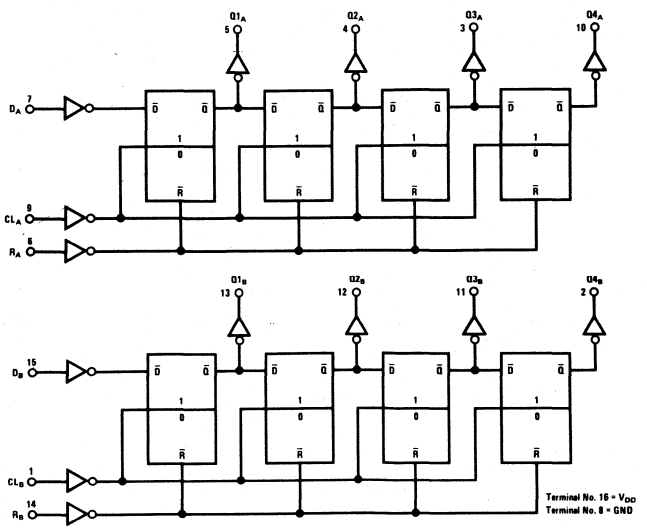
connection diagram and truth table



CL▲	D	R	Q1	Q_n	
⌐⌐	0	0	0	Q_{n-1}	
⌐⌐	1	0	1	Q_{n-1}	
⌐⌐	X	0	Q1	Q_n	(No change)
X	X	1	0	0	

▲ Level change.
X Don't care case.

logic diagrams



absolute maximum ratings (Note 1)

Voltage at Any Pin V_{SS} − 0.3V to V_{DD} + 0.3V

Operating Temperature Range

CD4015M −55°C to +125°C

CD4015C −40°C to +85°C

Storage Temperature Range −65°C to +150°C

Package Dissipation 500 mW

Operating $V_{DD} - V_{SS}$ Range 3.0V to 15V

Lead Temperature (Soldering, 10 seconds) 300°C

dc electrical characteristics CD4015M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	μA
	V_{DD} = 10V			10		1	10			600	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			25		2.5	25			1500	μW
	V_{DD} = 10V			100		10	100			6000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (Any Input) (V_{NL})	V_{DD} = 5V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3			3	4.5		2.9			V
Noise Immunity (Any Input) (V_{NH})	V_{DD} = 5V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.5V	0.15			0.12	0.3		0.085			mA
	V_{DD} = 10V, V_O = 0.5V	0.31			0.25	0.5		0.175			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 4.5V	−0.1			−0.08	−0.16		−0.055			mA
	V_{DD} = 10V, V_O = 9.5V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4015C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1400	μA
Quiescent Device Dissipation/Package (P_D)	V_{DD} = 5V			250		2.5	250			3500	μW
	V_{DD} = 10V			1000		10	1000			14000	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5V	4.99			4.99	5		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (Any Input (V_{NL})	V_{DD} = 5V, V_O = 0.8V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V, V_O = 1.0V	3			3	4.5		2.9			V
Noise Immunity (Any Input (V_{NH})	V_{DD} = 5V, V_O = 4.2V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V, V_O = 9.0V	2.9			3	4.5		3			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5V, V_O = 0.5V	0.072			0.06	0.3		0.05			mA
	V_{DD} = 10V, V_O = 0.5V	0.12			0.1	0.5		0.08			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5V, V_O = 4.5V	−0.06			−0.05	−0.16		−0.04			mA
	V_{DD} = 10V, V_O = 9.5V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

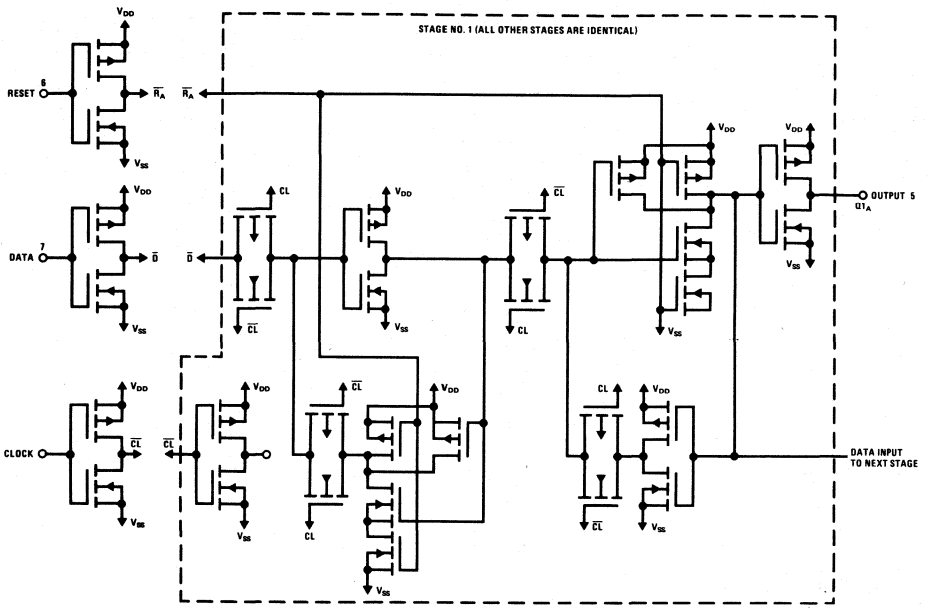
ac electrical characteristics CD4015M

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		250	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	175	ns
Clock Rise and Fall Time (t_{rCL}, t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-Up Time	V_{DD} = 5V		50	350	ns
	V_{DD} = 10V		25	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	4		MHz
	V_{DD} = 10V	3	9		MHz
Input Capacitance (C_I)			5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	750	ns
	V_{DD} = 10V		100	225	ns
Minimum Set and Reset Pulse Widths ($t_{WH(R)}$)	V_{DD} = 5V		150	500	ns
	V_{DD} = 10V		100	175	ns

ac electrical characteristics CD4015C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
CLOCKED OPERATION					
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		250	1000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		100	830	ns
	V_{DD} = 10V		50	200	ns
Clock Rise and Fall Time	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-Up Time	V_{DD} = 5V		50	500	ns
	V_{DD} = 10V		25	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	4		MHz
	V_{DD} = 10V	2.5	9		MHz
Input Capacitance (C_I)			5		pF
RESET OPERATION					
Propagation Delay Time ($t_{PHL(R)}$)	V_{DD} = 5V		200	1000	ns
	V_{DD} = 10V		100	300	ns
Minimum Set and Reset Pulse Widths ($t_{WH(R)}$)	V_{DD} = 5V		150	830	ns
	V_{DD} = 10V		100	200	ns

schematic diagram



National Semiconductor

CD4016M/CD4016C Quad Bilateral Switch

general description

The CD4016M/CD4016C is a quad bilateral switch which utilizes P-channel and N-channel complementary MOS (CMOS) circuits to provide an extremely high "OFF" resistance and low "ON" resistance switch. The switch will pass signals in either direction and is extremely useful in digital switching.

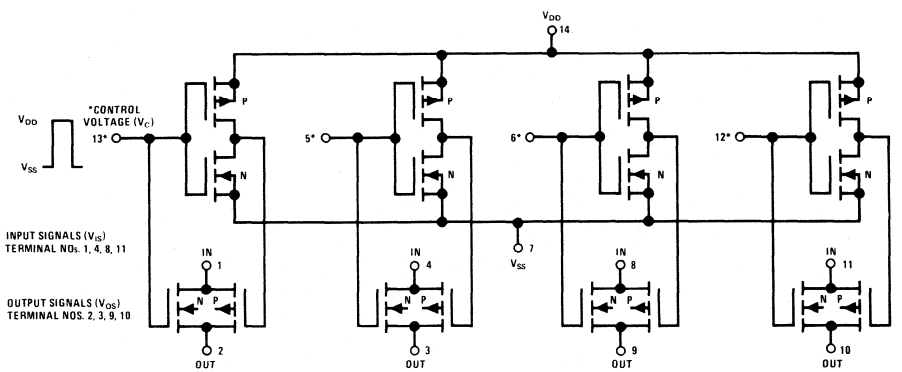
features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{CC} typ.
■ Wide range of digital and analog levels	±7.5 V_{PEAK}
■ Low "ON" resistance	300Ω typ. $V_{DD} - V_{SS} = 15V$
■ Matched switch characteristics	$\Delta R_{ON} = 40\Omega$ typ.
■ High "ON/OFF" output voltage ratio	65 dB typ. @ $f_{is} = 10$ kHz $R_L = 10k$
■ High degree of linearity	.5% distortion typ. @ $f_{is} = 1$ kHz
■ Extremely low leakage	$V_{is} = 5\ V_{p-p}$ $V_{DD} - V_{SS} = 10V$ $R_L = 10\ k\Omega$
■ Transmits frequencies up to 10 MHz	

applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator
  - Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog to digital/digital to analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

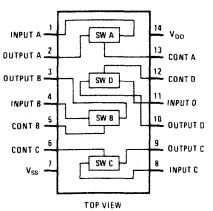
schematic and connection diagrams



Note 1: All switch P-channel substrates are internally connected to terminal No. 14.
Note 2: All switch N-channel substrates are internally connected to terminal No. 7.

Signal-level range: $V_{SS} < V_{is} > V_{DD}$

Normal operation: Control-line biasing, switch ON V_C "1" = V_{DD}, switch OFF V_C "0" = V_{SS}



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1) V_{SS} – 0.3V to V_{SS} + 15.5V
Operating Temperature Range CD4016M –55°C to +125°C
CD4016C –40°C to +85°C
Storage Temperature Range –65°C to +150°C
Package Dissipation 500mW
Lead Temperature (Soldering, 10 seconds) 300°C
Operating V_{DD} Range V_{SS} + 3V to V_{SS} + 15V

electrical characteristics CD4016M

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS –55°C MIN	LIMITS –55°C TYP	LIMITS –55°C MAX	LIMITS 25°C MIN	LIMITS 25°C TYP	LIMITS 25°C MAX	LIMITS 125°C MIN	LIMITS 125°C TYP	LIMITS 125°C MAX	UNITS
Quiescent Dissipation per Package	P_T	TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 GND; V_{is} 1, 4, 8, 11 ≤ +10; V_{os} 2, 3, 9, 10 ≤ +10										
All Switches "OFF"					5		0.1	5			300	μW
All Switches "ON"		TERMINALS / VOLTS APPLIED: V_{DD} 14 +10; V_{SS} 7 GND; V_C 5, 6, 12, 13 +10; $V_{is} = V_{OS}$ 1-4, 8-11 < +10			5		0.1	5			300	μW
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		–1.7			–1.5			–1.3		V
SIGNAL INPUTS (V_{is}) AND OUTPUTS (V_{os})												
"ON" Resistance	R_{ON}	R_L = 10kΩ; V_C = V_{DD}, V_{SS}, V_{is}: +7.5V: +7.5V, –7.5V, –7.5V		120	360		200	400		300	600	Ω
		+7.5V, –7.5V, ±0.25V		130	775		280	850		470	1230	Ω
		+5V		130	600		250	660		400	960	Ω
		+5V, –5V, –5V		130	600		250	660		400	960	Ω
		+5V, –5V, ±0.25V		325	1870		580	2000		900	2600	Ω
		+15V		120	360		200	400		300	600	Ω
		+15V, 0V, +0.25V		120	360		200	400		300	600	Ω
		9.3V		150	775		300	850		490	1230	Ω
		+10V		130	600		250	660		400	960	Ω
		+10V, 0V, +0.25V		130	600		250	660		400	960	Ω
		5.6V		300	1870		560	2000		880	2600	Ω
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V, –7.5V, ±7.5V					10					Ω
		+5V, –5V, ±5V					15					Ω
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz; +5V, –5V, 5V(p-p) (Note 3)					0.4					%
Input or Output Leakage–Switch "OFF" (Effective "OFF" Resistance)		V_{DD} +7.5V: V_C = V_{SS} = –7.5V; V_{is} +7.5V / –7.5V					±100					pA
		V_{DD} +7.5V: V_C = V_{SS} = –7.5V; V_{is} +7.5V / –7.5V					±100					pA
		V_{DD} +5V: V_C = V_{SS} = –5V; V_{is} +5V / –5V					(Note 2)	125				nA
		V_{DD} +5V: V_C = V_{SS} = –5V; V_{is} +5V / –5V					(Note 2)	125				nA
Frequency Response–Switch "ON" (Sine Wave Input)		V_C = V_{DD} = +5V, V_{SS} = –5V; R_L = 1 kΩ; V_{is} = 5V(p-p); $20 \log_{10} \frac{V_{os}}{V_{is}} = -3$ dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, V_C = V_{SS} = –5V; $20 \log_{10} \frac{V_{os}}{V_{is}} = -50$ dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at –50 dB)		R_L = 1 kΩ; $V_{is}(A)$ = 5V(p-p); $V_C(A)$ = V_{DD} = +5V, $V_C(B)$ = V_{SS} = –5V; $20 \log_{10} \frac{V_{os}(B)}{V_{is}(A)} = -50$ dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, V_C = V_{SS} = –5V					4					pF
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					pF
Propagation Delay Signal Input to Signal Output	t_{pd}	V_C = V_{DD} = +10V, V_{SS} = GND, C_L = 15 pF; V_{is} = 10V (square wave); t_r = t_f = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA	0.7		2.9	0.5	1.5	2.7	0.2		2.4	V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V; $V_C < V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk – Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V; V_C = 10V (square wave); R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	t_{rc} = t_{fc} = 20 ns; V_{is} < 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), t_r = t_f = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. **Note 2:** ±10 x 10^{-3}. **Note 3:** Symmetrical about 0V.

electrical characteristics CD4016C

CHARACTERISTIC	SYMBOL	TEST CONDITIONS	LIMITS –40°C MIN	–40°C TYP	–40°C MAX	25°C MIN	25°C TYP	25°C MAX	85°C MIN	85°C TYP	85°C MAX	UNITS
Quiescent Dissipation per Package												
		TERMINALS — VOLTS APPLIED										
		V_{DD} — 14 — +10										
All Switches "OFF"		V_{SS} — 7 — GND										
		V_C — 5, 6, 12, 13 — GND			5		0.1	5			80	μW
		V_{is} — 1, 4, 8, 11 — ≤ +10										
	P_T	V_{os} — 2, 3, 9, 10 — ≤ +10										
		TERMINALS — VOLTS APPLIED										
		V_{DD} — 14 — +10										
All Switches "ON"		V_{SS} — 7 — GND			5		0.1	5			80	μW
		V_C — 5, 6, 12, 13 — +10										
		$V_{is} = V_{OS}$ — 1-4, 8-11 — ≤ +10										
Threshold Voltage N-Channel	$V_{TH}N$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		1.7			1.5			1.3		V
P-Channel	$V_{TH}P$	I_{DS} = 10 μA, V_{DD} = 5V, 10V, or 15V		-1.7			-1.5			-1.3		V
SIGNAL INPUTS (V_S) AND OUTPUTS (V_{OS})												
		$V_C = V_{DD}$ — V_{SS} — V_{is}										
							+7.5V					
		+7.5V — -7.5V — -7.5V		130	370		200	400		260	520	Ω
							±0.25V					
				160	790		280	850		400	1080	
							+5V					
		+5V — -5V — -5V		150	610		250	660		340	840	Ω
							±0.25V					
"ON" Resistance	R_{ON}	R_L = 10kΩ		370	1900		580	2000		770	2380	
							+15V					
		+15V — 0V — +0.25V		130	370		200	400		260	520	Ω
							9.3V					
				180	790		300	850		400	1080	
							+10V					
		+10V — 0V — +0.25V		150	610		250	660		340	2380	Ω
							5.6V					
				350	1900		560	2000		750	2380	
Δ "ON" Resistance Between Any 2 of 4 Switches	ΔR_{ON}	+7.5V — -7.5V — ±7.5V					10					Ω
		+5V — -5V — ±5V					15					
Sine Wave Response (Distortion)		R_L = 10 kΩ, f_{is} = 1 kHz — +5V — -5V — 5V(p-p) (Note 3)					0.4					%
		V_{DD} — $V_C = V_{SS}$ — V_{is}										
Input or Output Leakage—Switch "OFF" (Effective "OFF" Resistance)		+7.5V — -7.5V — +7.5V					±100					pA
		+7.5V — -7.5V — -7.5V					±100					
		+5V — -5V — +5V					(Note 2)	125				nA
		+5V — -5V — -5V					(Note 2)	125				
Frequency Response—Switch "ON" (Sine Wave Input)		$V_C = V_{DD}$ = +5V, V_{SS} = -5V; R_L = 1 kΩ, V_{is} = 5V(p-p); 20 $\log_{10} \frac{V_{os}}{V_{is}}$ = -3 dB					40					MHz
Feedthrough Switch "OFF"		V_{DD} = +5V, $V_C = V_{SS}$ = -5V; 20 $\log_{10} \frac{V_{os}}{V_{is}}$ = -50 dB					1.25					MHz
Crosstalk Between any 2 of the 4 switches (Frequency at -50 dB)		R_L = 1 kΩ, $V_{is}(A)$ = 5V(p-p); $V_C(A) = V_{DD}$ = +5V, $V_C(B) = V_{SS}$ = -5V; 20 $\log_{10} \frac{V_{os}(B)}{V_{is}(A)}$ = -50 dB					0.9					MHz
Capacitance Input	C_{IS}	V_{DD} = +5V, $V_C = V_{SS}$ = -5V					4					
Output	C_{OS}						4					pF
Feedthrough	C_{IOS}						0.2					
Propagation Delay Signal Input to Signal Output	t_{pd}	$V_C = V_{DD}$ = +10V, V_{SS} = GND, C_L = 15 pF, V_{is} = 10V (square wave), $t_r = t_f$ = 20 ns (input signal)					10					ns
CONTROL (V_C)												
Switch Threshold Voltage	$V_{TH}C$	$V_{is} \leq V_{DD}$; $V_{DD} - V_{SS}$ = 15V, 10V, 5V; I_{IS} = 10 μA				0.5	1.5	2.7				V
Input Current	I_C	$V_{DD} - V_{SS}$ = 10V, $V_C \leq V_{DD} - V_{SS}$					±10					pA
Average Input Capacitance	C_C						5					pF
Crosstalk — Control Input to Signal Output		$V_{DD} - V_{SS}$ = 10V, V_C = 10V (square wave), R_L = 10 kΩ					50					mV
Turn "ON" Propagation Delay	$t_{pd}C$	$t_{rc} = t_{fc}$ = 20 ns, $V_{is} \leq$ 10V, C_L = 15 pF					20					ns
Maximum Allowable Control Input Repetition Rate		V_{DD} = 10V, V_{SS} = GND, R_L = 1 kΩ, C_L = 15 pF, V_C = 10V (square wave), $t_r = t_f$ = 20 ns					10					MHz

Note 1: The device should not be connected to circuits with the power on. **Note 2:** $\pm 10 \times 10^{-3}$. **Note 3:** Symmetrical about 0 V.

typical ON resistance characteristics

CHARACTERISTIC*	SUPPLY CONDITIONS		LOAD CONDITIONS					
			R_L = 1 kΩ		R_L = 10 kΩ		R_L = 100 kΩ	
	V_{DD} (V)	V_{SS} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)	VALUE (Ω)	V_{is} (V)
R_{ON}	+15	0	200	+15	200	+15	180	+15
			200	0	200	0	200	0
R_{ON} (max.)	+15	0	300	+11	300	+9.3	320	+9.2
R_{ON}	+10	0	290	+10	250	+10	240	+10
			290	0	250	0	300	0
R_{ON} (max.)	+10	0	500	+7.4	560	+5.6	610	+5.5
R_{ON}	+5	0	860	+5	470	+5	450	+5
			600	0	580	0	800	0
R_{ON} (max.)	+5	0	1.7k	+4.2	7k	+2.9	33k	+2.7
R_{ON}	+7.5	−7.5	200	+7.5	200	+7.5	180	+7.5
			200	−7.5	200	−7.5	180	−7.5
R_{ON} (max.)	+7.5	−7.5	290	±0.25	280	±25	400	±0.25
R_{ON}	+5	−5	260	+5	250	+5	240	+5
			310	−5	250	−5	240	−5
R_{ON} (max.)	+5	−5	600	±0.25	580	±0.25	760	±0.25
R_{ON}	+2.5	−2.5	590	+2.5	450	+2.5	490	+2.5
			720	−2.5	520	−2.5	520	−2.5
R_{ON} (max.)	+2.5	−2.5	232k	±0.25	300k	±0.25	870k	±0.25

*Variation from a perfect switch: $R_{ON} = 0\Omega$.

National Semiconductor

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

general description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

features

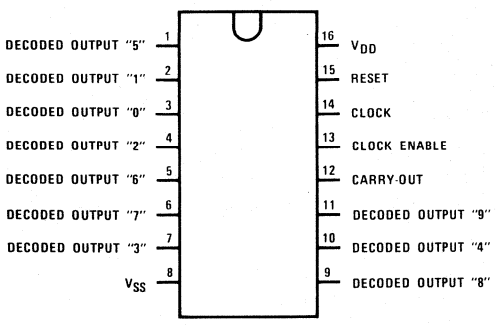
■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	5.0 MHz typ with 10V V_{DD}
■ Low power	10μW typ
■ Fully static operation	

applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

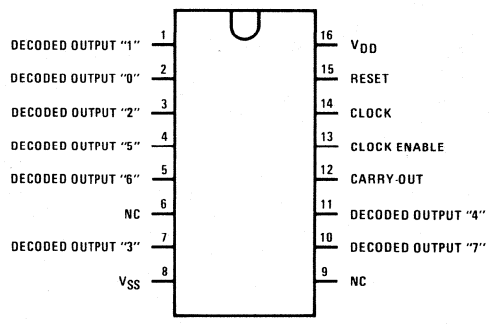
connection diagrams

CD4017B
Dual-In-Line and Flat Package



TOP VIEW

CD4022B
Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4017BM, CD4022BM	−55°C to +125°C
CD4017BC, CD4022BC	−40°C to +85°C

dc electrical characteristics CD4017BM, CD4022BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4017BC, CD4022BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (con't) CD4017BC, CD4022BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} and t_{fCL} = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time:					
	Carry Out Line	V_{DD} = 5V		415	830	ns
		V_{DD} = 10V		160	320	ns
		V_{DD} = 15V		130	260	ns
	Carry Out Line	V_{DD} = 5V, C_L = 15 pF		240	480	ns
		V_{DD} = 10V, C_L = 15 pF		85	170	ns
		V_{DD} = 15V, C_L = 15 pF		70	140	ns
	Decode Out Lines	V_{DD} = 5V		500	1000	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		160	320	ns
t_{TLH}, t_{THL}	Transition Time Carry Out and Decode Out Lines					
	t_{TLH}	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
	t_{THL}	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V, Measured with Respect to Carry Output Line	1.0	2		MHz
		V_{DD} = 10V, Measured with Respect to Carry Output Line	2.5	5		MHz
		V_{DD} = 15V, Measured with Respect to Carry Output Line	3.0	6		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			20	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Clock Inhibit Data Set-Up Time	V_{DD} = 5V		120	240	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
C_{IN}	Average Input Capacitance			5	7.5	pF

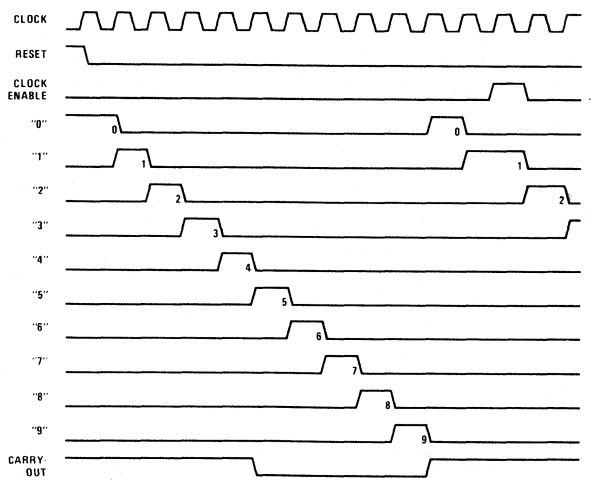
ac electrical characteristics (con't)

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, t_{rCL} and $t_{fCL} = 20$ ns, unless otherwise specified.

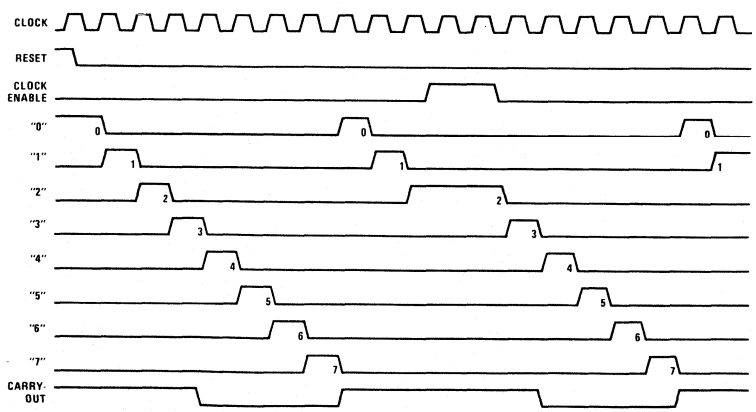
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
RESET OPERATION						
t_{PHL}	Propagation Delay Time:					
	Carry Out Line	$V_{DD} = 5V$		415	830	ns
		$V_{DD} = 10V$		160	320	ns
		$V_{DD} = 15V$		130	260	ns
	Carry Out Line	$V_{DD} = 5V$, $C_L = 15$ pF		240	480	ns
		$V_{DD} = 10V$, $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$, $C_L = 15$ pF		70	140	ns
	Decode Out Lines	$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		55	110	ns
t_{REM}	Minimum Reset Removal Time	$V_{DD} = 5V$		75	150	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns

timing diagrams

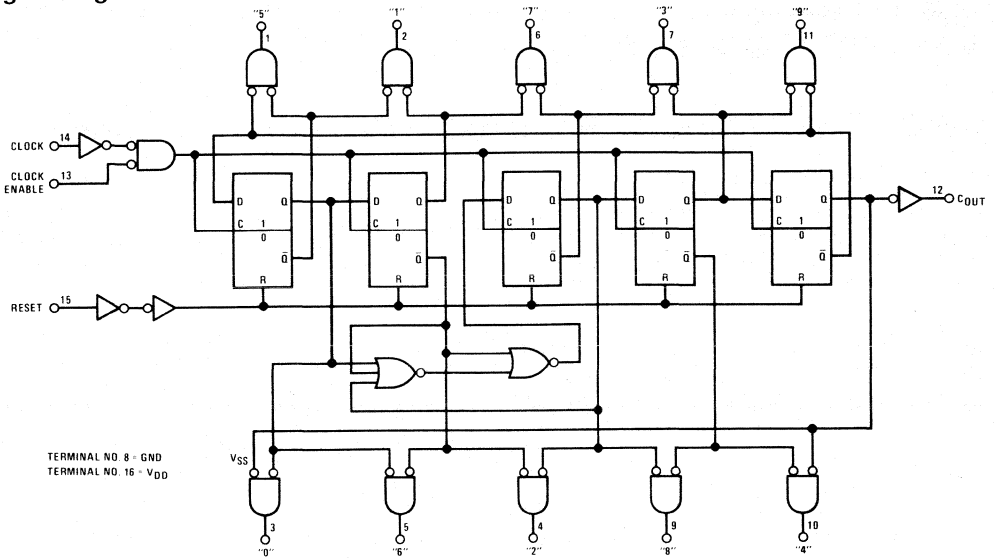
CD4017B



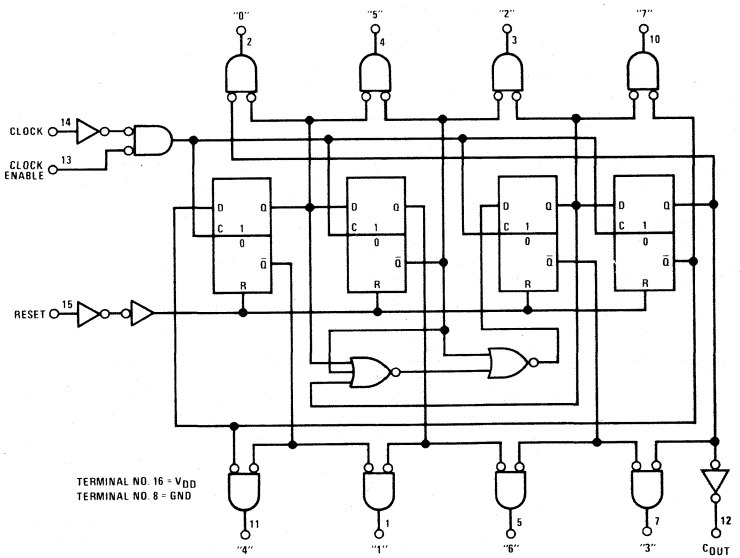
CD4022B



logic diagrams



CD4017B



CD4022B

National Semiconductor

CD4018BM/CD4018BC Presettable Divide-by-N Counter

general description

The CD4018B consists of 5 Johnson counter stages. A buffered $\overline{Q}$ output from each stage, "CLOCK", "RESET", "DATA", "PRESET ENABLE", and 5 individual "JAM" inputs are provided. The counter is advanced one count at the positive clock signal transition. A high "RESET" signal clears the counters to an "ALL ZERO" condition. A high "PRESET ENABLE" signal allows information on the "JAM" inputs to preset the counter. Anti-lock gating is provided to assure the proper counting sequence.

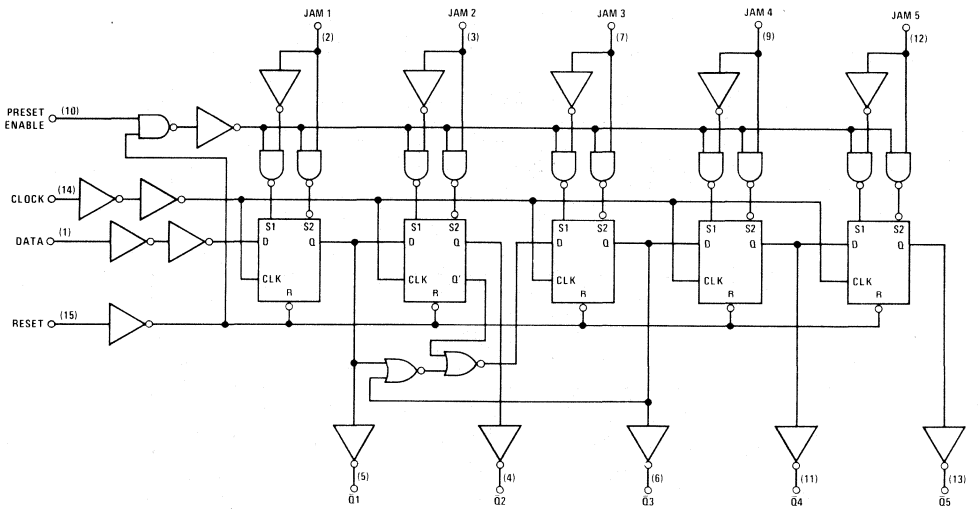
features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation

applications

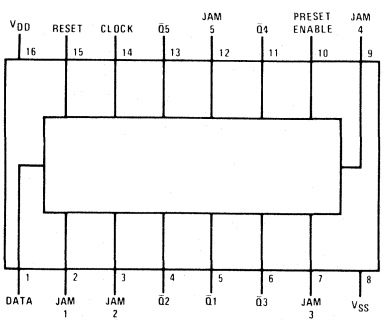
- Fixed and programmable divide-by-10, 9, 8, 7, 6, 5, 4, 3, 2, counter
- Fixed and programmable counters greater than 10
- Programmable decade counters
- Divide by "N" counters/frequency synthesizers

logic diagram



connection diagram

Dual-In-Line and Flat Package



absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4018BM	−55°C to +125°C
CD4018BC	−40°C to +85°C

dc electrical characteristics CD4018BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4018BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V

dc electrical characteristics (Continued) CD4018BC

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, Input t_r = t_f = 20 ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCK OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	700	ns
		V_{DD} = 10V		95	250	ns
		V_{DD} = 15V		70	200	ns
t_{THL}, t_{TLH}	Transition Time $\overline{Q}$ Outputs	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		65	130	ns
		V_{DD} = 15V		50	100	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	500	ns
		V_{DD} = 10V		50	200	ns
		V_{DD} = 15V		40	160	ns
t_{RCL}, t_{FCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
t_{SU}	Minimum Data Input Set-Up Time	V_{DD} = 5V		40	200	ns
		V_{DD} = 10V		20	100	ns
		V_{DD} = 15V		16	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1	4		MHz
		V_{DD} = 10V	3	9		MHz
		V_{DD} = 15V	5	14		MHz
PRESET OR RESET OPERATION						
$t_{PLH(R)}$	Propagation Delay Time to $\overline{Q}$	V_{DD} = 5V		235	750	ns
$t_{PHL(PR)}$		V_{DD} = 10V		95	250	ns
$t_{PLH(PR)}$		V_{DD} = 15V		70	200	ns
$t_{WH(R)}$	Minimum Preset or Reset	V_{DD} = 5V		100	400	ns
$t_{WH(PR)}$	Pulse Width	V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
t_{REM}	Minimum Preset or Reset Removal Time	V_{DD} = 5V		100	400	ns
		V_{DD} = 10V		40	160	ns
		V_{DD} = 15V		30	120	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		63		pF

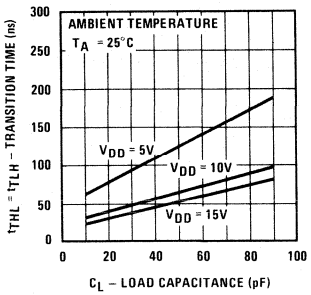
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

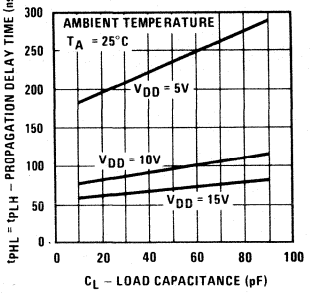
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C family characteristics application note AN-90.

typical performance characteristics

Typical Transition Time vs C_L



Typical Propagation Delay vs. C_L



external connections

External Connections for Divide by 10, 9, 8, 7, 6, 5, 4, 3, 2, Operation

Divide By 10	$\overline{Q}5$	Connected Back To "DATA" Input
Divide By 8	$\overline{Q}4$	
Divide By 6	$\overline{Q}3$	
Divide By 4	$\overline{Q}2$	
Divide By 2	$\overline{Q}1$	

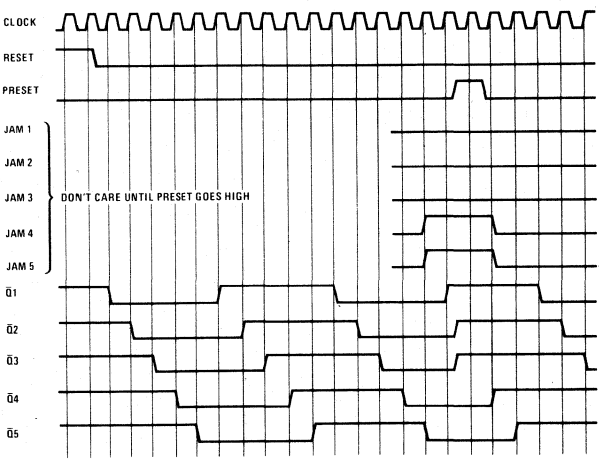
Divide By 9

Divide By 7

Divide By 5

Divide By 3

timing diagram



Note. "Data" input tied to $\overline{Q}5$ for decade counter configuration.

National Semiconductor

CD4019BM/CD4019BC Quad AND-OR Select Gate

general description

The CD4019BM/CD4019BC is a complementary MOS quad AND-OR select gate. Low power and high noise margin over a wide voltage range is possible through implementation of N and P-channel enhancement mode transistors. These complementary MOS (CMOS) transistors provide the building blocks for the 4 "AND-OR select" gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by control bits K_A and K_B. All inputs are protected against static discharge damage.

features

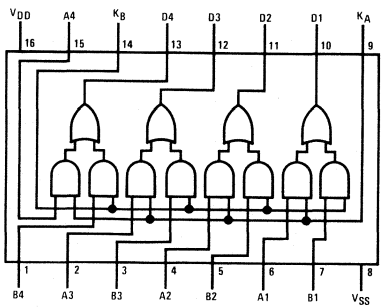
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

applications

- AND-OR select gating
- Shift-right/shift-left registers
- True/complement selection
- AND/OR/EXCLUSIVE-OR selection

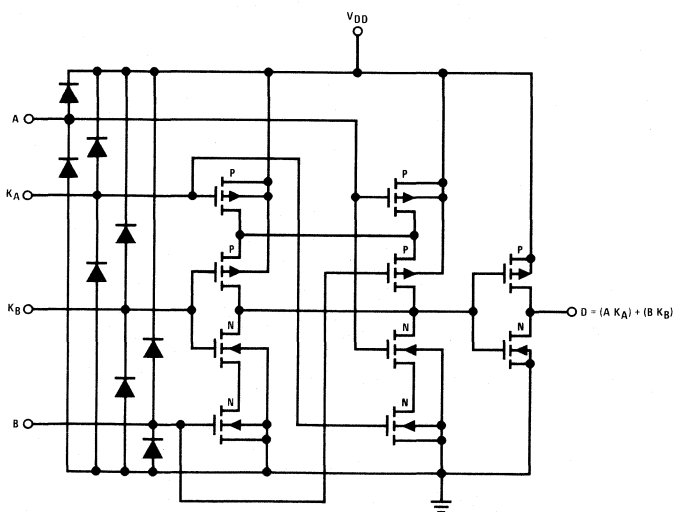
connection diagram

Dual-In-Line and Flat Package



TOP VIEW

schematic diagram



Schematic diagram for 1 of 4 identical stages

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD} V
T_A Operating Temperature Range	
CD4019BM	−55°C to +125°C
CD4019BC	−40°C to +85°C

dc electrical characteristics CD4019BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.03	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.05	0.5		15	μA
		V_{DD} = 15V		1.0		0.07	1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	10		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

dc electrical characteristics CD4019BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.03	1		7.5	μA
		V_{DD} = 10V		2		0.05	2		15	μA
		V_{DD} = 15V		4		0.07	4		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	1		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.5		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	10		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.4		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−1.0		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.0		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay	V_{DD} = 5V		100	300	ns
	Input to Output	V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		45	100	ns
t_{THL}	High-to-Low Level	V_{DD} = 5V		100	200	ns
	Transition Time	V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{TLH}	Low-to-High Level	V_{DD} = 5V		150	300	ns
	Transition Time	V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	All A and B Inputs		5	7.5	pF
		K_A and K_B Inputs, (Note 3)		10	15	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

National Semiconductor

CD4020BM/CD4020BC 14-Stage Ripple Carry Binary Counters
CD4040BM/CD4040BC 12-Stage Ripple Carry Binary Counters
CD4060BM/CD4060BC 14-Stage Ripple Carry Binary Counters

general description

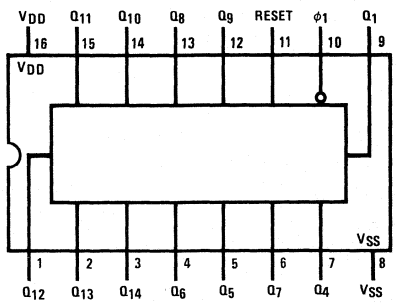
The CD4020BM/CD4020BC, CD4060BM/CD4060BC are 14-stage ripple carry binary counters, and the CD4040BM/CD4040BC is a 12-stage ripple carry binary counter. The counters are advanced one count on the negative transition of each clock pulse. The counters are reset to the zero state by a logical "1" at the reset input independent of clock.

features

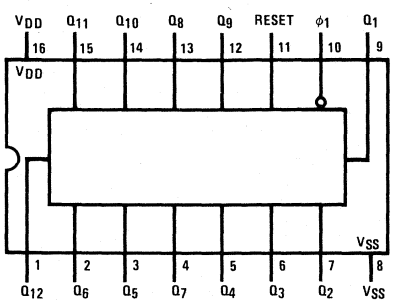
■ Wide supply voltage range	1.0V to 15V
■ High noise immunity	$0.45V_{DD}$ typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Medium speed operation	8MHz typ at V_{DD} = 10V
■ Schmitt trigger clock input	

connection diagrams

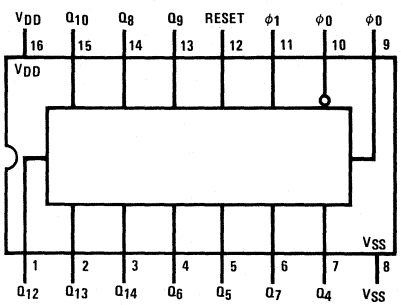
TOP VIEW



CD4020BM/CD4020BC



CD4040BM/CD4040BC



CD4060BM/CD4060BC

absolute maximum ratings (Notes 1 and 2)

V_{DD}	Supply Voltage	−0.5V to +18V
V_{IN}	Input Voltage	−0.5V to V_{DD} + 0.5V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

recommended operating conditions

V_{DD}	Supply Voltage	+3V to +15V
V_{IN}	Input Voltage	0V to V_{DD}
T_A	Operating Temperature Range	
	CD40XXBM	−55°C to +125°C
	CD40XXBC	−40°C to +85°C

dc electrical characteristics CD40XXBM (Note 2)

	PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Data does not apply to oscillator points ϕ_0 and ϕ_0 of CD4060BM/CD4060BC.

dc electrical characteristics CD40XXBC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current (See Note 3)	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.6	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics CD4020BM/CD4020BC, CD4040BM/CD4040BC

T_A = 25°C, C_L = 50pF, R_L = 200k, t_r = t_f = 20ns, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL1}, t_{PLH1}	Propagation Delay Time to Q_1	V_{DD} = 5V		250	550	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		75	150	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	V_{DD} = 5V		150	330	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		45	90	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V		125	335	ns
		V_{DD} = 10V		50	125	ns
		V_{DD} = 15V		40	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V		—	no limit	ns
		V_{DD} = 10V		—	no limit	ns
		V_{DD} = 15V		—	no limit	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	4		MHz
		V_{DD} = 10V	4	10		MHz
		V_{DD} = 15V	5	12		MHz
$t_{PHL(R)}$	Reset Propagation Delay	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	V_{DD} = 5V		200	450	ns
		V_{DD} = 10V		100	210	ns
		V_{DD} = 15V		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

Note 1: Capacitance guaranteed by periodic testing.

Note 2: C_{pd} determines the no-load etc.

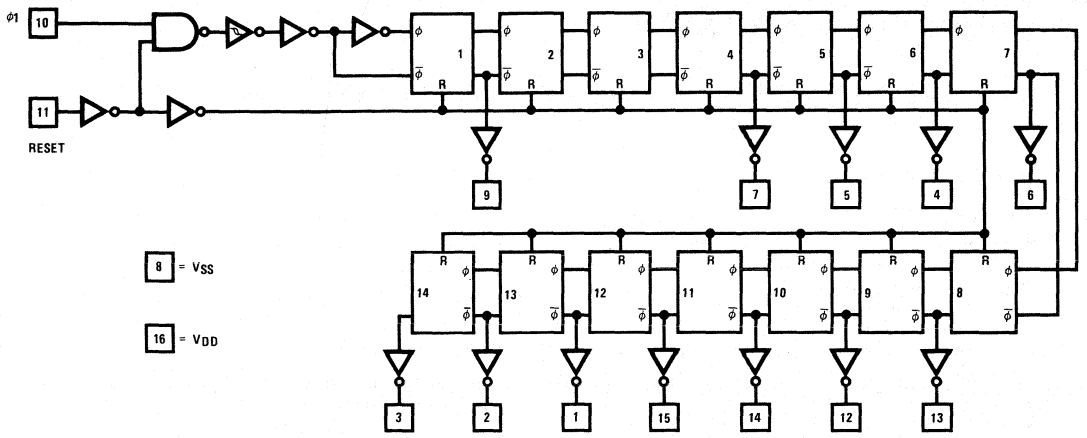
ac electrical characteristics CD4060BM/CD4060BC $T_A = 25°C, C_L = 50pF, R_L = 200k, t_r = t_f = 20ns$, unless otherwise noted.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL4}, t_{PLH4}	Propagation Delay Time to Q_4	$V_{DD} = 5V$		550	1300	ns
		$V_{DD} = 10V$		250	525	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	Interstage Propagation Delay Time from Q_n to Q_{n+1}	$V_{DD} = 5V$		150	330	ns
		$V_{DD} = 10V$		60	125	ns
		$V_{DD} = 15V$		45	90	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		170	500	ns
		$V_{DD} = 10V$		65	170	ns
		$V_{DD} = 15V$		50	125	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$		—	no limit	ns
		$V_{DD} = 10V$		—	no limit	ns
		$V_{DD} = 15V$		—	no limit	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1	3		MHz
		$V_{DD} = 10V$	3	8		MHz
		$V_{DD} = 15V$	4	10		MHz
$t_{PHL(R)}$	Reset Propagation Delay	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
$t_{WH(R)}$	Minimum Reset Pulse Width	$V_{DD} = 5V$		200	450	ns
		$V_{DD} = 10V$		100	210	ns
		$V_{DD} = 15V$		80	170	ns
C_{in}	Average Input Capacitance	Any Input (Note 1)		5	7.5	pF
C_{pd}	Power Dissipation Capacitance	(Note 2)		50		pF

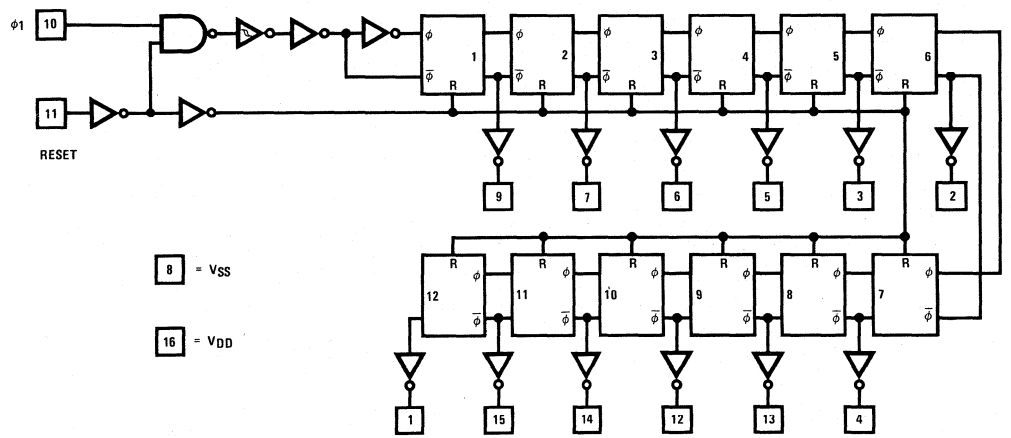
Note 1: Capacitance guaranteed by periodic testing.

Note 2: C_{pd} determines the no-load etc.

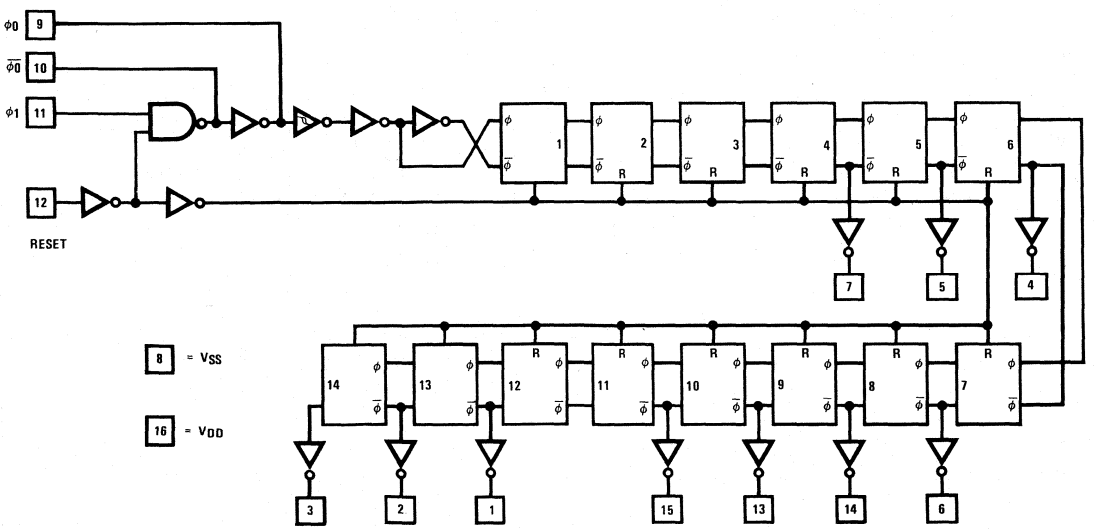
schematic diagram



CD4020BM/CD4020BC Schematic Diagram



CD4040BM/CD4040BC Schematic Diagram



CD4060BM/CD4060BC Schematic Diagram

National Semiconductor

CD4021M/CD4021C 8-Stage Static Shift Register

general description

The CD4021M/CD4021C is an 8-stage parallel input/serial output shift register. A parallel/serial control input enables individual "jam" inputs to each of 8-stages. Q outputs are available from the sixth, seventh and eighth stages.

When the parallel/serial control input is in the logical "0" state, data is serially shifted into the register synchronously with the positive transition of the clock. When the parallel/serial control is in the logical "1" state, data is "jammed" into each stage of the register asynchronously with the clock.

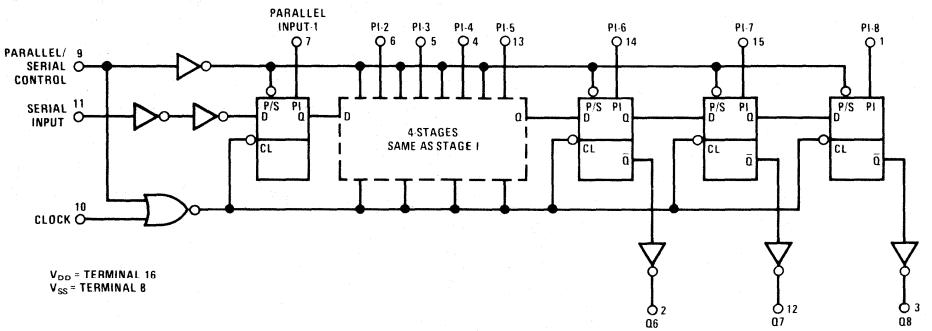
features

- Asynchronous parallel or synchronous serial operation.
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{CC} typ
- Medium speed operation clock rate at $V_{DD} - V_{SS} = 10V$ 5 MHz typ
- Fully static operation

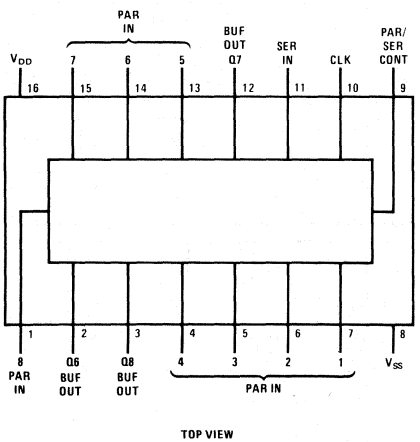
applications

- Parallel to serial data conversion
- General purpose register

logic diagram



connection diagram



TOP VIEW

truth table

CL▲	SERIAL INPUT	PARALLEL/ SERIAL CONTROL	PI 1	PI n	Q1 (INTERNAL)	Q_n	
X	X	1	Q	0	0	0	
X	X	1	0	1	0	1	
X	X	1	1	0	1	0	
X	X	1	1	1	1	1	
⌐	0	0	X	X	0	Q_{n-1}	
⌐	1	0	X	X	1	Q_{n-1}	
¬	X	0	X	X	Q1	Q_n	NO CHANGE

▲ = LEVEL CHANGE X = DON'T CARE CASE

absolute maximum ratings (Note 1)

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4021M	−55°C to +125°C
CD4021C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4021M

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			5		0.5	5			300	μA
	V_{DD} = 10V			10		1	10			600	μA
Quiescent Device Dissipation	V_{DD} = 5V			25		2.5	25			1,500	μW
Package (P_D)	V_{DD} = 10V			100		10	100			6,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.15			0.12	0.3		0.085			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.31			0.25	0.5		0.175			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.1			−0.08	−0.16		−0.055			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.25			−0.20	−0.44		−0.14			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4021C

PARAMETERS	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5V			50		0.5	50			700	μA
	V_{DD} = 10V			100		1	100			1,400	μA
Quiescent Device Dissipation	V_{DD} = 5V			250		2.5	250			3,500	μW
Package (P_D)	V_{DD} = 10V			1,000		10	1,000			14,000	μW
Output Voltage	V_{DD} = 5V			0.01		0	0.01			0.05	V
Low-Level (V_{OL})	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage	V_{DD} = 5V	4.99			4.99	5		4.95			V
High-Level (V_{OH})	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity	V_O = 0.8V, V_{DD} = 5V	1.5			1.5	2.25		1.4			V
(All Inputs) (V_{NL})	V_O = 1V, V_{DD} = 10V	3			3	4.5		2.9			V
Noise Immunity	V_O = 4.2V, V_{DD} = 5V	1.4			1.5	2.25		1.5			V
(All Inputs) (V_{NH})	V_O = 9V, V_{DD} = 10V	2.9			3	4.5		3			V
Output Drive Current	V_O = 0.5V, V_{DD} = 5V	0.072			0.06	0.3		0.05			mA
N-Channel (I_DN)	V_O = 0.5V, V_{DD} = 10V	0.12			0.1	0.5		0.08			mA
Output Drive Current	V_O = 4.5V, V_{DD} = 5V	−0.06			−0.05	−0.16		−0.04			mA
P-Channel (I_DP)	V_O = 9.5V, V_{DD} = 10V	−0.12			−0.1	−0.44		−0.08			mA
Input Current (I_I)						10					pA

ac electrical characteristics CD4021M

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	750	ns
	V_{DD} = 10V		100	225	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	300	ns
	V_{DD} = 10V		75	125	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	500	ns
	V_{DD} = 10V		100	175	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	350	ns
	V_{DD} = 10V		50	80	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	1	2.5		MHz
	V_{DD} = 10V	3	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

ac electrical characteristics CD4021C

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Propagation Delay Time (t_{PHL}, t_{PLH})	V_{DD} = 5V		300	1,000	ns
	V_{DD} = 10V		100	300	ns
Transition Time (t_{THL}, t_{TLH})	V_{DD} = 5V		150	400	ns
	V_{DD} = 10V		75	150	ns
Minimum Clock Pulse Width (t_{WL}, t_{WH})	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Minimum High Level Parallel/Serial Control Pulse Width ($t_{WH(P/S)}$)	V_{DD} = 5V		200	830	ns
	V_{DD} = 10V		100	200	ns
Clock Rise Time (t_{rCL}) or Clock Fall Time (t_{fCL})	V_{DD} = 5V			15	μs
	V_{DD} = 10V			15	μs
Set-up Time	V_{DD} = 5V		100	500	ns
	V_{DD} = 10V		50	100	ns
Maximum Clock Frequency (f_{CL})	V_{DD} = 5V	0.6	2.5		MHz
	V_{DD} = 10V	2.5	5		MHz
Input Capacitance (C_I) (Note 2)	Any Input		5		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Capacitance is guaranteed by periodic testing.

National Semiconductor

CD4023BM/CD4023BC Triple 3-Input NAND Gate
CD4025BM/CD4025BC Triple 3-Input NOR Gate

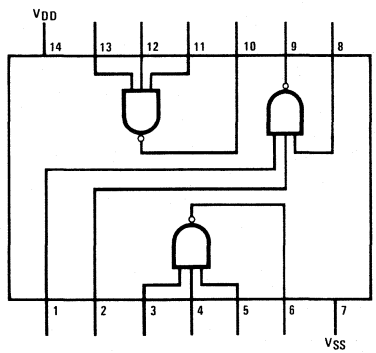
general description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

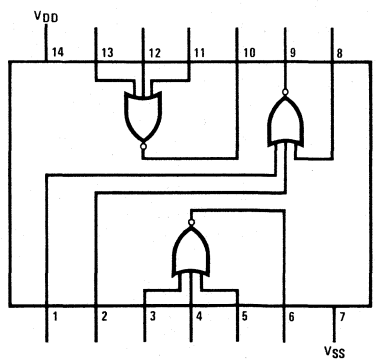
features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5 V - 10 V - 15 V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1 μA at 15 V over full temperature range

connection diagrams



CD4023BM/CD4023BM
TOP VIEW



CD4025BM/CD4025BC
TOP VIEW

absolute maximum ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	$300°C$

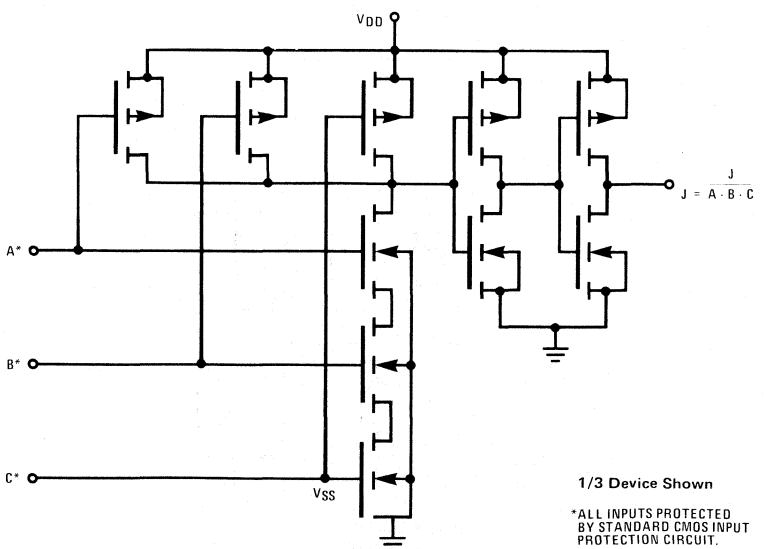
recommended operating conditions (Note 2)

V_{DD}	DC Supply Voltage	$+5\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4023BM, CD4025BM	$-55°C$ to $+125°C$
	CD4023BC, CD4025BC	$-40°C$ to $+85°C$

dc electrical characteristics — CD4023BM, CD4025BM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	$V_{DD} = 5\ V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10\ V$		0.5		0.005	0.5		15	μA
		$V_{DD} = 15\ V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\ V$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\ V$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\ V$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\ V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\ V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\ V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 4.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\ V$, $V_O = 9.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\ V$, $V_O = 1.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.10		10^{-5}	0.10		1.0	μA

schematic diagram



CD4023BC/CD4023BM

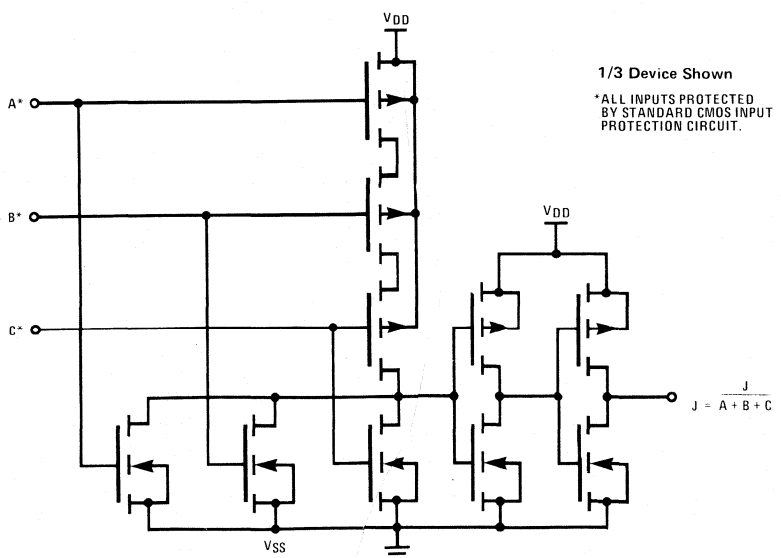
dc electrical characteristics — CD4023BC, CD4025BC (Note 2)

PARAMETER		CONDITIONS	-40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V				0.004			7.5	μA
		V_{DD} = 10 V				0.005			15	μA
		V_{DD} = 15 V				0.006			30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 4.5 V		1.5		2	1.5		1.5	V
		V_{DD} = 10 V, V_O = 9.0 V, $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		V_{DD} = 15 V, V_O = 13.5 V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V	3.5		3.5	3		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	-0.52		-0.44	-0.88		-0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	-1.3		-1.1	-2.2		-0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	-3.6		-3.0	-8		-2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		-0.3		-10^{-5}	-0.3		-1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

schematic diagram



CD4025BM/CD4025BC

ac electrical characteristics $T_A = 25°C$, $C_L = 50pF$, $R_L = 200k$, unless otherwise specified.

PARAMETER		CONDITIONS	CD4023BC CD4023BM			CD4025BC CD4025BM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5V$		130	250		130	250	ns
		$V_{DD} = 10V$		60	100		60	100	ns
		$V_{DD} = 15V$		40	70		40	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5V$		110	250		120	250	ns
		$V_{DD} = 10V$		50	100		60	100	ns
		$V_{DD} = 15V$		35	70		40	70	ns
t_{THL}	Transition Time	$V_{DD} = 5V$		90	200		90	200	ns
t_{TLH}		$V_{DD} = 10V$		50	100		50	100	ns
		$V_{DD} = 15V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance (See Note 3)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4024BM/CD4024BC 7-Stage Ripple Carry Binary Counter

general description

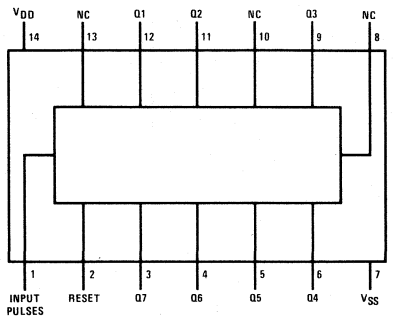
The CD4024BM/CD4024BC is a 7-stage ripple-carry binary counter. Buffered outputs are externally available from stages 1 through 7. The counter is reset to its logical "0" state by a logical "1" on the reset input. The counter is advanced one count on the negative transition of each clock pulse.

features

■ Wide supply voltage range	3.0V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ High speed	12 MHz (typ) input pulse rate $V_{DD} - V_{SS} = 10V$
■ Fully static operation	

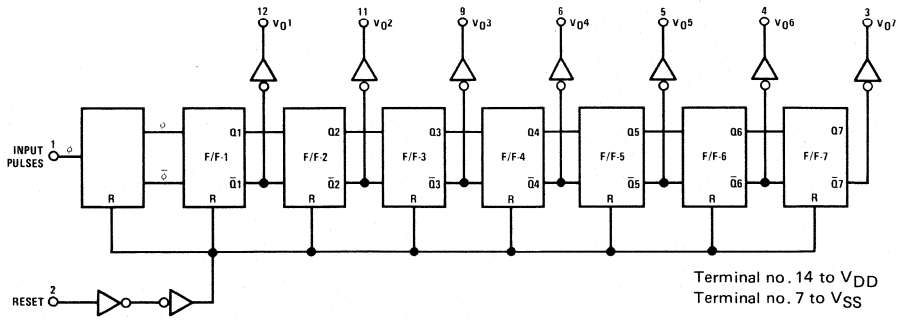
connection diagram

Dual-In-Line Package

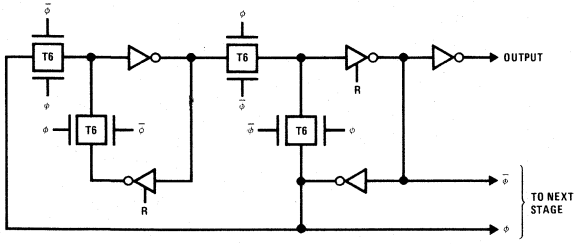


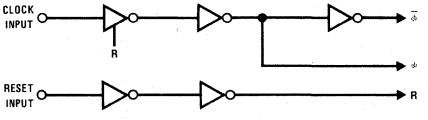
TOP VIEW

logic diagram



schematic diagram





Input Logic

Flip-flop logic (1 of 7 identical stages).

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	+3 to +15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4024BM	−55°C to +125°C
CD4024BC	−40°C to +85°C

dc electrical characteristics CD4024BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		0.7	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA-
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

dc electrical characteristics CD4024BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.3	20		150	μA
		V_{DD} = 10V		40		0.5	40		300	μA
		V_{DD} = 15V		60		0.7	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (con't) CD4024BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time (Note 3)	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Width	V_{DD} = 5V		75	200	ns
		V_{DD} = 10V		40	110	ns
		V_{DD} = 15V		35	90	ns
t_{RCL}, t_{FCL}	Input Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			8	μs
f_{CL}	Maximum Input Pulse Frequency	V_{DD} = 5V	1.5	5		MHz
		V_{DD} = 10V	4	12		MHz
		V_{DD} = 15V	5	15		MHz
t_{PHL}	Reset Propagation Delay Time	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
t_{WH}	Reset Minimum Pulse Width	V_{DD} = 5V		185	350	ns
		V_{DD} = 10V		85	125	ns
		V_{DD} = 15V		70	100	ns
C_{IN}	Input Capacitance (Note 4)	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: To Q1 output.

Note 4: Capacitance is guaranteed by periodic testing.

National Semiconductor

CD4025M/CD4025C Triple 3-Input NOR Gate

general description

These NOR gates are monolithic complementary MOS (CMOS) integrated circuits. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swings essentially equal to the supply voltage. This results in high noise immunity over a wide supply voltage range. No dc power other than that caused by leakage current is consumed during static conditions. All inputs are protected against static discharge and latching conditions.

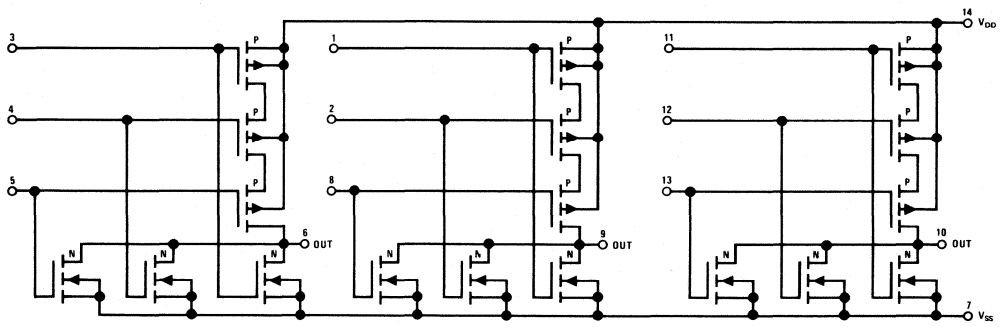
features

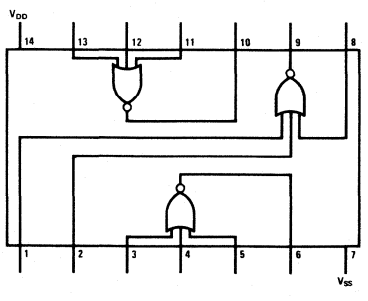
- Wide supply voltage range 3.0V to 15V
- Low power 10 nW (typ.)
- High noise immunity 0.45 V_{DD} (typ.)
- Medium speed operation $t_{PHL} = t_{PLH}$ = 25 ns (typ.) at C_L = 15 pF

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

logic and connection diagrams





TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4025M	−55°C to +125°C
CD4025C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4025M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.05		0.001	0.05			3.0	μA
	V_{DD} = 10V			0.1		0.001	0.1			6.0	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			0.25		0.005	0.25			15	μW
	V_{DD} = 10V			1.0		0.01	1.0			60	μW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	I_O = 0, V_O = 4.3V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	I_O = 0, V_O = 9.3V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	I_O = 0, V_O = 0.7V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	I_O = 0, V_O = 0.7V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, V_O = 0.4, V_{DD} = 5.0V	0.5			0.40			0.28			mA
	$V_I = V_{DD}$, V_O = 0.5, V_{DD} = 10V	1.1			0.9			0.65			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq$ 2.5V, V_{DD} = 5.0V	−0.62			−0.5			−0.35			mA
	$V_I = V_{SS}$, V_O = 9.5V, V_{DD} = 10V	−0.62			−0.5			−0.35			mA
Input Current (I_I)						10					pA

dc electrical characteristics CD4025C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			15	μA
	V_{DD} = 10V			1.0		0.005	1.0			30	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			0.25		0.025	2.5			75	μA
	V_{DD} = 10V			10		0.05	10			300	μW
Output Voltage Low Level (V_{OL})	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	$V_I = V_{SS}$, I_O = 0A, V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	$V_I = V_{DD}$, I_O = 0A,V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	$V_I = V_{DD}$, I_O = 0A, V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (V_{NL})(All Inputs)	I_O = 0, V_O = 4.3V, V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	I_O = 0, V_O = 9.3V, V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (V_{NH})(All Inputs)	I_O = 0, V_O = 0.7V, V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	I_O = 0, V_O = 0.7V, V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	$V_I = V_{DD}$, V_O = 0.4V, V_{DD} = 5.0V	0.35			0.3	1.0		0.24			mA
	$V_I = V_{DD}$, V_O = 0.5V, V_{DD} = 10V	0.72			0.6	2.5		0.48			mA
Output Drive Current P-Channel (I_DP)	$V_I = V_{SS}$, $V_O \neq$ 2.5V, V_{DD} = 5.0V	−0.35			−0.3	−2.0		−0.24			mA
	$V_I = V_{SS}$, V_O = 9.5V, V_{DD} = 10V	−0.3			−0.25	−1.0		−0.2			mA
Input Current (I_I)						10					pA

Note 1: This device should not be connected to circuits with the power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4025M

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	50	ns
	$V_{DD} = 10V$		25	40	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	70	ns
	$V_{DD} = 10V$		25	45	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	125	ns
	$V_{DD} = 10V$		35	70	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	175	ns
	$V_{DD} = 10V$		35	75	ns
Input Capacitance (C_I)	Any Input		5.0		pF

ac electrical characteristics CD4025C

$T_A = 25°C$ and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time High to Low Level (t_{PHL})	$V_{DD} = 5.0V$		35	80	ns
	$V_{DD} = 10V$		25	55	ns
Propagation Delay Time Low to High Level (t_{PLH})	$V_{DD} = 5.0V$		35	120	ns
	$V_{DD} = 10V$		25	65	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		65	200	ns
	$V_{DD} = 10V$		35	115	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		65	300	ns
	$V_{DD} = 10V$		35	125	ns
Input Capacitance (C_I)	Any Input		5.0		pF

National Semiconductor

CD4027BM/CD4027BC Dual J-K Master/Slave Flip-Flop with Set and Reset

general description

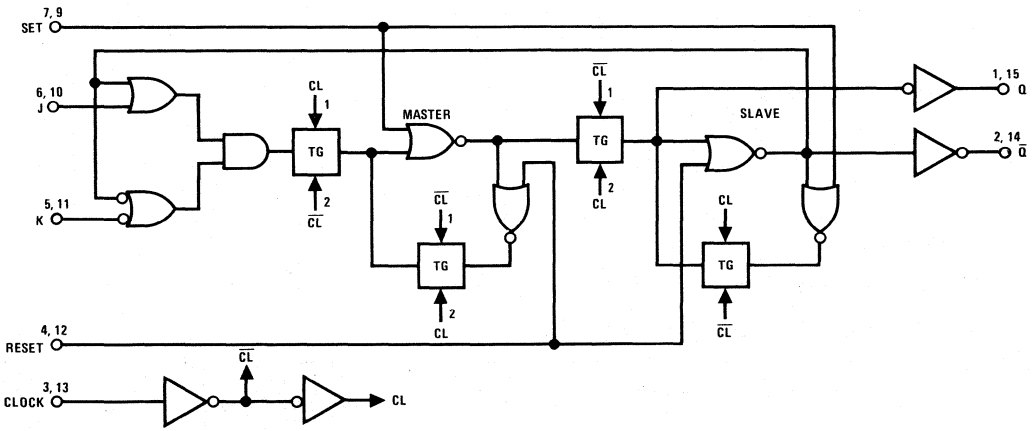
These dual JK flip-flops are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. Each flip-flop has independent J, K, set, reset and clock inputs and buffered Q and $\overline{Q}$ outputs. These flip-flops are edge sensitive to the clock input and change state on the positive-going transition of the clock pulses. Set or reset is independent of the clock and is accomplished by a high level on the respective input.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

features

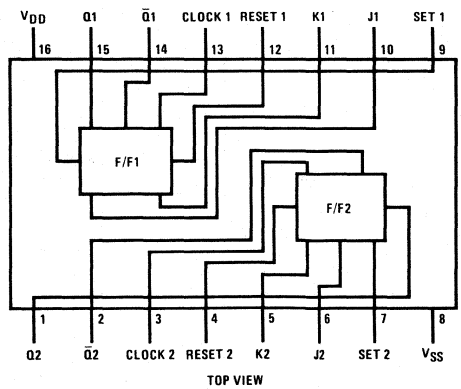
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Low power	50 nW typ
■ Medium speed operation	12 MHz typ with 10V supply

schematic diagram



connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4027BM	−55°C to +125°C
CD4027BC	−40°C to +85°C

dc electrical characteristics CD4027BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1			1		30	μA
		V_{DD} = 10V		2			2		60	μA
		V_{DD} = 15V		4			4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4027BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

dc electrical characteristics (con't) CD4027BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, t_{rCL} = t_{fCL} = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q or $\overline{Q}$	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to $\overline{Q}$ or Reset to Q	V_{DD} = 5V		170	340	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Set to Q or Reset to $\overline{Q}$	V_{DD} = 5V		110	220	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_s	Minimum Data Set-Up Time	V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		55	110	ns
		V_{DD} = 15V		45	90	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency (Toggle Mode)	V_{DD} = 5V	2.5	5		MHz
		V_{DD} = 10V	6.2	12.5		MHz
		V_{DD} = 15V	7.6	15.5		MHz
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_W	Minimum Clock Pulse Width (t_{WH} = t_{WL})	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		32	65	ns
t_{WH}	Minimum Set and Reset Pulse Width	V_{DD} = 5V		80	160	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Per Flip-Flop (Note 3)		35		pF

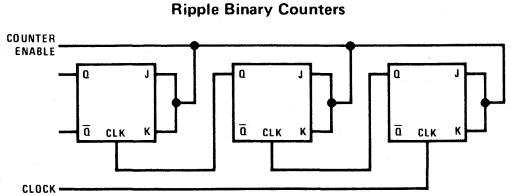
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

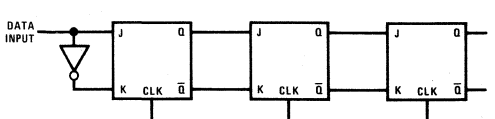
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

typical applications

Ripple Binary Counters



Shift Registers



truth table

$^{\bullet}t_{n-1}$ INPUTS						$^{\blacklozenge}t_n$ OUTPUTS		
CL▲	J	K	S	R	Q	Q	$\overline{Q}$	
⌐¯	1	X	0	0	0	1	0	
⌐¯	X	0	0	0	1	1	0	
⌐¯	0	X	0	0	0	0	1	
⌐¯	X	1	0	0	1	0	1	
¯⌐	X	X	0	0	X			(No change)
X	X	X	1	0	X	1	0	
X	X	X	0	1	X	0	1	
X	X	X	1	1	X	1	1	

Where:
- 1 = High Level
- 0 = Low Level
- ▲ = Level Change
- X = Don't Care
- ● = t_{n-1} refers to the time interval prior to the positive clock pulse transition
- ◆ = t_n refers to the time intervals after the positive clock pulse transition

National Semiconductor

CD4028BM/CD4028BC BCD-to-Decimal Decoder

general description

The CD4028BM/CD4028BC is a BCD-to-decimal or binary-to-octal decoder consisting of 4 inputs, decoding logic gates, and 10 output buffers. A BCD code applied to the 4 inputs, A, B, C and D, results in a high level at the selected 1-of-10 decimal decoded outputs. Similarly, a 3-bit binary code applied to inputs A, B and C is decoded in octal at outputs 0–7. A high level signal at the D input inhibits octal decoding and causes outputs 0–7 to go low.

All inputs are protected against static discharge damage by diode clamps to V_{DD} and V_{SS}.

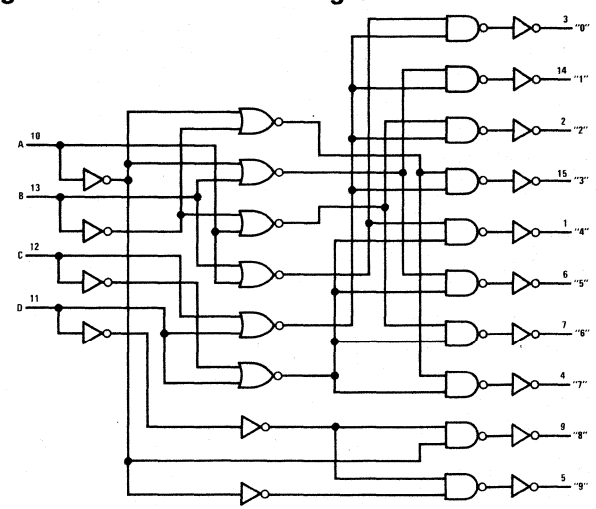
features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low power
- Glitch free outputs
- "Positive logic" on inputs and outputs

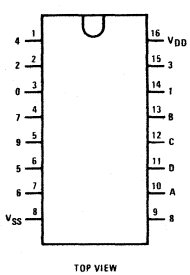
applications

- Code conversion
- Address decoding
- Indicator–tube decoder

logic and connection diagrams



Dual-In-Line and Flat Package



TOP VIEW

truth table

D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	0	0	0	1	0	0	0	0	0	0	0	0	0	BCD States
0	0	0	1	0	1	0	0	0	0	0	0	0	0	
0	0	1	0	0	0	1	0	0	0	0	0	0	0	
0	0	1	1	0	0	0	1	0	0	0	0	0	0	
0	1	0	0	0	0	0	0	1	0	0	0	0	0	
0	1	0	1	0	0	0	0	0	1	0	0	0	0	
0	1	1	0	0	0	0	0	0	0	1	0	0	0	
0	1	1	1	0	0	0	0	0	0	0	1	0	0	
1	0	0	0	0	0	0	0	0	0	0	0	1	0	
1	0	0	1	0	0	0	0	0	0	0	0	0	1	
1	0	1	0	0	0	0	0	0	0	0	0	1	0	Extraordinary States
1	0	1	1	0	0	0	0	0	0	0	0	0	1	
1	1	0	0	0	0	0	0	0	0	0	0	1	0	
1	1	0	1	0	0	0	0	0	0	0	0	0	1	
1	1	1	0	0	0	0	0	0	0	0	0	1	0	
1	1	1	1	0	0	0	0	0	0	0	0	0	1	

1 = High level
0 = Low level

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4028BM	−55°C to +125°C
CD4028BC	−40°C to +85°C

dc electrical characteristics CD4028BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	1.0		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.6		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	6.8		2.4		mA
I_{OH}	High Level Output Current	V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.4		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−1.0		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.0		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4028BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

dc electrical characteristics (Continued) CD4028BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.2		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	6.0		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.32		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.8		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−2.4		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3			−0.3			−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V	0.3			0.3			1.0	μA

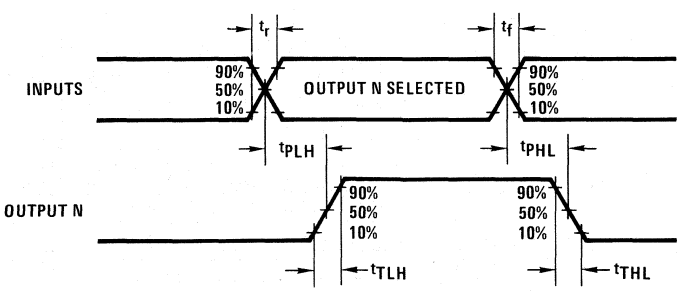
ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay	V_{CC} = 5V		240	480	ns
		V_{CC} = 10V		100	200	ns
		V_{CC} = 15V		70	140	ns
t_{THL} or t_{TLH}	Transition Time	V_{CC} = 5V		175	350	ns
		V_{CC} = 10V		75	150	ns
		V_{CC} = 15V		60	110	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

switching time waveforms



National Semiconductor

CD4029BM/CD4029BC Presettable Binary/Decade Up/Down Counter

general description

The CD4029BM/CD4029BC is a presettable up/down counter which counts in either binary or decade mode depending on the voltage level applied at binary/decade input. When binary/decade is at logical "1," the counter counts in binary, otherwise it counts in decade. Similarly, the counter counts up when the up/down input is at logical "1" and vice versa.

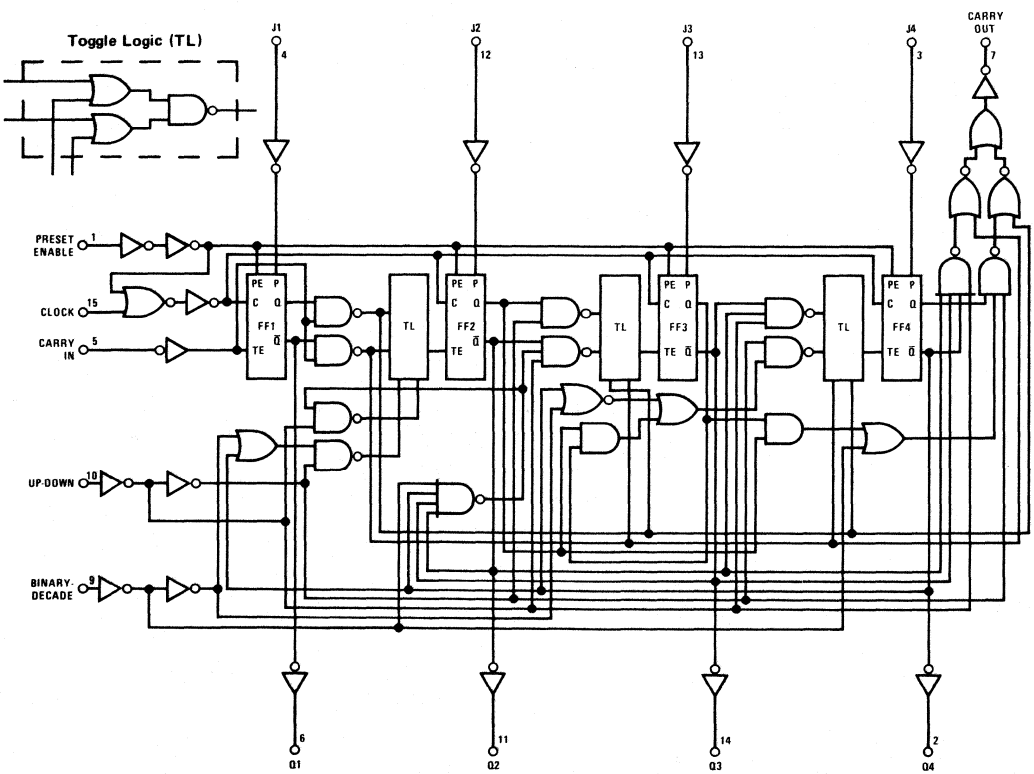
A logical "1" preset enable signal allows information at the "jam" inputs to preset the counter to any state asynchronously with the clock. The counter is advanced one count at the positive-going edge of the clock if the carry in and preset enable inputs are at logical "0." Advancement is inhibited when either or both of these two inputs is at logical "1." The carry out signal is normally at logical "1" state and goes to logical "0" state when the counter reaches its maximum count in the "up" mode or the minimum count in the "down" mode provided the carry input is at logical "0" state.

All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel jam inputs
- Binary or BCD decade up/down counting

logic diagram



absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4029BM	−55°C to +125°C
CD4029BC	−40°C to +85°C

dc electrical characteristics CD4029BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5	5	150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4029BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (con't) CD4029BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5 or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_{rCL} = t_{fCL} = 20 ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Outputs	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		70	140	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V		320	640	ns
		V_{DD} = 10V		135	270	ns
		V_{DD} = 15V		110	220	ns
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	V_{DD} = 5V, C_L = 15 pF		285	570	ns
		V_{DD} = 10V, C_L = 15 pF		120	240	ns
		V_{DD} = 15V, C_L = 15 pF		95	190	ns
t_{THL} or t_{TLH}	Transition Time/Q or Carry Output	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH} or t_{WL}	Minimum Clock Pulse Width	V_{DD} = 5V		160	320	ns
		V_{DD} = 10V		70	135	ns
		V_{DD} = 15V		55	110	ns
t_{rCL} or t_{fCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	10			μs
		V_{DD} = 15V	5			μs
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		180	360	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		55	110	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	3.1		MHz
		V_{DD} = 10V	3.7	7.4		MHz
		V_{DD} = 15V	4.5	9		MHz
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		65		pF
PRESET ENABLE OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Q Output	V_{DD} = 5V		285	570	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		95	195	ns

ac electrical characteristics (con't)

$T_A = 25°C$, $C_L = 50$ pF, $t_{rCL} = t_{fCL} = 20$ ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PRESET ENABLE OPERATION (con't)						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		400	800	ns
		$V_{DD} = 10V$		165	330	ns
		$V_{DD} = 15V$		135	270	ns
t_{WH}	Minimum Preset Enable Pulse Width	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		30	60	ns
		$V_{DD} = 15V$		25	50	ns
t_{REM}	Minimum Preset Enable Removal Time	$V_{DD} = 5V$		150	300	ns
		$V_{DD} = 10V$		60	120	ns
		$V_{DD} = 15V$		50	100	ns
CARRY INPUT OPERATION						
t_{PHL} or t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$		265	530	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time to Carry Output	$V_{DD} = 5V$, $C_L = 15$ pF		200	400	ns
		$V_{DD} = 10V$, $C_L = 15$ pF		85	170	ns
		$V_{DD} = 15V$, $C_L = 15$ pF		70	140	ns

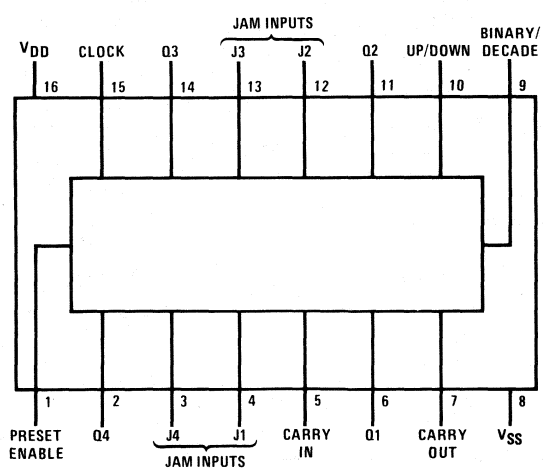
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

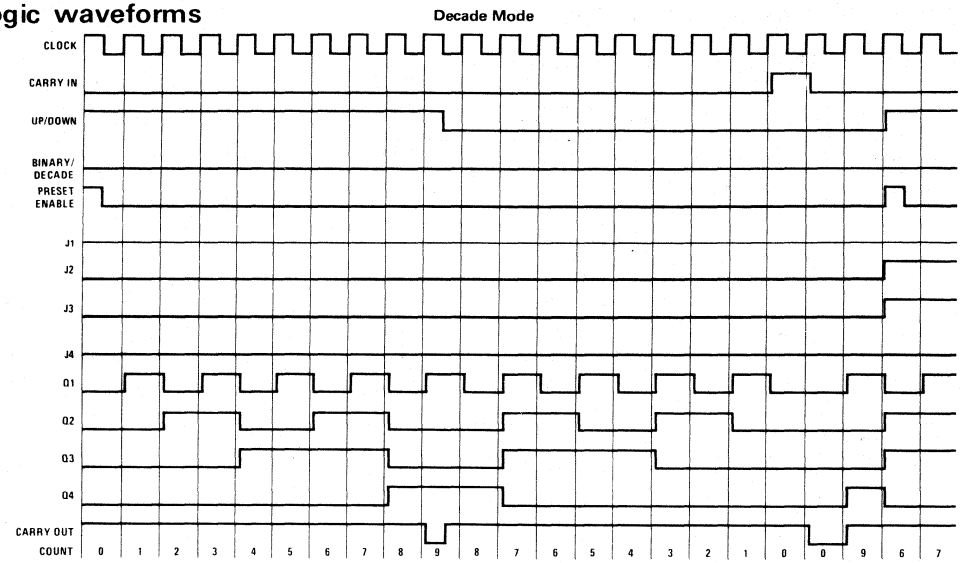
connection diagram

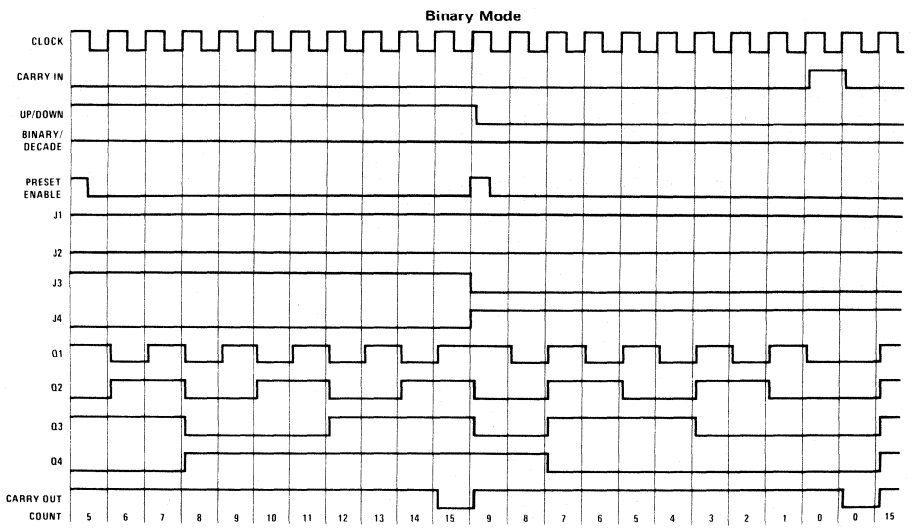
Dual-In-Line Package



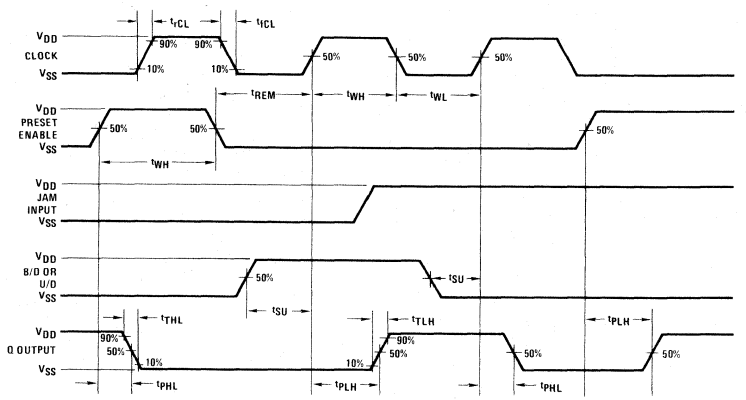
TOP VIEW

logic waveforms



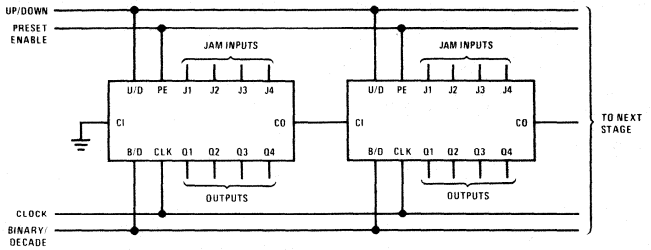


switching time waveforms

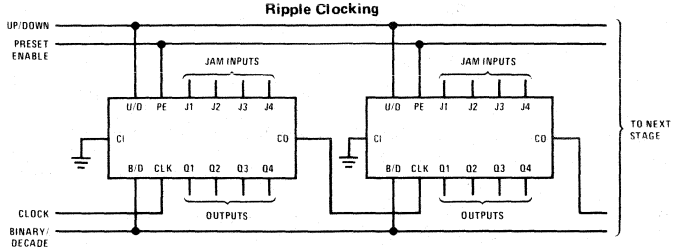


cascading packages

Parallel Clocking



Ripple Clocking



National Semiconductor

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

general description

These EXCLUSIVE-OR gates are monolithic Complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

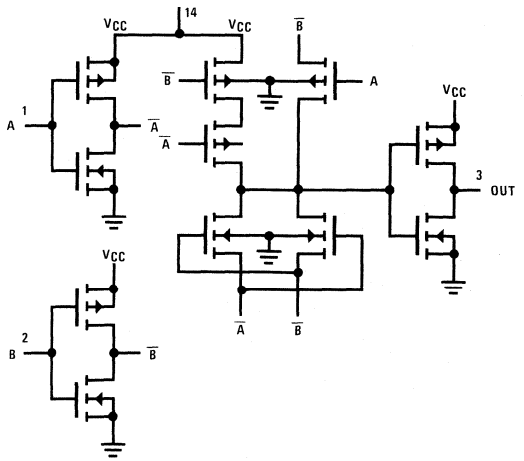
features

- Wide supply voltage range 3.0V to 15V
- Low power 100 nW (typ)
- Medium speed operation $t_{PHL} = t_{PLH} = 40$ ns (typ) at $C_L = 15$ pF, 10V supply
- High noise immunity 0.45 V_{CC} (typ)

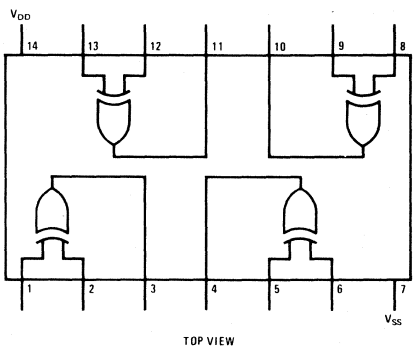
applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

schematic diagram



connection diagram



TOP VIEW

absolute maximum ratings

Voltage at Any Pin (Note 1)	V_{SS} − 0.3V to V_{SS} + 15.5V
Operating Temperature Range	
CD4030M	−55°C to +125°C
CD4030C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4030M

PARAMETER	CONDITIONS	LIMITS									UNITS
		−55°C			25°C			125°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			0.5		0.005	0.5			30	μA
	V_{DD} = 10V			1.0		0.01	1.0			60	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			2.5		0.025	2.5			150	μW
	V_{DD} = 10V			10		0.1	10			600	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs) (V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0V	0.75			0.6	1.2		0.45			mA
	V_{DD} = 10V	1.5			1.2	2.4		0.9			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.45			−0.3	−0.6		−0.21			mA
	V_{DD} = 10V	−0.95			−0.65	−1.3		−0.45			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

dc electrical characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS									UNITS
		−40°C			25°C			85°C			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Quiescent Device Current (I_L)	V_{DD} = 5.0V			5.0		0.05	5.0			70	μA
	V_{DD} = 10V			10		0.1	10			140	μA
Quiescent Device Dissipation Package (P_D)	V_{DD} = 5.0V			25		0.25	25			350	μW
	V_{DD} = 10V			100		1.0	100			1,400	μW
Output Voltage Low Level (V_{OL})	V_{DD} = 5.0V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
Output Voltage High Level (V_{OH})	V_{DD} = 5.0V	4.99			4.99	5.0		4.95			V
	V_{DD} = 10V	9.99			9.99	10		9.95			V
Noise Immunity (All Inputs)(V_{NL})	V_{DD} = 5.0V	1.5			1.5	2.25		1.4			V
	V_{DD} = 10V	3.0			3.0	4.5		2.9			V
Noise Immunity (All Inputs)(V_{NH})	V_{DD} = 5.0V	1.4			1.5	2.25		1.5			V
	V_{DD} = 10V	2.9			3.0	4.5		3.0			V
Output Drive Current N-Channel (I_DN)	V_{DD} = 5.0	0.35			0.3	1.2		0.25			mA
	V_{DD} = 10V	0.7			0.6	2.4		0.5			mA
Output Drive Current P-Channel (I_DP)	V_{DD} = 5.0V	−0.21			−0.15	−0.6		−0.12			mA
	V_{DD} = 10V	−0.45			−0.32	−1.3		−0.25			mA
Input Current (I_I)	V_I = 0V or V_I = V_{DD}					10					pA

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

ac electrical characteristics CD4030M

at $T_A = 25°C$, $V_{SS} = 0V$, and $C_L = 15$ pF. Typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	200	ns
	$V_{DD} = 10V$		40	100	ns.
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	150	ns
	$V_{DD} = 10V$		25	75	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	150	ns
	$V_{DD} = 10V$		30	75	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

ac electrical characteristics CD4030C

PARAMETER	CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Propagation Delay Time (t_{PHL})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Propagation Delay Time (t_{PLH})	$V_{DD} = 5.0V$		100	300	ns
	$V_{DD} = 10V$		40	150	ns
Transition Time High to Low Level (t_{THL})	$V_{DD} = 5.0V$		70	300	ns
	$V_{DD} = 10V$		25	150	ns
Transition Time Low to High Level (t_{TLH})	$V_{DD} = 5.0V$		80	300	ns
	$V_{DD} = 10V$		30	150	ns
Input Capacitance (C_I)	$V_I = 0V$ or $V_I = V_{DD}$		5.0		pF

truth table (For One of Four Identical Gates)

A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

National Semiconductor

CD4031BM/CD4031BC 64-Stage Static Shift Register

general description

The CD4031BM/CD4031BC is an integrated, complementary MOS (CMOS), 64-stage, fully static shift register. Two data inputs, DATA IN and RECIRCULATE IN, and a MODE CONTROL input are provided. Data at the DATA input (when MODE CONTROL is LOW) or data at the RECIRCULATE input (when MODE CONTROL is HIGH), which meets the setup and hold time requirements, is entered into the first stage of the register and is shifted one stage at each positive transition of the CLOCK.

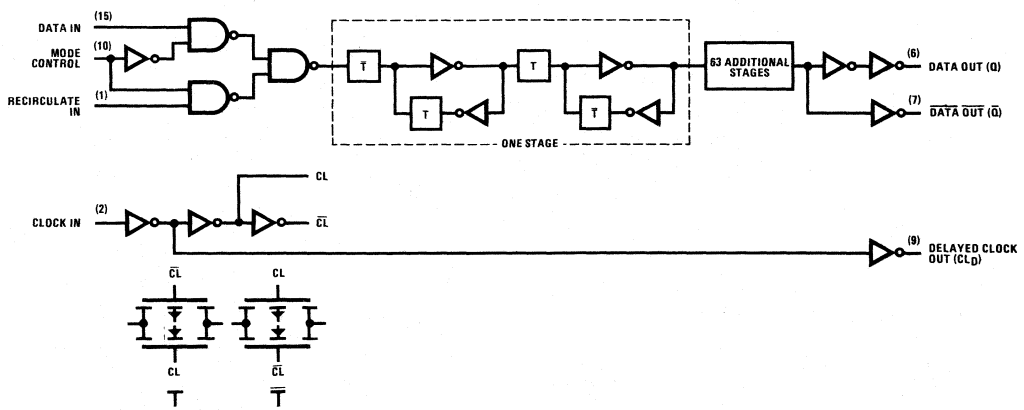
Data output is available in both true and complement forms from the 64th stage. Both the DATA OUT (Q) and $\overline{\text{DATA OUT}}$ ($\overline{Q}$) outputs are fully buffered.

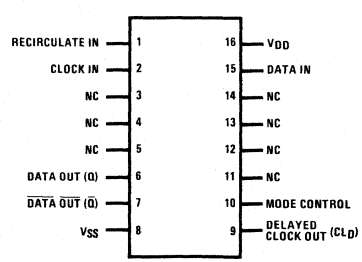
The CLOCK input of the CD4031BM/CD4031BC is fully buffered, and presents only a standard input load capacitance. However, a DELAYED CLOCK OUTPUT (CL_D) has been provided to allow reduced clock drive fan-out and transition time requirements when cascading packages.

features

- Wide supply voltage range — 3.0 V to 15 V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Fully static operation — DC to 8 MHz (typical @ V_{DD} = 10 V)
- Fully buffered clock input — 5 pF (typ) input capacitance
- Single phase clocking requirements
- Delayed clock output for reduced clock drive requirements
- Fully buffered outputs
- High Current Sinking Capability, Q Output — 1.6 mA @ V_{DD} = 5 V and 25°C

logic and connection diagrams





absolute maximum ratings (Notes 1 & 2)

V_{DD}	Supply Voltage	−0.5 V to +18 V
V_{IN}	Input Voltage	−0.5 V to V_{DD} + 0.5 V
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions (Note 2)

V_{DD}	Supply Voltage	+3 V to +15 V
V_{IN}	Input Voltage	0 V to V_{DD}
T_A	Operating Temperature Range	
	CD4031BM	−55°C to +125°C
	CD4031BC	−40°C to +85°C

dc electrical characteristics (Note 2) CD4031BM

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		5		0.01	5		150	μA
		V_{DD} = 10 V		10		0.01	10		300	μA
		V_{DD} = 15 V		20		0.02	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, V_{IH} = V_{DD}, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\ \mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\ \mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V	2.3		1.9	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	5.1		4.2	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V	10.5		8.8	17		6.1		mA
I_{OL}	Low Level Output Current, Q and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, V_{IH} = V_{DD}, V_{IL} = 0 V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.1		10^{-5}	0.1		1.0	μA

truth tables

MODE CONTROL (data selection)

MODE CONTROL	DATA IN	RECIRCULATE IN	DATA INTO FIRST STAGE
0	0	X	0
0	1	X	1
1	X	0	0
1	X	1	1

EACH STAGE

D_n	CL	Q_n
0	⌐	0
1	⌐	1
X	⌙	NC

X = irrelevant
NC = no change
⌐ = Low to High level transition
⌙ = High to Low level transition

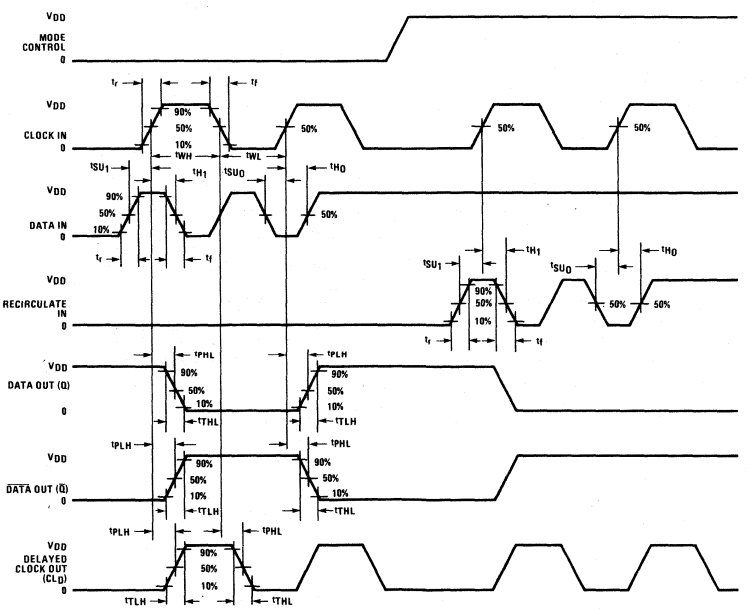
dc electrical characteristics (Note 2) CD4031BC

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		20		0.01	20		150	μA
		V_{DD} = 10 V		40		0.01	40		300	μA
		V_{DD} = 15 V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V, $\|I_O\| < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\|I_O\| < 1\ \mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\ \mu A$		3.0		4.5	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\|I_O\| < 1\ \mu A$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V, $\|I_O\| < 1\ \mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10 V, V_O = 1.0 V or 9.0 V, $\|I_O\| < 1\ \mu A$	7.0		7.0	5.5		7.0		V
		V_{DD} = 15 V, V_O = 1.5 V or 13.5 V, $\|I_O\| < 1\ \mu A$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current, Q Output	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	1.8		1.6	3.8		1.3		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	4.0		3.5	8.4		2.8		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	8.7		7.5	17		6.1		mA
I_{OL}	Low Level Output Current, Q and CL_D Outputs	V_{DD} = 5 V, V_O = 0.4 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15 V, V_O = 1.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current, All Outputs	V_{DD} = 5 V, V_O = 4.6 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15 V, V_O = 13.5 V, $V_{IH} = V_{DD}$, V_{IL} = 0 V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

switching time waveforms



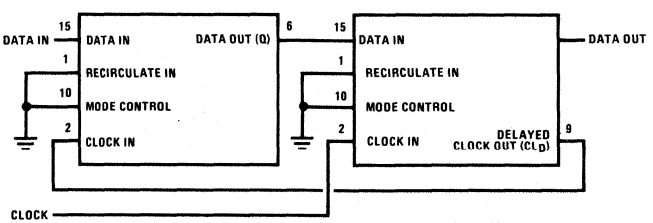
ac electrical characteristics $T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200K\Omega$, $t_r = t_f = 20\,ns$, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to Q and $\overline{Q}$	$V_{CC} = 5\,V$		300	600	ns
		$V_{CC} = 10\,V$		125	250	ns
		$V_{CC} = 15\,V$		100	200	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock to CL_D	$V_{CC} = 5\,V$		125	250	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
t_{THL}, t_{TLH}	Output Transition Time, All Outputs	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{SU_0} t_{SU_1}	Minimum Data Setup Time, DATA IN or RECIRCULATE IN to Clock	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{H_0} t_{H_1}	Minimum Data Hold Time, Clock to DATA IN or RECIRCULATE IN	$V_{CC} = 5\,V$		100	200	ns
		$V_{CC} = 10\,V$		50	100	ns
		$V_{CC} = 15\,V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{CC} = 5\,V$		150	300	ns
		$V_{CC} = 10\,V$		60	125	ns
		$V_{CC} = 15\,V$		50	100	ns
f_{CL}	Maximum Clock Frequency	$V_{CC} = 5\,V$	1.6	3.2		MHz
		$V_{CC} = 10\,V$	4.0	8.0		MHz
		$V_{CC} = 15\,V$	5.0	10		MHz
t_{RCL}, t_{FCL}	Maximum Clock Input Rise and Fall Times (Note 3)	$V_{CC} = 5\,V$	15			μs
		$V_{CC} = 10\,V$	10			μs
		$V_{CC} = 15\,V$	5			μs
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

Note 3: When clocking cascaded packages in parallel, one should insure that: $t_{r\,CL} \leq 2(t_{PD} - t_H)$ where: t_{PD} = the propagation delay of the driving stage and t_H = the hold time of the driven stage.

block diagram

cascading packages using DELAYED CLOCK (CL_D) output



National Semiconductor

CD4034BM/CD4034BC 8-State TRI-STATE® Bidirectional Parallel/Serial Input/Output Bus Register

general description

The CD4034BM/CD4034BC is an 8-bit CMOS static shift register with two parallel bidirectional data ports (A and B) which, when combined with serial shifting operations, can be used to (1) bidirectionally transfer parallel data between two buses, (2) convert serial data to parallel form and direct them to either of two buses, (3) store (recirculate) parallel data, or (4) accept parallel data from either of two buses and convert them to serial form. These operations are controlled by five control inputs:

A ENABLE (AE) – "A" data port is enabled only when AE is at logical "1." This allows the use of a common bus for multiple packages.

A-BUS-TO-B-BUS/B-BUS-TO-A-BUS (A/B) – This input controls the direction of data flow. When at logical "1," data flows from port A to B (A is input, B is output). When at logical "0," the data flow direction is reversed.

ASYNCHRONOUS/SYNCHRONOUS (A/S) – When A/S is at logical "0," data transfer occurs at positive transition of the CLOCK. When A/S is at logical "1," data transfer is independent of the CLOCK for parallel operation. In serial mode A/S input is internally disabled such that the operation is always synchronous. (Asynchronous serial operation is not possible.)

PARALLEL/SERIAL (P/S) – A logical "1" P/S input allows data transfer into the registers via A or B port (synchronous if A/S = logical "0," asynchronous if A/S = logical "1"). A logical "0" P/S allows serial data to transfer into the register synchronously with the positive transition of the CLOCK, independent of the A/S input.

CLOCK – Single phase, enabled only in synchronous mode. (Either P/S = logical "1" and A/S = logical "0" or P/S = logical "0.")

All register stages are D-type master-slave flip-flops with separate master and slave clock inputs generated internally to allow synchronous or asynchronous data transfer from master to slave.

All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

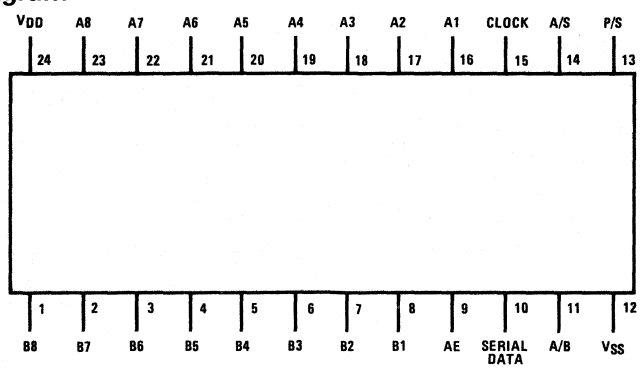
features

■ Wide supply voltage range	3.0 V to 18 V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ RCA CD4034B second source	

applications

- Parallel Input/Parallel Output
  Parallel Input/Serial Output
  Serial Input/Parallel Output
  Serial Input/Serial Output Register
- Shift right/shift left register
- Shift right/shift left with parallel loading
- Address register
- Buffer register
- Bus system register with enable parallel lines at bus side
- Double bus register system
- Up-Down Johnson or ring counter
- Pseudo-random code generators
- Sample and hold register (storage, counting, display)
- Frequency and phase comparator

connection diagram



absolute maximum ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions (Note 2)

V_{DD}	DC Supply Voltage	$+3\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
	CD4034BM	$-55°C$ to $+125°C$
	CD4034BC	$-40°C$ to $+85°C$

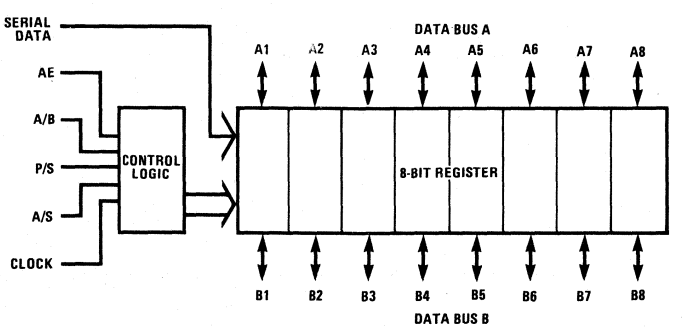
dc electrical characteristics— CD4034BM (Note 2)

PARAMETER	CONDITIONS	−55°C		+25°C			+125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	$V_{DD} = 5\ V$		5			5		150	μA
	$V_{DD} = 10\ V$		10			10		300	μA
	$V_{DD} = 15\ V$		20			20		600	μA
V_{OL} Low Level Output Voltage	$V_{DD} = 5\ V$		0.05			0.05		0.05	V
	$V_{DD} = 10\ V$		0.05			0.05		0.05	V
	$V_{DD} = 15\ V$		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	$V_{DD} = 5\ V$	4.95		4.95			4.95		V
	$V_{DD} = 10\ V$	9.95		9.95			9.95		V
	$V_{DD} = 15\ V$	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$		1.5			1.5		1.5	V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$		3.0			3.0		3.0	V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$V_{DD} = 5\ V$, $V_O = 0.5\ V$ or $4.5\ V$	3.5		3.5			3.5		V
	$V_{DD} = 10\ V$, $V_O = 1.0\ V$ or $9.0\ V$	7.0		7.0			7.0		V
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$ or $13.5\ V$	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	$V_{DD} = 5\ V$, $V_O = 0.4\ V$	0.64		0.51			0.36		mA
	$V_{DD} = 10\ V$, $V_O = 0.5\ V$	1.6		1.3			0.9		mA
	$V_{DD} = 15\ V$, $V_O = 1.5\ V$	4.2		3.4			2.4		mA
I_{OH} High Level Output Current	$V_{DD} = 5\ V$, $V_O = 4.6\ V$	−0.64		−0.51			−0.36		mA
	$V_{DD} = 10\ V$, $V_O = 9.5\ V$	−1.6		−1.3			−0.9		mA
	$V_{DD} = 15\ V$, $V_O = 13.5\ V$	−4.2		−3.4			−2.4		mA
I_{IN} Input Current	$V_{DD} = 15\ V$, $V_{IN} = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_{IN} = 15\ V$		0.1		10^{-5}	0.1		1.0	μA
I_{OZ} Tri-State Leakage Current	$V_{DD} = 15\ V$, $V_O = 0\ V$	−0.1		−0.1	-10^{-5}		−1.0		μA
	$V_{DD} = 15\ V$, $V_O = 15\ V$		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0\ V$ unless otherwise specified.

logic diagram



dc electrical characteristics — CD4034BC (Note 2)

PARAMETER	CONDITIONS	−40°C		+25°C			+85°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5 V		20			20		150	μA
	V_{DD} = 10 V		40			40		300	μA
	V_{DD} = 15 V		80			80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5 V		0.05			0.05		0.05	V
	V_{DD} = 10 V		0.05			0.05		0.05	V
	V_{DD} = 15 V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5 V	4.95		4.95			4.95		V
	V_{DD} = 10 V	9.95		9.95			9.95		V
	V_{DD} = 15 V	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V		1.5			1.5		1.5	V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V		3.0			3.0		3.0	V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V or 4.5 V	3.5		3.5			3.5		V
	V_{DD} = 10 V, V_O = 1.0 V or 9.0 V	7.0		7.0			7.0		V
	V_{DD} = 15 V, V_O = 1.5 V or 13.5 V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44			0.36		mA
	V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1			0.9		mA
	V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0			2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44			−0.36		mA
	V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1			−0.9		mA
	V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0			−2.4		mA
I_{IN} Input Current	V_{DD} = 15 V, V_{IN} = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_{IN} = 15 V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ} Tri-State Leakage Current	V_{DD} = 15 V, V_O = 0 V	−0.3		−0.3	-10^{-5}		−1.0		μA
	V_{DD} = 15 V, V_O = 15 V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, input $t_r = t_f$ = 20 ns, unless otherwise specified.

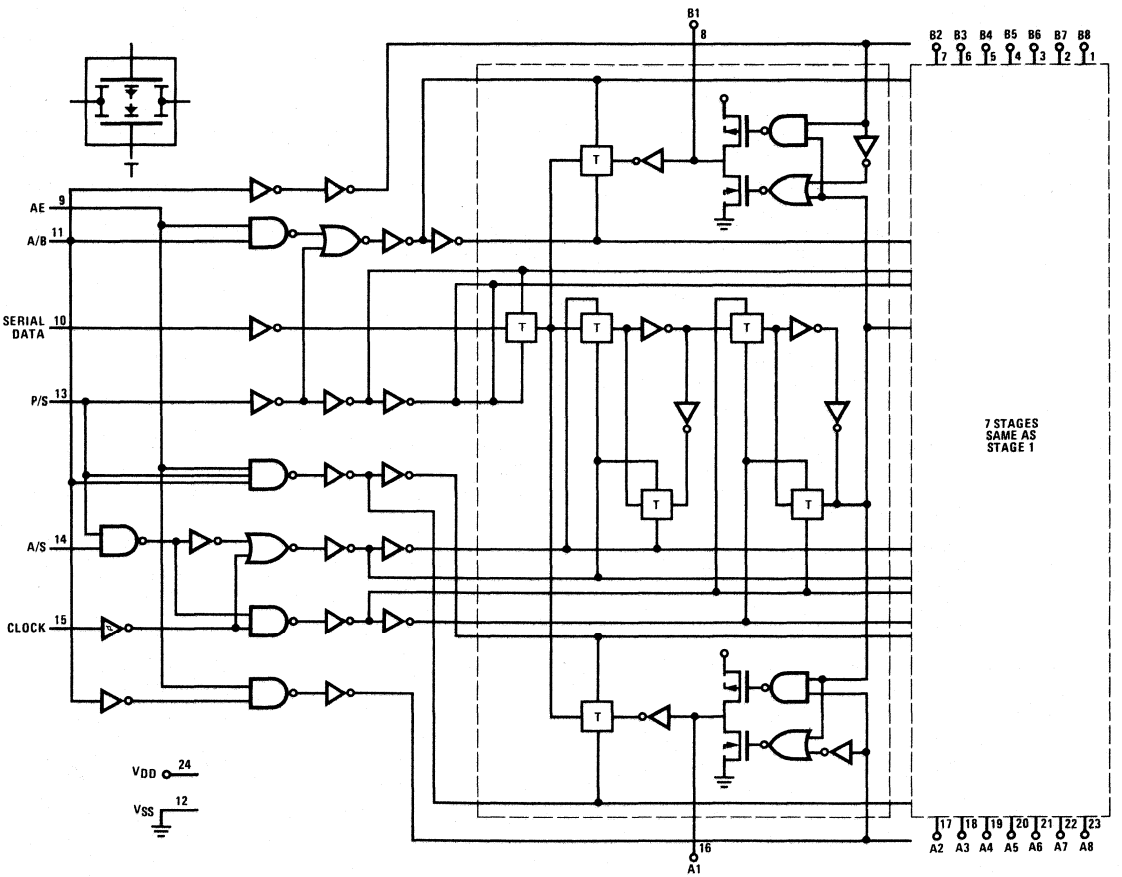
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) Synchronous Parallel Data or Serial Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHL}, t_{PLH}	Propagation Delay Time, A(B) A(B) Asynchronous Parallel Data Input, B(A) Parallel Data Output	V_{DD} = 5 V		280	700	ns
		V_{DD} = 10 V		120	270	ns
		V_{DD} = 15 V		85	190	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from A/B or AE to High Impedance State at A Outputs or from A/B to High Impedance State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		95	220	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		60	130	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		45	100	ns
t_{PZH}, t_{PZL}	Propagation Delay Time from A/B or AE to Logical "1" or Logical "0" State at A Outputs or from A/B to Logical "1" or Logical "0" State at B Outputs	V_{DD} = 5 V, R_L = 1.0KΩ		180	480	ns
		V_{DD} = 10 V, R_L = 1.0KΩ		75	190	ns
		V_{DD} = 15 V, R_L = 1.0KΩ		55	140	ns
t_{THL}, t_{TLH}	Output Transition Time	V_{DD} = 5 V		100	200	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		40	80	ns
f_{CL}	Maximum Clock Input Frequency	V_{DD} = 5 V	2	4		MHz
		V_{DD} = 10 V	5	10		MHz
		V_{DD} = 15 V	7	14		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5 V		125	250	ns
		V_{DD} = 10 V		50	100	ns
		V_{DD} = 15 V		35	70	ns

ac electrical characteristics (cont'd.)

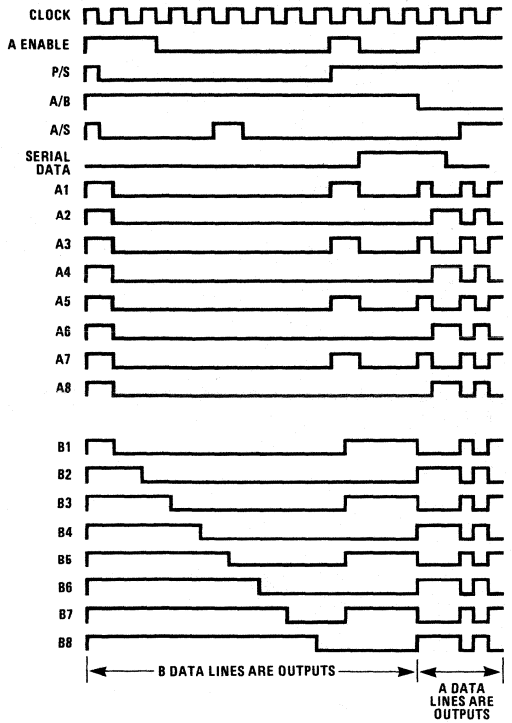
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{RCL}, t_{FCL}	Maximum Clock Rise & Fall Time	V_{DD} = 5 V	15			μs
		V_{DD} = 10 V	15			μs
		V_{DD} = 15 V	15			μs
t_{SU}	Parallel (A or B) and Serial Data Setup Time	V_{DD} = 5 V		25	70	ns
		V_{DD} = 10 V		10	30	ns
		V_{DD} = 15 V		7	20	ns
t_{SU}	Control Inputs AE, A/B, P/S, A/S Setup Time	V_{DD} = 5 V		110	280	ns
		V_{DD} = 10 V		35	100	ns
		V_{DD} = 15 V		20	60	ns
t_{WH}	Minimum High Level AE, A/B, P/S, A/S Pulse Width	V_{DD} = 5 V		160	400	ns
		V_{DD} = 10 V		70	160	ns
		V_{DD} = 15 V		40	90	ns
C_{IN}	Average Input Capacitance	A and B Data I/O and A/B Control Input		7	15	pF
		Any Other Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	(Note 3)		155		pF

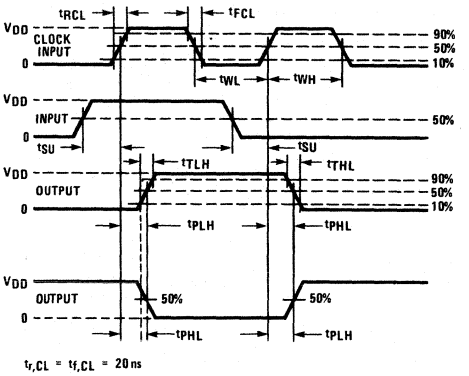
Note 3: C_{PD} determines the no-load power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

schematics diagram

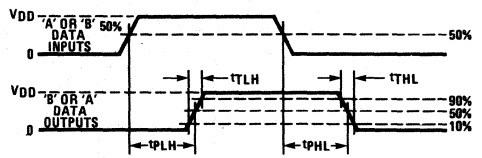


switching time waveforms and test circuits

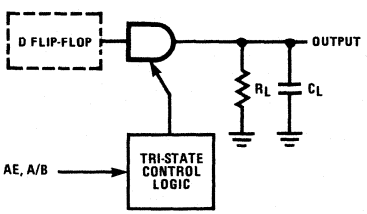


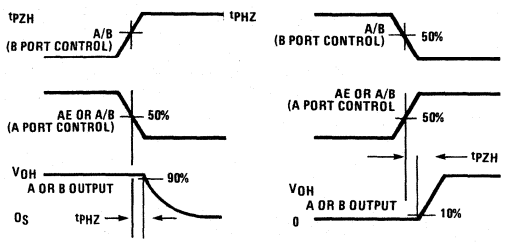


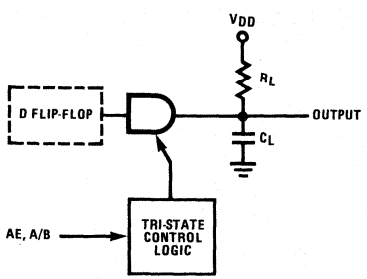
Synchronous Operation

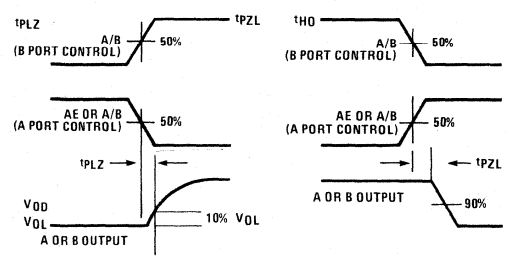


Asynchronous Operation

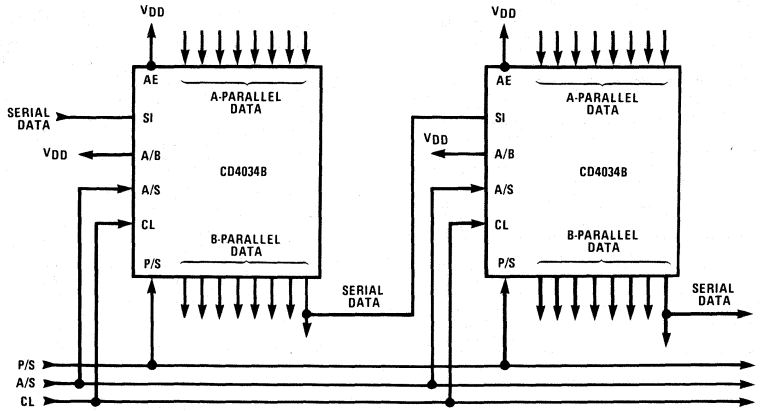




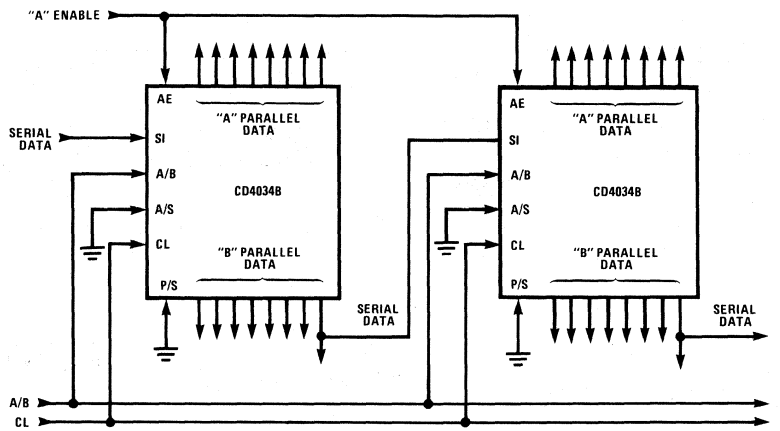




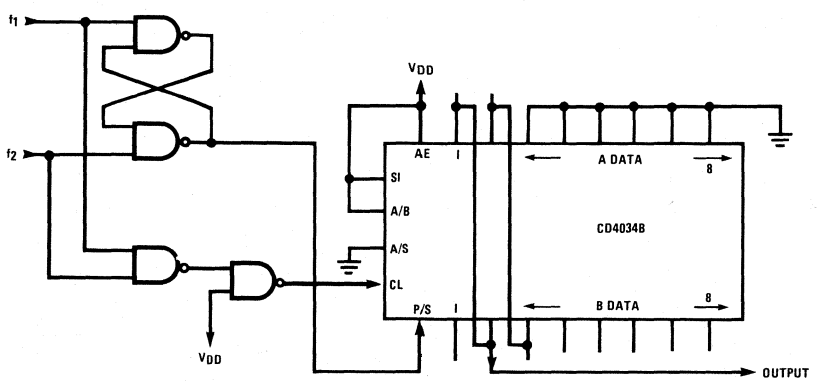
applications



16-Bit parallel in/parallel out,parallel in/ serial out, serial in/parallel out, serial in/ serial out register.

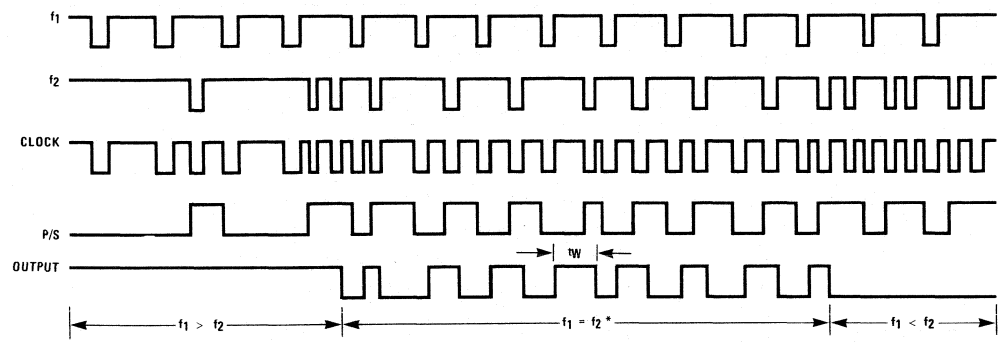


16-Bit serial in/gated parallel out register.

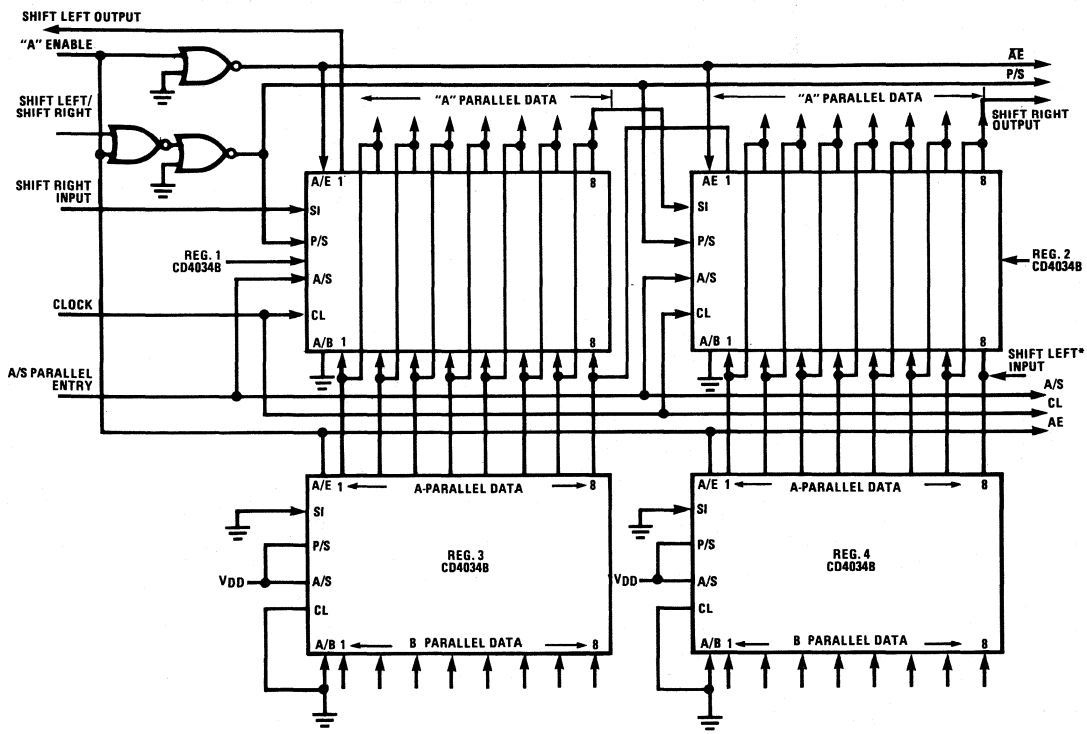


Frequency and Phase Comparator

applications (cont'd.)



*WHEN $f_1=f_2$, t_W IS PROPORTIONAL TO THE PHASE OF f_1 WITH RESPECT TO f_2



A "High" ("Low") on the Shift Left/Shift Right input allows serial data on the Shift Left Input (Shift Right Input) to enter the register on the positive transition of the clock signal. A "high" on the "A" Enable Input disables the "A" parallel data lines on Registers 1 and 2 and enables the "A" data lines on Registers 3 and 4 and allows parallel data into Registers 1 and 2. Other logic schemes may be used in place of registers 3 and 4 for parallel loading.

When parallel inputs are not used Registers 3 and 4 and associated logic are not required.

*Shift left input must be disabled during parallel entry.

Shift Right/Shift Left with Parallel Inputs

truth tables

"A" ENABLE	P/S	A/B	A/S	MODE	OPERATION*
0	0	0	X	Serial	Synchronous Serial data input, A- and B-Parallel data outputs disabled.
0	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
0	1	0	0	Parallel	B Synchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	0	1	Parallel	B Asynchronous Parallel data inputs, A-Parallel data outputs disabled.
0	1	1	0	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, synchronous data recirculation.
0	1	1	1	Parallel	A-Parallel data inputs disabled, B-Parallel data outputs, asynchronous data recirculation.
1	0	0	X	Serial	Synchronous Serial data input, A-Parallel data output.
1	0	1	X	Serial	Synchronous Serial data input, B-Parallel data output.
1	1	0	0	Parallel	B Synchronous Parallel data input, A-Parallel data output.
1	1	0	1	Parallel	B Asynchronous Parallel data input, A-Parallel data output.
1	1	1	0	Parallel	A Synchronous Parallel data input, B-Parallel data output.
1	1	1	1	Parallel	A Asynchronous Parallel data input, B-Parallel data output.

X = Don't Care

*For synchronous operation (serial mode or when A/S = 0 in parallel mode), outputs change state at positive transition of the clock.

National Semiconductor

CD4035BM/CD4035BC 4-Bit Parallel-In/Parallel-Out Shift Register

general description

The CD4035B 4-bit parallel-in/parallel-out shift register is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. This shift register is a 4-stage clocked serial register having provisions for synchronous parallel inputs to each stage and serial inputs to the first stage via $J\overline{K}$ logic. Register stages 2, 3, and 4 are coupled in a serial "D" flip-flop configuration when the register is in the serial mode (parallel/serial control low).

Parallel entry via the "D" line of each register stage is permitted only when the parallel/serial control is "high."

In the parallel or serial mode information is transferred on positive clock transitions.

When the true/complement control is "high," the true contents of the register are available at the output terminals. When the true/complement control is "low", the outputs are the complements of the data in the register. The true/complement control functions asynchronously with respect to the clock signal.

$J\overline{K}$ input logic is provided on the first stage serial input to minimize logic requirements particularly in counting and sequence-generation applications. With $J\overline{K}$ inputs connected together, the first stage becomes a "D" flip-flop. An asynchronous common reset is also provided.

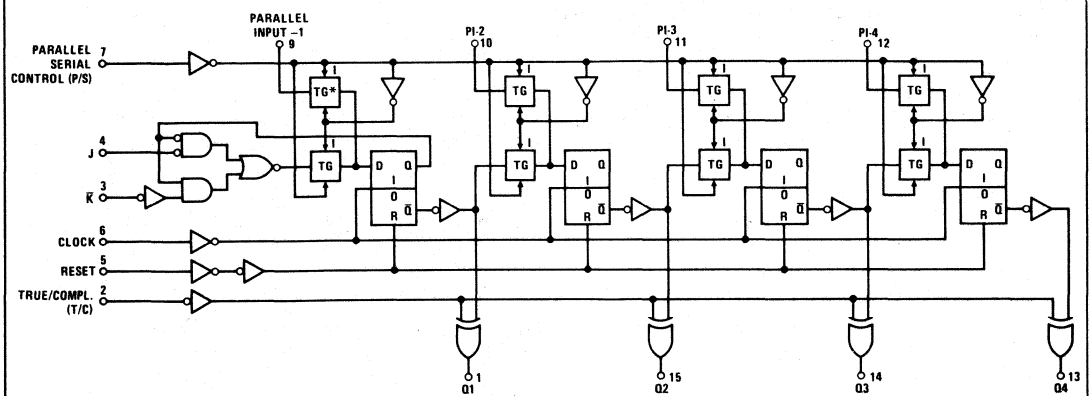
features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ 4-stage clocked shift operation	
■ Synchronous parallel entry on all 4 stages	
■ $J\overline{K}$ inputs on first stage	
■ Asynchronous true/complement control on all outputs	
■ Reset control	
■ Static flip-flop operation; master/slave configuration	
■ Buffered outputs	
■ Low-power dissipation	5 μW typ (ceramic)
■ High speed	to 5 MHz

applications

- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial controls
- Remote metering
- Computers

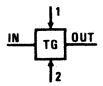
logic diagram



P/S = 0 = serial mode

T/C =1 = true outputs

*TG = transmission gate



Input to output is:

a) A bidirectional low impedance when control input 1 is low and control input 2 is high.

b) An open circuit when control input 1 is high and control input 2 is low.

absolute maximum ratings (Note 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4035BM	−55°C to +125°C
CD4035BC	−40°C to +85°C

dc electrical characteristics CD4035BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.3	5		150	μA
		V_{DD} = 10V		10		0.5	10		300	μA
		V_{DD} = 15V		20		1.0	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5 V		0.05		0	0.05		0.05	V
		V_{DD} = 10 V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1.0\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	0.36		−0.14		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4035BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.5	20		150	μA
		V_{DD} = 10V		40		1.0	40		300	μA
		V_{DD} = 15V		80		5.0	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V

dc electrical characteristics (Continued) CD4035BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.2		−0.16	−0.36		−0.12		mA
		V_{DD} = 10V, V_O = 9.5V	−0.5		−0.4	−0.9		−0.3		mA
		V_{DD} = 15V, V_O = 13.5V	−1.4		−1.2	−3.5		−1.0		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

ac electrical characteristics

T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified.

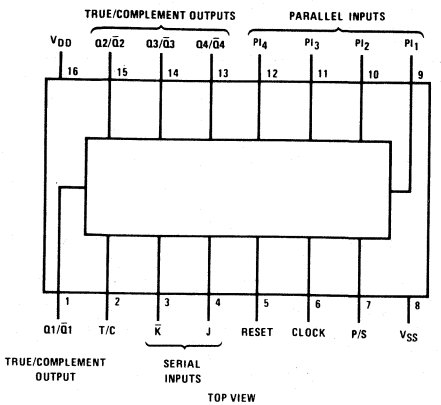
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}	Transition Time	V_{DD} = 5V		90	175	ns
		V_{DD} = 10V		50	75	ns
		V_{DD} = 15V		40	60	ns
t_{TLH}		V_{DD} = 5V		135	270	ns
		V_{DD} = 10V		70	140	ns
		V_{DD} = 15V		60	120	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	V_{DD} = 5V	335	135		ns
		V_{DD} = 10V	165	50		ns
		V_{DD} = 15V	100	40		ns
t_{rCL}, t_{fCL}	Clock Rise and Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			10	μs
		V_{DD} = 15V			5	μs
t_{SU}	Minimum Set-up Time					
	J/K Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
	Parallel-In Lines	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
	P/S Control	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	60	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	1.5	2.5		MHz
		V_{DD} = 10V	3	6		MHz
		V_{DD} = 15V	5	9		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
RESET OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	500	ns
		V_{DD} = 10V		150	200	ns
		V_{DD} = 15V		85	150	ns
t_{WH}	Minimum Reset Pulse Width	V_{DD} = 5V		75	400	ns
		V_{DD} = 10V		30	175	ns
		V_{DD} = 15V		25	130	ns

truth table

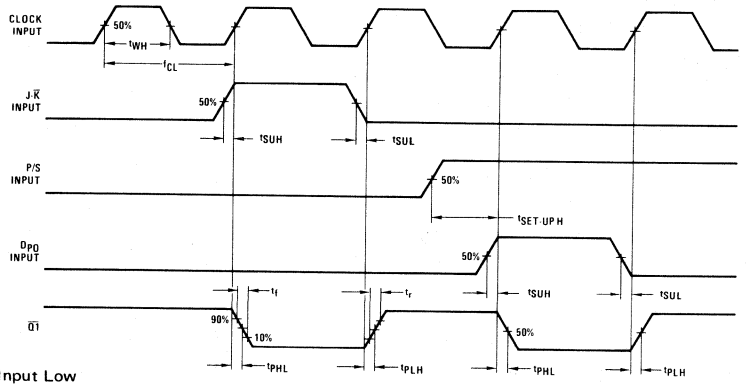
C_L	$t_n - 1$ (INPUTS)				t_n (OUTPUTS)
	J	$\overline{K}$	R	$Q_n - 1$	Q_n
⎍	0	X	0	0	0
⎍	1	X	0	0	1
⎍	X	0	0	1	0
⎍	1	0	0	Q_{n-1}	$\overline{Q_{n-1}}$ TOGGLE MODE
⎍	X	1	0	1	1
⎎	X	X	0	Q_{n-1}	Q_{n-1}
X	X	X	1	X	0

connection diagram

Dual-In-Line and Flat Package



switching time waveforms



T/C Input Low
Reset Input Low

National Semiconductor

CD4041M/CD4041C Quad True/Complement Buffer

general description

The CD4041M/CD4041C is a quad true/complement buffer consisting of N- and P-channel enhancement mode transistors having low-channel resistance and high current (sourcing and sinking) capability. The CD4041 is intended for use as a buffer, line driver, or CMOS-to-TTL driver.

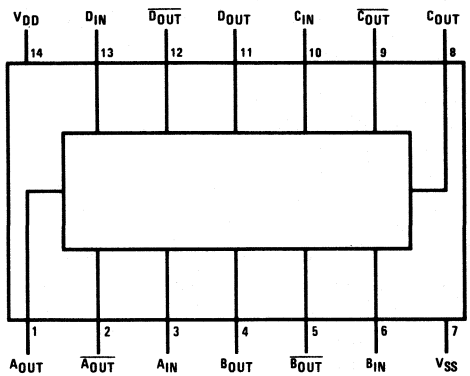
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 40% V_{DD} typ
- True output
  - High current source and sink capability
  - 8 mA (typ) @ V_O = 9.5V, V_{DD} = 10V
  - 3.2 mA (typ) @ V_O = 0.4V, V_{DD} = 5V (two TTL loads)
- Complement output
  - Medium current source and sink capability
  - 3.6 mA (typ) @ V_O = 9.5V, V_{DD} = 10V
  - 1.6 mA (typ) @ V_O = 0.4V, V_{DD} = 5V

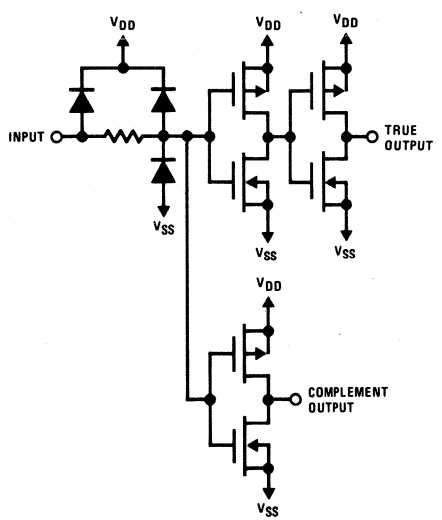
connection diagram

Dual-In-Line and Flat Package



TOP VIEW

schematic diagram



1 of 4 Identical Units

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4041M	−55°C to +125°C
CD4041C	−40°C to +85°C

dc electrical characteristics CD4041M (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.01	1		30	μA
		V_{DD} = 10V		2		0.01	2		60	μA
		V_{DD} = 15V		4		0.01	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2.0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4.0		4.0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8.0		8.0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V								
	True Output	V_{DD} = 5V, V_O = 0.4V	2.1		1.6	3.2		1.2		mA
		V_{DD} = 10V, V_O = 0.5V	6.25		5.0	10		3.5		mA
		V_{DD} = 15V, V_O = 1.5V	14		12	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	V_{DD} = 5V, V_O = 0.4V	1.0		0.8	1.6		0.55		mA
		V_{DD} = 10V, V_O = 0.5V	2.5		2	4.0		1.4		mA
		V_{DD} = 15V, V_O = 1.5V	5.5		4.5	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	V_{DD} = 5V, V_O = 4.6V	−1.75		−1.4	−2.8		−1.0		mA
		V_{DD} = 10V, V_O = 9.5V	−5.0		−4.0	−8.0		−2.8		mA
		V_{DD} = 15V, V_O = 13.5V	−11		−9	−18		−6		mA
I_{OH}	High Level Output Current	V_{IL} = 0V								
	Complement Output	V_{DD} = 5V, V_O = 4.6V	−0.75		−0.6	−1.2		−0.4		mA
		V_{DD} = 10V, V_O = 9.5V	−2.25		−1.8	−3.6		−1.25		mA
		V_{DD} = 15V, V_O = 13.5V	−4.8		−4	−8		−2.7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

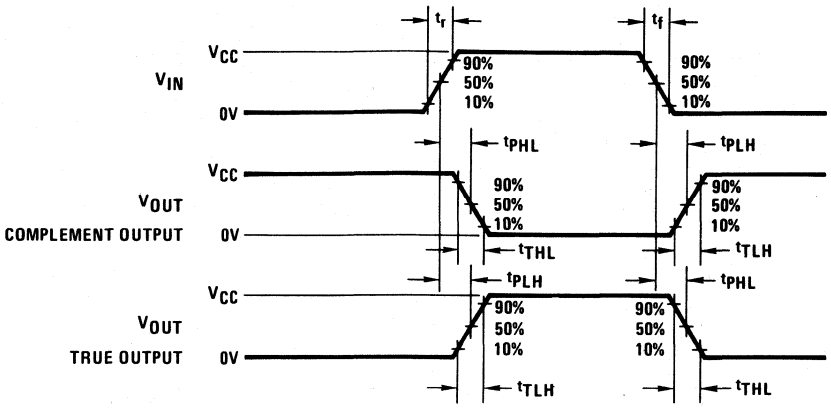
dc electrical characteristics CD4041C (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.01	4		30	μA
		V_{DD} = 10V		8		0.01	8		60	μA
		V_{DD} = 15V		16		0.01	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, V_{IL} = 0V, $V_{IH} = V_{DD}$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.0		2	1.0		1.0	V
		V_{DD} = 10V, V_O = 1V or 9V		2.0		4	2.0		2.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		3.0		6	3.0		3.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	4.0		4.0	3		4.0		V
		V_{DD} = 10V, V_O = 1V or 9V	8.0		8.0	6		8.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	12.0		12.0	9		12.0		V
I_{OL}	Low Level Output Current	V_{IL} = 0V								
	True Output	V_{DD} = 5V, V_O = 0.4V	1.7		1.5	3.2		1.2		mA
		V_{DD} = 10V, V_O = 0.5V	4.9		4.3	10		3.5		mA
		V_{DD} = 15V, V_O = 1.5V	11		10	24		8		mA
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$								
	Complement Output	V_{DD} = 5V, V_O = 0.4V	0.75		0.68	1.6		0.55		mA
		V_{DD} = 10V, V_O = 0.5V	2.0		1.8	4.0		1.4		mA
		V_{DD} = 15V, V_O = 1.5V	4.4		3.8	9.0		3.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$								
	True Output	V_{DD} = 5V, V_O = 4.6V	−1.5		−1.3	−2.8		−1.0		mA
		V_{DD} = 10V, V_O = 9.5V	−4.0		−3.5	−8.0		−2.8		mA
		V_{DD} = 15V, V_O = 13.5V	−8.7		−7.5	−18		−6		mA
I_{OH}	High Level Output Current	V_{IL} = 0V								
	Complement Output	V_{DD} = 5V, V_O = 4.6V	−0.57		−0.50	−1.2		−0.4		mA
		V_{DD} = 10V, V_O = 9.5V	−1.8		−1.6	−3.6		−1.25		mA
		V_{DD} = 15V, V_O = 13.5V	−3.9		−3.4	−8.0		−2.7		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, and $t_r = t_f$ = 20 ns unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		60	120	ns
	True Output	V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		25	50	ns
t_{PHL} or t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	150	ns
	Complement Output	V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		30	65	ns
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		55	110	ns
	True Output	V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		90	180	ns
	Complement Output	V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	75	ns
C_{IN}	Input Capacitance	Any Input		10	15	pF

switching time waveforms



National Semiconductor

CD4042BM/CD4042BC Quad Clocked D Latch

general description

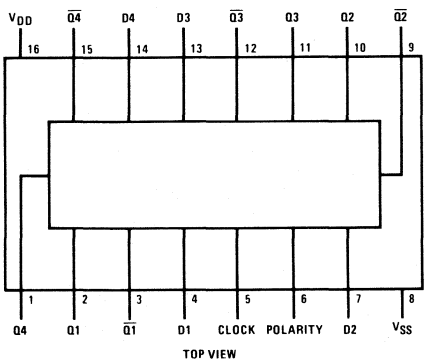
The CD4042BM/CD4042BC quad clocked "D" latch is a monolithic complementary MOS (CMOS) integrated circuit constructed with P and N-channel enhancement mode transistors. The outputs Q and $\overline{Q}$ either latch or follow the data input depending on the clock level which is programmed by the polarity input. For polarity = 0; the information present at the data input is transferred to Q and $\overline{Q}$ during 0 clock level; and for polarity = 1, the transfer occurs during the 1 clock level. When a clock transition occurs (positive for polarity = 0 and negative for polarity = 1) the information present at the input during the clock transition is retained at the outputs until an opposite clock transition occurs.

features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Clock polarity control	
■ Fully buffered data inputs	
■ Q and $\overline{Q}$ outputs	

connection diagram

Dual-In-Line and Flat Package

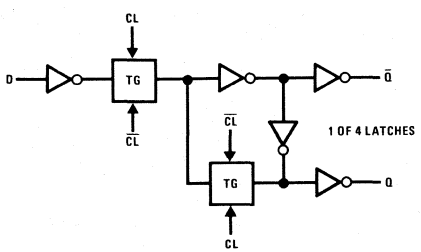


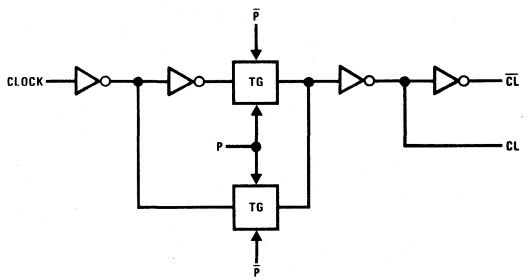
TOP VIEW

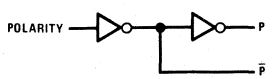
truth table

CLOCK	POLARITY	Q
0	0	D
⌐	0	Latch
1	1	D
⌐	1	Latch

logic diagrams







absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4042BM	−55°C to +125°C
CD4042BC	−40°C to +85°C

dc electrical characteristics CD4042BM (Note 2)

PARAMETERS		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.02	1		30	μA
		V_{DD} = 10V		2		0.02	2		60	μA
		V_{DD} = 15V		4		0.02	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4042BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.02	4		30	μA
		V_{DD} = 10V		8		0.02	8		60	μA
		V_{DD} = 15V		16		0.02	16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V

dc electrical characteristics (Continued) CD4042BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, and $t_r = t_f$ = 20 ns, unless otherwise specified.

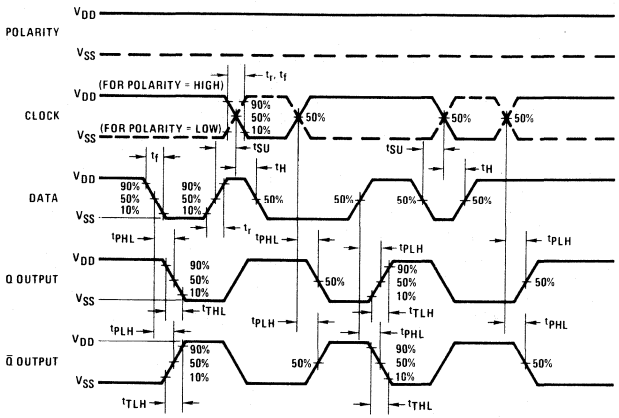
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to Q	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Data In to $\overline{Q}$	V_{DD} = 5V		150	300	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		80	160	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to $\overline{Q}$	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		115	230	ns
		V_{DD} = 15V		90	180	ns
t_H	Minimum Hold Time	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time	V_{DD} = 5V		0	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	25	ns
t_W	Minimum Clock Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		30	60	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		60	125	ns
		V_{DD} = 15V		50	100	ns
C_{IN}	Input Capacitance	Any Input		5.0	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Being a latch, the CD4042BM/CD4042BC is not clock rise and fall time sensitive.

switching time waveforms



National Semiconductor

CD4043M/CD4043C Quad TRI-STATE® NOR R/S Latches
CD4044M/CD4044C Quad TRI-STATE® NAND R/S Latches

general description

CD4043M/CD4043C is quad cross-couple TRI-STATE CMOS NOR latches, and CD4044M/CD4044C is quad cross-couple TRI-STATE CMOS NAND latches. Each latch has a separate Q output and individual SET and RESET inputs. It has a common TRI-STATE ENABLE input for all four latches. A logic "1" on the ENABLE input connects the latch states to the Q outputs. A logic "0" on the ENABLE input disconnects the latch states from the Q outputs resulting in an open circuit condition on the Q outputs. The TRI-STATE feature allows common bussing of the outputs.

features

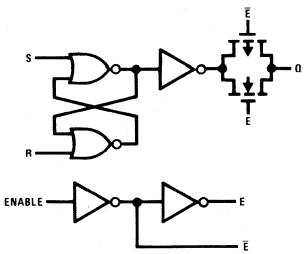
- Wide supply voltage range — 3V to 15V
- Low power — 100 nW typ.
- High noise immunity — 0.45 V_{DD} typ.
- Separate SET and RESET inputs for each latch
- NOR and NAND configuration
- TRI-STATE output with common output enable

applications

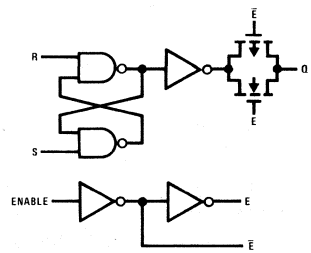
- Multiple bus storage
- Strobed register
- Four bits of independent storage with output enable
- General digital logic

schematic and connection diagrams

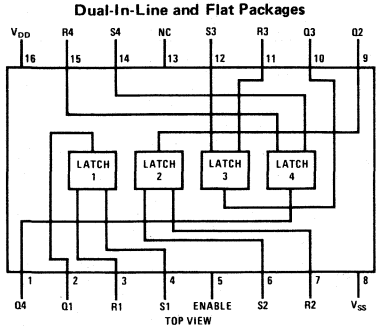
CD4043M/CD4043C



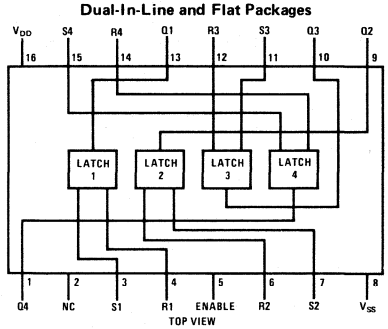
CD4044M/CD4044C



CD4043M/CD4043C
Dual-In-Line and Flat Packages



CD4044M/CD4044C
Dual-In-Line and Flat Packages



truth tables

CD4043M/CD4043C

S	R	E	Q
X	X	0	OC
0	0	1	NC
1	0	1	1
0	1	1	0
1	1	1	Δ

CD4044M/CD4044C

S	R	E	Q
X	X	0	OC
1	1	1	NC
0	1	1	1
1	0	1	0
0	0	1	ΔΔ

OC — TRI-STATE
NC — No change
X — Don't care
Δ — Dominated by S=1 input
ΔΔ — Dominated by R=0 input

absolute maximum ratings

Voltage at any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	
CD4043M/CD4044M	−55°C to +125°C
CD4043C/CD4044C	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Operating V_{DD} Range	V_{SS} + 3.0V to V_{SS} + 15V
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics CD4043M/CD4044M

PARAMETER		CONDITIONS	−55°C			25°C			125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Quiescent Device Current	V_{DD} = 5V			1		0.005	1			60	μA
		V_{DD} = 10V			2		0.005	2			120	μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5V			5		0.025	5			300	μW
		V_{DD} = 10V			20		0.05	20			1200	μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5V			0.01		0	0.01			0.05	V
		V_{DD} = 10V			0.01		0	0.01			0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5V	4.99			4.99	5		4.95			V
		V_{DD} = 10V	9.99			9.99	10		9.95			V
V_{NL}	Noise Immunity All Inputs	V_{DD} = 5V, V_O = 0.95V	1.5			1.5	2.25		1.4			V
		V_{DD} = 10V, V_O = 2.9V	3			3	4.5		2.9			V
V_{NH}	Noise Immunity All Inputs	V_{DD} = 5V, V_O = 3.6V	1.4			1.5	2.25		1.5			V
		V_{DD} = 10V, V_O = 7.2V	2.9			3	4.5		3			V
I_DN	Output Drive Current	V_{DD} = 5V, V_O = 0.5V	0.25			0.2	0.5		0.14			mA
		V_{DD} = 10V, V_O = 0.5V	0.61			0.5	1		0.35			mA
I_DP	Output Drive Current	V_{DD} = 5V, V_O = 4.5V	−0.22			−0.175	−0.5		−0.12			mA
		V_{DD} = 10V, V_O = 9.5V	−0.5			−0.4	−1		−0.28			mA
I_I	Input Current	Any Input					10					pA

dc electrical characteristics CD4043C/CD4044C

PARAMETER		CONDITIONS	−40°C			25°C			85°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_L	Quiescent Device Current	V_{DD} = 5V			10		0.01	10			140	μA
		V_{DD} = 10V			20		0.02	20			280	μA
P_D	Quiescent Device Dissipation/Package	V_{DD} = 5V			50		0.05	50			700	μW
		V_{DD} = 10V			200		0.2	200			2800	μW
V_{OL}	Output Voltage Low Level	V_{DD} = 5V			0.01		0	0.01			0.05	V
		V_{DD} = 10V			0.01		0	0.01			0.05	V
V_{OH}	Output Voltage High Level	V_{DD} = 5V	4.99			4.99	5		4.95			V
		V_{DD} = 10V	9.99			9.99	10		9.95			V
V_{NL}	Noise Immunity All Inputs	V_{DD} = 5V, V_O = 0.95V	1.5			1.5	2.25		1.4			V
		V_{DD} = 10V, V_O = 2.9V	3			3	4.5		2.9			V
V_{NH}	Noise Immunity All Inputs	V_{DD} = 5V, V_O = 3.6V	1.4			1.5	2.25		1.5			V
		V_{DD} = 10V, V_O = 7.2V	2.9			3	4.5		3			V
I_DN	Output Drive Current	V_{DD} = 5V, V_O = 0.5V	0.12			0.1	0.5		0.9			mA
		V_{DD} = 10V, V_O = 0.5V	0.3			0.25	1		0.22			mA
I_DP	Output Drive Current	V_{DD} = 5V, V_O = 4.5V	−0.11			−0.09	−0.5		−0.08			mA
		V_{DD} = 10V, V_O = 9.5V	−0.24			−0.2	−1		−0.18			mA
I_I	Input Current	Any Input					10					pA

ac electrical characteristics CD4043M/CD4044M

$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns.
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5V$		175	350	ns
		$V_{DD} = 10V$		75	175	ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
$t_{WH(S)}, t_{WH(R)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		80	200	ns
		$V_{DD} = 10V$		40	100	ns
t_{1H}, t_{0H}	Delay Time From Enable to High Impedance State	$V_{DD} = 5V$		60	150	ns
		$V_{DD} = 10V$		45	110	ns
		$R_L = 10k$				
		$C_L = 10$ pF				
t_{H1}, t_{H0}	Delay Time From Enable to Logical State	$V_{DD} = 5V$		90	250	ns
		$V_{DD} = 10V$		35	125	ns
		$R_L = 10k$				
		$C_L = 10$ pF				
C_I	Input Capacitance	Any Input		5		pF
C_O	Output Capacitance	Any Output		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 1)		50		pF

ac electrical characteristics CD4043C/CD4044C

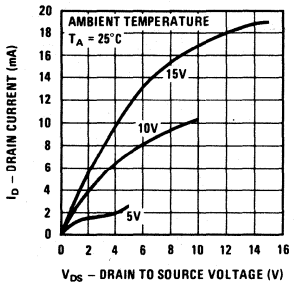
$T_A = 25°C$ and $C_L = 15$ pF and input rise and fall times = 20 ns.
Typical Temperature Coefficient for all values of $V_{DD} = 0.3\%/°C$.

	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PLH} = t_{PHL}$	Propagation Delay Time	$V_{DD} = 5V$		175	400	ns
		$V_{DD} = 10V$		75	200	ns
$t_{TLH} = t_{THL}$	Transition Time	$V_{DD} = 5V$		100	250	ns
		$V_{DD} = 10V$		50	125	ns
$t_{WH(S)}, t_{WH(R)}$	Minimum Set and Reset Pulse Width	$V_{DD} = 5V$		80	225	ns
		$V_{DD} = 10V$		40	110	ns
t_{1H}, t_{0H}	Delay Time From Enable to High Impedance State	$V_{DD} = 5V$		60	200	ns
		$V_{DD} = 10V$		45	150	ns
		$R_L = 10k$				
		$C_L = 10$ pF				
t_{H1}, t_{H0}	Delay Time From Enable to Logical State	$V_{DD} = 5V$		90	300	ns
		$V_{DD} = 10V$		35	150	ns
		$R_L = 10k$				
		$C_L = 10$ pF				
C_I	Input Capacitance	Any Input		5		pF
C_O	Output Capacitance	Any Output		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 1)		50		pF

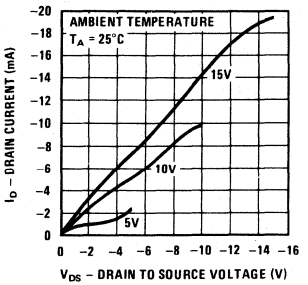
Note 1: C_{PD} determine the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C family characteristics application note AN-90.

typical performance characteristics

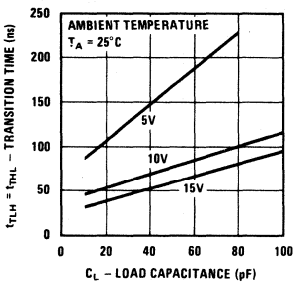
Typical Sink Current Characteristics



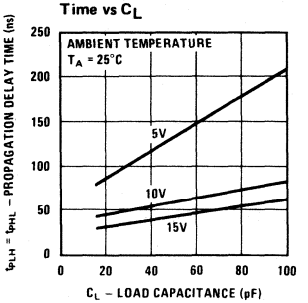
Typical Source Current Characteristics



Typical Transition Time vs C_L



Typical Propagation Delay Time vs C_L



National Semiconductor

CD4046BM/CD4046BC Micropower Phase-Locked Loop

general description

The CD4046B micropower phase-locked loop (PLL) consists of a low power, linear, voltage-controlled oscillator (VCO), a source follower, a zener diode, and two phase comparators. The two phase comparators have a common signal input and a common comparator input. The signal input can be directly coupled for a large voltage signal, or capacitively coupled to the self-biasing amplifier at the signal input for a small voltage signal.

Phase comparator I, an exclusive OR gate, provides a digital error signal (phase comp. I Out) and maintains 90° phase shifts at the VCO center frequency. Between signal input and comparator input (both at 50% duty cycle), it may lock onto the signal input frequencies that are close to harmonics of the VCO center frequency.

Phase comparator II is an edge-controlled digital memory network. It provides a digital error signal (phase comp. II Out) and lock-in signal (phase pulses) to indicate a locked condition and maintains a 0° phase shift between signal input and comparator input.

The linear voltage-controlled oscillator (VCO) produces an output signal (VCO Out) whose frequency is determined by the voltage at the VCO_{IN} input, and the capacitor and resistors connected to pin $C1_A$, $C1_B$, R1 and R2.

The source follower output of the VCO_{IN} (demodulator Out) is used with an external resistor of 10 kΩ or more. The INHIBIT input, when high, disables the VCO and source follower to minimize standby power consumption. The zener diode is provided for power supply regulation if necessary.

features

- Wide supply voltage range—3V to 18V
- Low dynamic power consumption—70 μW (typ) at f_o = 10 kHz, V_{DD} = 5V
- VCO frequency—1.3 MHz (typ) at V_{DD} = 10V
- Low frequency drift with temperature—0.06%/°C at V_{DD} = 10V
- High VCO linearity—1% (typ)

applications

- FM demodulator and modulator
- Frequency synthesis and multiplication
- Frequency discrimination
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Tone decoding
- FSK modulation
- Motor speed control

block and connection diagrams

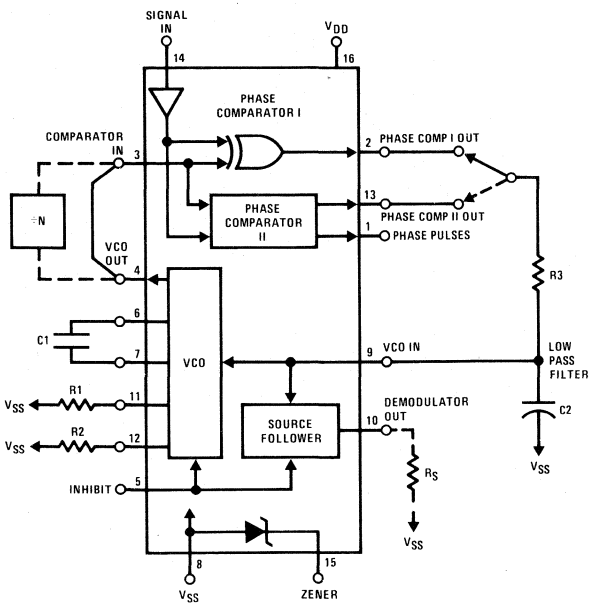
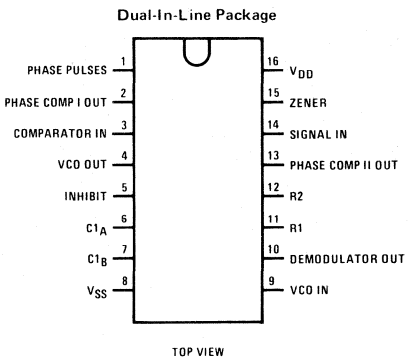


FIGURE 1

Dual-In-Line Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4046BM	−55°C to +125°C
CD4046BC	−40°C to +85°C

dc electrical characteristics CD4046BM (Note 2)

Parameter	Conditions	−55°C		25°C			125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3, 9 = V_{SS}								
	V_{DD} = 5V		5		0.005	5		150	μA
	V_{DD} = 10V		10		0.01	10		300	μA
	V_{DD} = 15V		20		0.015	20		600	μA
	PIN 5 = V_{DD}, PIN 14 = Open PIN 3,2 = V_{SS}								
	V_{DD} = 5V		45		5	35		185	μA
	V_{DD} = 10V		450		20	350		650	μA
	V_{DD} = 15V		1200		50	900		1500	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH} High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	All Inputs Except Signal Input								
	V_{DD} = 14V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
C_{IN} Input Capacitance	Any Input, (Note 3)							7.5	pF
P_T Total Power Dissipation	f_o = 10kHz, R1 = 1MΩ R2 = ∞, VCO_{IN} = V_{DD}/2								
	V_{DD} = 5V				0.07				mW
	V_{DD} = 10V				0.6				mW
	V_{DD} = 15V				2.4				mW

dc electrical characteristics CD4046BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	PIN 5 = V_{DD}, PIN 14 = V_{DD}, PIN 3,9 = V_{SS}								
	V_{DD} = 5V		20		0.005	20		150	μA
	V_{DD} = 10V		40		0.01	40		300	μA
	V_{DD} = 15V		80		0.015	80		600	μA
	PIN 5 = V_{DD}, PIN 14 = Open, PIN 3,9 = V_{SS}								
	V_{DD} = 5V		70		5	55		205	μA
	V_{DD} = 10V		530		20	410		710	μA
	V_{DD} = 15V		1500		50	1200		1800	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.25	4.0		4.0	V
V_{IH} High Level Input Voltage Comparator and Signal In	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		1..0	8.25		1..0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN} Input Current	All Inputs Except Signal Input								
	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
C_{IN} Input Capacitance	Any Input, (Note 3)					7.5			pF
P_T Total Power Dissipation	f_o = 10 kHz, R1 = 1 MΩ R2 = ∞, VCO_{IN} = V_{DD}/2								
	V_{DD} = 5V				0.07				mW
	V_{DD} = 10V				0.6				mW
	V_{DD} = 15V				2.4				mW

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

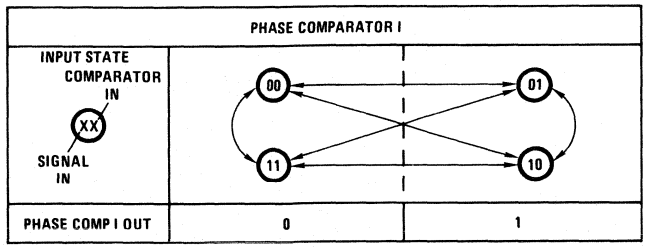
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

ac electrical characteristics CD4046BM/CD4046BC (C_L = 50 pF, T_A = 25°C)

Parameter	Conditions	Min	Typ	Max	Units
VCO Section					
Operating Current I_{DD}	f_0 = 10kHz, R1 = 1MΩ R2 = ∞, VCO_{IN} = V_{DD}/2				
	V_{DD} = 5V		20		μA
	V_{DD} = 10V		90		μA
	V_{DD} = 15V		200		μA
f_{MAX} = Maximum Operating Frequency	C1 = 50 pF, 41 = 10kΩ, R2 = ∞, VCO_{IN} = V_{DD}				
	V_{DD} = 5V	0.4	0.8		MHz
	V_{DD} = 10V	0.6	1.2		MHz
	V_{DD} = 15V	1.0	1.6		MHz
Linearity	VCO_{IN} = 2.5V ∓0.3V, R1 ⩾ 10kΩ, V_{DD} = 5V		1		%
	VCO_{IN} = 5V ±2.5V, R1⩾400kΩ, V_{DD} = 10V		1		%
	VCO_{IN} = 7.5V ±5V, R1 ⩾ 1 MΩ, V_{DD} = 15V		1		%
Temperature-Frequency Stability	%/°C∝1/f. V_{DD}				
No Frequency Offset, f_{MIN} = 0	R2 = ∞				
	V_{DD} = 5V		0.12–0.24		%/°C
	V_{DD} = 10V		0.04–0.08		%/°C
	V_{DD} = 15V		0.015–0.03		%/°C
Frequency Offset, $f_{MIN} \neq 0$	V_{DD} = 5V		0.06–0.12		%/°C
	V_{DD} = 10V		0.05–0.1		%/°C
	V_{DD} = 15V		0.03–0.06		%/°C
VCO_{IN} Input Resistance (VCO_{IN})	V_{DD} = 5V		10^6		MΩ
	V_{DD} = 10V		10^6		MΩ
	V_{DD} = 15V		10^6		MΩ
VCO Output Duty Cycle	V_{DD} = 5V		50		%
	V_{DD} = 10V		50		%
	V_{DD} = 15V		50		%
t_{THL} VCO Output Transition Time	V_{DD} = 5V		90	200	ns
t_{THL}	V_{DD} = 10V		50	100	ns
	V_{DD} = 15V		45	80	ns
Phase Comparators Section					
R_{IN} Input Resistance					
Signal Input	V_{DD} = 5V	1	3		MΩ
	V_{DD} = 10V	0.2	0.7		MΩ
	V_{DD} = 15V	0.1	0.3		MΩ
Comparator Input	V_{DD} = 5V		10^6		MΩ
	V_{DD} = 10V		10^6		MΩ
	V_{DD} = 15V		10^6		MΩ
AC-Coupled Signal Input Voltage Sensitivity	C_{SERIES} = 1000 pF f = 50 kHz				
	V_{DD} = 5V		200	400	mV
	V_{DD} = 10V		400	800	mV
	V_{DD} = 15V		700	1400	mV
Demodulator Output					
Offset Voltage (VCO_{IN} – V_{DEM})	RS ⩾ 10 kΩ, V_{DD} = 5V		1.50	2.2	V
	RS ⩾ 10 kΩ, V_{DD} = 10V		1.50	2.2	V
	RS ⩾ 50 kΩ, V_{DD} = 15V		1.50	2.2	V
Linearity	RS ⩾ 50 kΩ				
	VCO_{IN} = 2.5 ±0.3V, V_{DD} = 5V		0.1		%
	VCO_{IN} = 5 ±2.5V, V_{DD} = 10V		0.6		%
	VCO_{IN} = 7.5 ±5V, V_{DD} = 15V		0.8		%
Zener Diode					
V_Z Zener Diode Voltage					
CD4046BM	I_Z = 50μA	6.7	7.0	7.3	V
CD4046BC		6.3	7.0	7.7	V
R_Z Zener Dynamic Resistance	I_Z = 1mA		100		Ω

phase comparator state diagrams



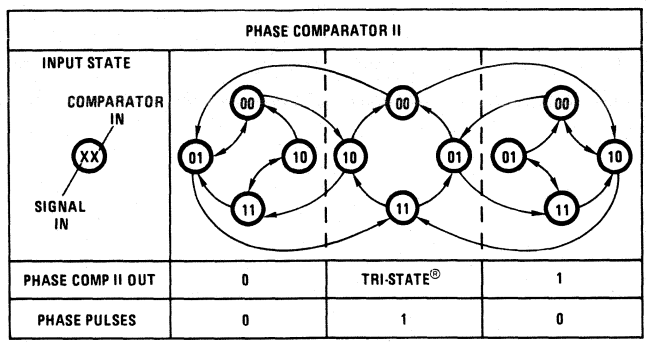


FIGURE 2

typical waveforms

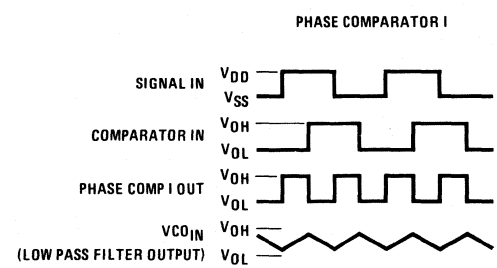


FIGURE 3. Typical Waveform Employing Phase Comparator I in Locked Condition

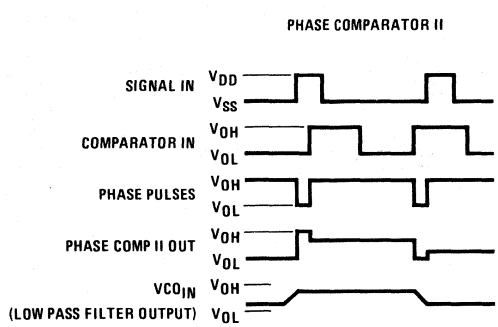


FIGURE 4. Typical Waveform Employing Phase Comparator II in Locked Condition

typical performance characteristics

Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ and 1 MΩ

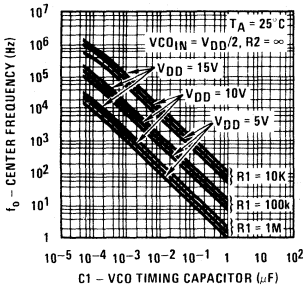


FIGURE 5a

Typical Frequency Offset vs C1 for R2 = 10 kΩ, 100 kΩ and 1 MΩ

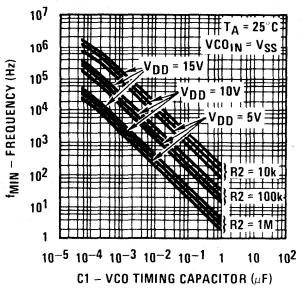


FIGURE 5b

Typical f_{MAX}/f_{MIN} vs R2/R1

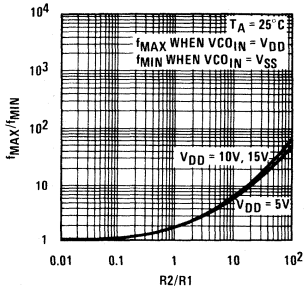


FIGURE 5c

Typical VCO Power Dissipation at Center Frequency vs R1

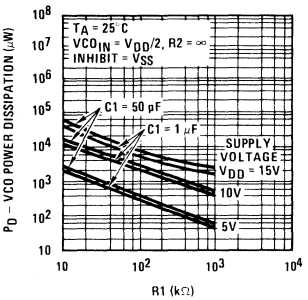


FIGURE 6a

Typical VCO Power Dissipation at f_{MIN} vs R2

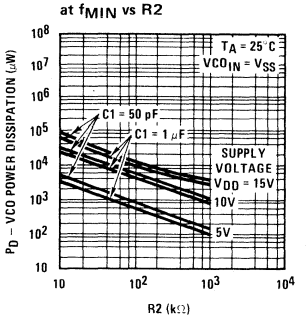


FIGURE 6b

Typical Source Follower Power Dissipation vs R_S

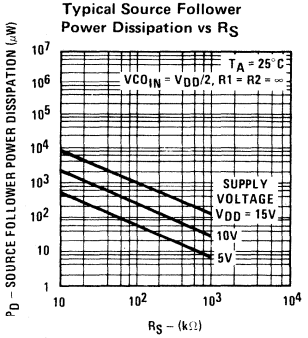


FIGURE 6c

Typical VCO Linearity vs R1 and C1

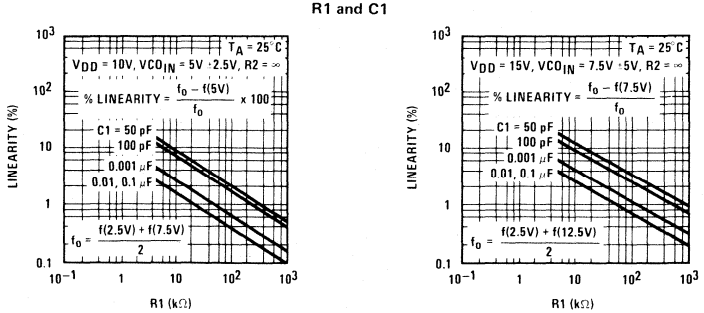


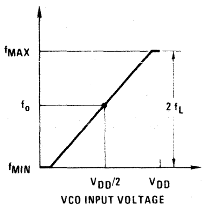
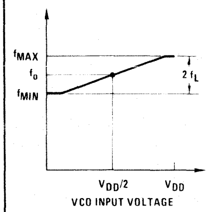
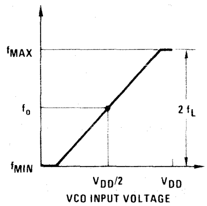
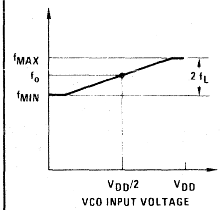
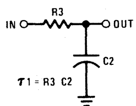
FIGURE 7

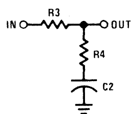
Note. To obtain approximate total power dissipation of PLL system for no-signal input: Phase Comparator I, P_D (Total) = P_D (f_o) + P_D (f_{MIN}) + P_D (R_S); Phase Comparator II, P_D (Total) = P_D (f_{MIN}).

design information

This information is a guide for approximating the value of external components for the CD4046B in a phase-locked-loop system. The selected external components must be within the following ranges: R1, R2 $\geq$ 10 kΩ, $R_S \geq$ 10 kΩ, C1 $\geq$ 50 pF.

In addition to the given design information, refer to *Figure 5* for R1, R2 and C1 component selections.

<table>
<tr><th rowspan="2">CHARACTERISTICS</th><th colspan="2">USING PHASE COMPARATOR I</th><th colspan="2">USING PHASE COMPARATOR II</th></tr>
<tr><th>VCO WITHOUT OFFSET
R2 = ∞</th><th>VCO WITH OFFSET</th><th>VCO WITHOUT OFFSET
R2 = ∞</th><th>VCO WITH OFFSET</th></tr>
<tr><td>VCO Frequency</td><td> 
</td><td> 
</td><td> 
</td><td> 
</td></tr>
<tr><td>For No Signal Input</td><td colspan="2">VCO in PLL system will adjust to center frequency, f_o</td><td colspan="2">VCO in PLL system will adjust to lowest operating frequency, f_{min}</td></tr>
<tr><td>Frequency Lock Range, 2 f_L</td><td colspan="4">2 f_L = full VCO frequency range
$2 f_L = f_{max} - f_{min}$</td></tr>
<tr><td>Frequency Capture Range, 2f_C</td><td colspan="2"> 

$2 f_C \approx \frac{1}{\pi}\sqrt{\frac{2\pi f_L}{\tau 1}}$</td><td colspan="2" rowspan="2">$f_C = f_L$</td></tr>
<tr><td>Loop Filter Component Selection</td><td colspan="2"> 

For 2 f_C, see Ref.</td></tr>
<tr><td>Phase Angle Between Signal and Comparator</td><td colspan="2">90° at center frequency (f_o), approximating 0° and 180° at ends of lock range (2 f_L)</td><td colspan="2">Always 0° in lock</td></tr>
<tr><td>Locks on Harmonics of Center Frequency</td><td colspan="2">Yes</td><td colspan="2">No</td></tr>
<tr><td>Signal Input Noise Rejection</td><td colspan="2">High</td><td colspan="2">Low</td></tr>
<tr><td>VCO Component Selection</td><td>–Given: f_o
–Use f_o with *Figure 5a* to determine R1 and C1</td><td>–Given: f_o and f_L
–Calculate f_{min} from the equation
$f_{min} = f_o - f_L$
–Use f_{min} with *Figure 5b* to determine R2 and C1
–Calculate $\frac{f_{max}}{f_{min}}$ from the equation
$\frac{f_{max}}{f_{min}} = \frac{f_o + f_L}{f_o - f_L}$
–Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1</td><td>–Given: f_{max}
–Calculate f_o from the equation
$f_o = \frac{f_{max}}{2}$
–Use f_o with *Figure 5a* to determine R1 and C1</td><td>–Given: f_{min} and f_{max}
–Use f_{min} with *Figure 5b* to determine R2 and C1
–Calculate $\frac{f_{max}}{f_{min}}$
–Use $\frac{f_{max}}{f_{min}}$ with *Figure 5c* to determine ratio R2/R1 to obtain R1</td></tr>
</table>

REF. G.S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.
Floyd Gardner, "Phaselock Techniques," John Wiley & Sons, 1966.

National Semiconductor

CD4047BM/CD4047BC Low Power Monostable/Astable Multivibrator

general description

CD4047B is capable of operating in either the monostable or astable mode. It requires an external capacitor (between pins 1 and 3) and an external resistor (between pins 2 and 3) to determine the output pulse width in the monostable mode, and the output frequency in the astable mode.

Astable operation is enabled by a high level on the astable input or low level on the $\overline{\text{astable}}$ input. The output frequency (at 50% duty cycle) at Q and $\overline{Q}$ outputs is determined by the timing components. A frequency twice that of Q is available at the Oscillator Output; a 50% duty cycle is not guaranteed.

Monostable operation is obtained when the device is triggered by low-to-high transition at + triggger input or high-to-low transition at – trigger input. The device can be retriggered by applying a simultaneous low-to-high transition to both the + trigger and retrigger inputs.

A high level on Reset input resets the outputs Q to low, $\overline{Q}$ to high.

features

■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or driving 74LS

SPECIAL FEATURES

- Low power consumption: special CMOS oscillator configuration
- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external R and C required

MONOSTABLE MULTIVIBRATOR FEATURES

- Positive or negative-edge trigger
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse width expansion
- Long pulse widths possible using small RC components by means of external counter provision
- Fast recovery time essentially independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

ASTABLE MULTIVIBRATOR FEATURES

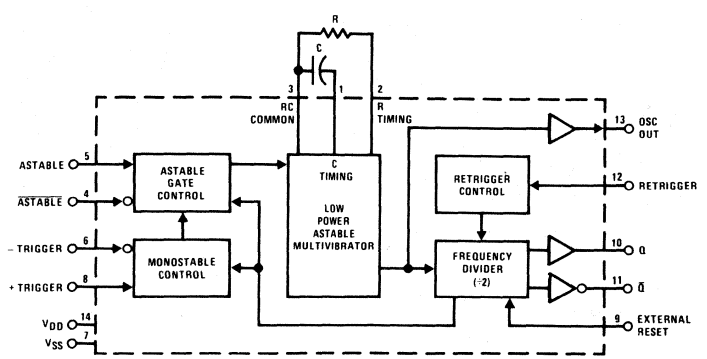
- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available
- Good astable frequency stability

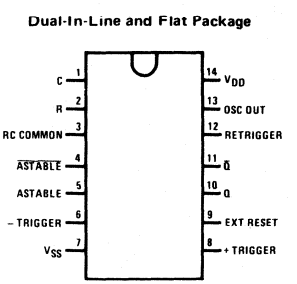
  typical frequency deviation = ±2% + 0.03%/°C @ 100 kHz
  = ±0.5% + 0.015%/°C @ 10 kHz
  (circuits trimmed to frequency V_{DD} = 10V ±10%)

applications

- Frequency discriminators
- Timing circuits
- Time-delay applications
- Envelope detection
- Frequency multiplication
- Frequency division

block and connection diagrams





absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4047BM	−55°C to +125°C
CD4047BC	−40°C to +85°C

dc electrical characteristics CD4047BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4047BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

dc electrical characteristics (Continued) CD4047BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

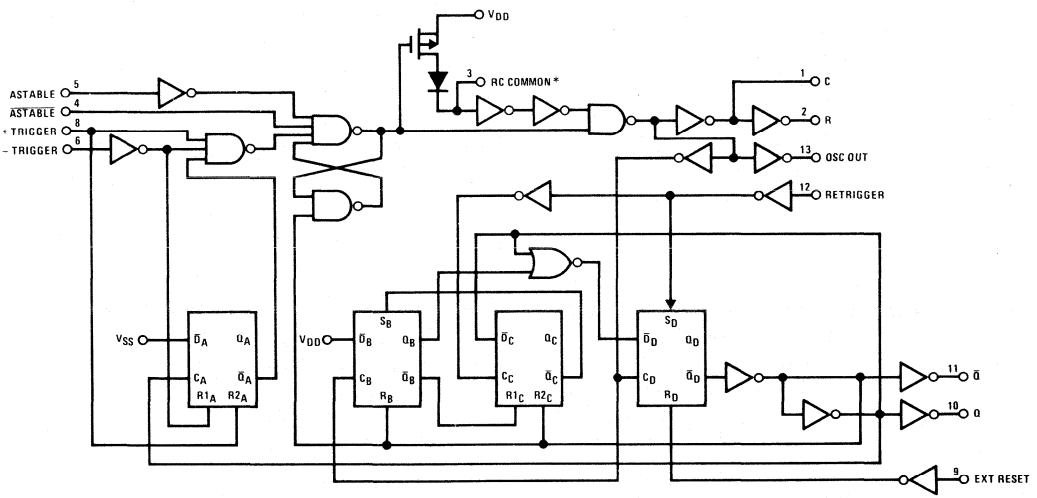
Note 2: $V_{SS} = 0V$ unless otherwise specified.

ac electrical characteristics CD4047B

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, Input $t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time Astable, $\overline{\text{Astable}}$ to Osc Out	$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	160	ns
t_{PHL}, t_{PLH}	Astable, $\overline{\text{Astable}}$ to Q, $\overline{Q}$	$V_{DD} = 5V$		550	900	ns
		$V_{DD} = 10V$		250	500	ns
		$V_{DD} = 15V$		200	400	ns
t_{PHL}, t_{PLH}	+ Trigger, − Trigger to Q, $\overline{Q}$	$V_{DD} = 5V$		700	1200	ns
		$V_{DD} = 10V$		300	600	ns
		$V_{DD} = 15V$		240	480	ns
t_{PHL}, t_{PLH}	+ Trigger, Retrigger to Q, $\overline{Q}$	$V_{DD} = 5V$		300	600	ns
		$V_{DD} = 10V$		175	300	ns
		$V_{DD} = 15V$		150	250	ns
t_{PHL}, t_{PLH}	Reset to Q, $\overline{Q}$	$V_{DD} = 5V$		300	600	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q, $\overline{Q}$, Osc Out	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Input Pulse Duration	Any Input				
		$V_{DD} = 5V$		500	1000	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{RCL}, t_{FCL}	+ Trigger, Retrigger, Rise and Fall Time	$V_{DD} = 5V$			15	μs
		$V_{DD} = 10V$			5	μs
		$V_{DD} = 15V$			5	μs
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF

logic diagram



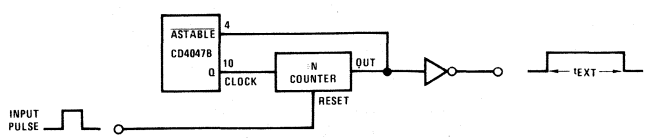
*Special input protection circuit to permit larger input-voltage swings

truth table

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	TYPICAL OUTPUT PERIOD OR PULSE WIDTH
	TO V_{DD}	TO V_{SS}	INPUT PULSE TO		
Astable Multivibrator					
Free-Running	4, 5, 6, 14	7, 8, 9, 12		10, 11, 13	$t_A(10, 11) = 4.40\ RC$
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A(13) = 2.20\ RC$
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
Monostable Multivibrator					
Positive-Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	
Negative-Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	$t_M(10, 11) = 2.48\ RC$
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown*	14	5, 6, 7, 8, 9, 12	(See Figure)	(See Figure)	(See Figure)

Note: External resistor between terminals 2 and 3. External capacitor between terminals 1 and 3.

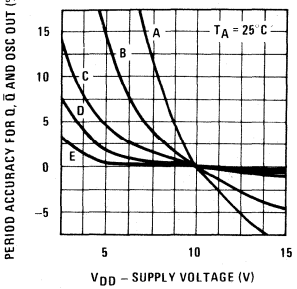
*** Typical Implementation of External Countdown Option**



$$t_{EXT} = (N - 1)\ t_A + (t_M + t_A/2)$$

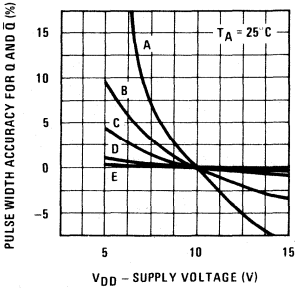
typical performance characteristics

Typical Q, $\overline{Q}$, Osc Out Period Accuracy vs Supply Voltage (Astable Mode Operation)



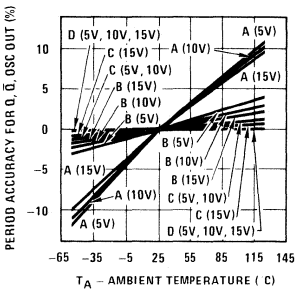
	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF
E	100 Hz	2.2M	1000 pF

Typical Q, $\overline{Q}$, Pulse Width Accuracy vs Supply Voltage Monostable Mode Operation



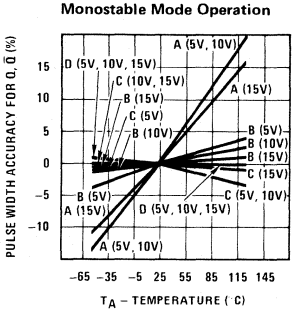
	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF
E	5.5 ms	2.2M	1000 pF

Typical Q, $\overline{Q}$ and Osc Out Period Accuracy vs Temperature Astable Mode Operation



	$f_{Q, \overline{Q}}$	R	C
A	1000 kHz	22k	10 pF
B	100 kHz	22k	100 pF
C	10 kHz	220k	100 pF
D	1 kHz	220k	1000 pF

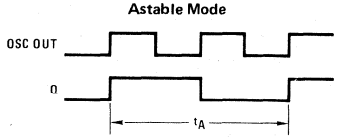
Typical Q and $\overline{Q}$ Pulse Width Accuracy vs Temperature Monostable Mode Operation



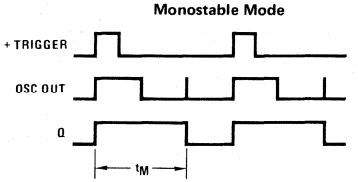
	t_M	R	C
A	2 μs	22k	10 pF
B	7 μs	22k	100 pF
C	60 μs	220k	100 pF
D	550 μs	220k	1000 pF

timing diagrams

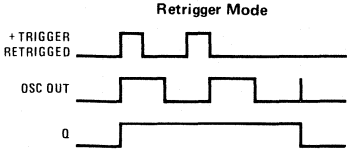
Astable Mode



Monostable Mode



Retrigger Mode



National Semiconductor

CD4048BM/CD4048BC TRI-STATE® Expandable 8-Function 8-Input Gate

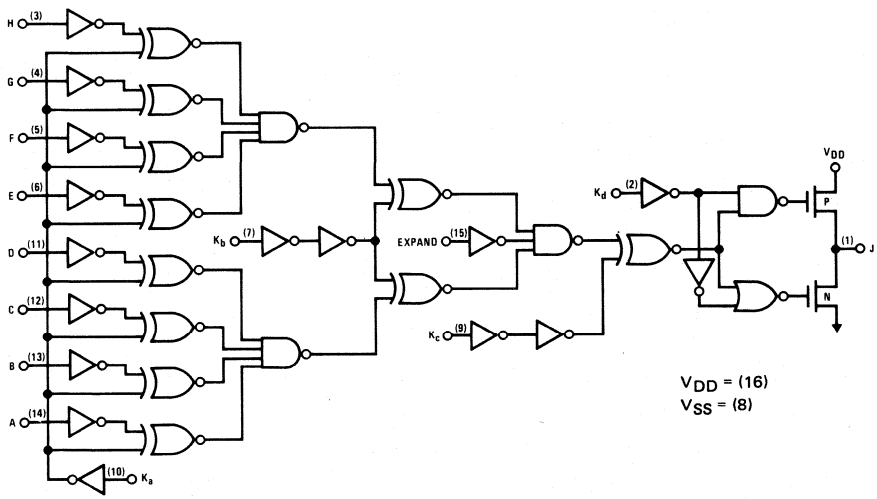
general description

The CD4048BM/CD4048BC is a programmable 8-input gate. Three binary control lines K_a, K_b and K_c determine the 8 different logic functions of the gate. These functions are OR, NOR, AND, NAND, OR/AND, OR/NAND, AND/OR and AND/NOR. A fourth input, K_d, is a TRI-STATE control. When K_d is high, the output is enabled; when K_d is low, the output is a high impedance. This feature enables the user to connect the device to a common bus line. The Expand input permits the user to increase the number of gate inputs. For example, two 8-input CD4048's can be cascaded into a 16-input multifunction gate. When the Expand input is not used, it should be connected to V_{SS}. All inputs are buffered and protected against electrostatic effects.

features

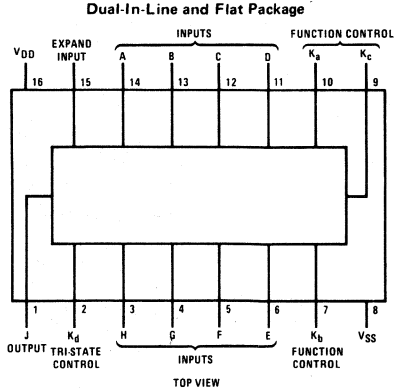
- Wide supply voltage range 3V to 15V
- High noise immunity 0.45 V_{DD} typ
- High sink and source current capability
- TTL compatibility—drives 1 standard TTL load at V_{CC} = 5V, over full temperature range
- Many logic functions in one package

logic diagram



connection diagram

Dual-In-Line and Flat Package



absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4048BM	−55°C to +125°C
CD4048BC	−40°C to +85°C

dc electrical characteristics CD4048BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.01	5.0		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	2.8		2.3	4.0		1.6		mA
		V_{DD} = 10V, V_O = 0.5V	6.4		5.2	11		3.6		mA
		V_{DD} = 15V, V_O = 1.5V	14		11.5	23		8.0		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−2.8		−2.3	−4.0		−1.6		mA
		V_{DD} = 10V, V_O = 9.5V	−6.4		−5.2	−11		−3.6		mA
		V_{DD} = 15V, V_O = 13.5V	−14		−11.5	−23		−8.0		mA
I_{OZ}	TRI-STATE Leakage Current	V_{DD} = 15V, V_O = 0V		−0.2		−0.002	−0.2		−2	μA
		V_{DD} = 15V, V_O = 15V		0.2		0.002	0.2		2	μA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4048BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V

dc electrical characteristics (Continued) CD4048BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V$	9.95		9.95	10		9.95		V
		$V_{DD} = 15V$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	2.3		2.0	4.0			1.6	mA
		$V_{DD} = 10V$, $V_O = 0.5V$	5.2		4.5	11			3.6	mA
		$V_{DD} = 15V$, $V_O = 1.5V$	11.5		9.8	23			8.0	mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−2.3		−2.0	−4.0			−1.6	mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−5.2		−4.5	−11			−3.6	mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−11.5		−9.8	−23			−8.0	mA
I_{TL}	TRI-STATE Leakage Current	$V_{DD} = 15V$, $V_O = 0V$		−0.6		−0.005	−0.6		−2	μA
		$V_{DD} = 15V$, $V_O = 15V$		0.6		0.005	0.6		2	μA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k\Omega$, and $t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	$V_{DD} = 5V$		425	850	ns
		$V_{DD} = 10V$		200	400	ns
		$V_{DD} = 15V$		160	320	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, K_d to High Impedance (From Active Low or High Level)	$R_L = 1.0k\Omega$				
		$V_{DD} = 5V$		175	350	ns
		$V_{DD} = 10V$		125	250	ns
		$V_{DD} = 15V$		100	200	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, K_d to Active High or Low Level (From High Impedance)	$R_L = 1.0k\Omega$				
		$V_{DD} = 5V$		225	450	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		70	140	ns
t_{THL}, t_{TLH}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{OUT}	Tristate output Capacitance				22.5	pF

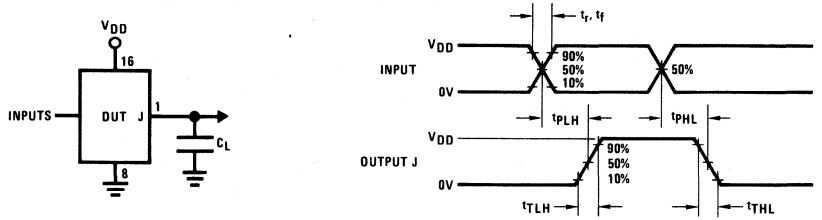
truth table

OUTPUT FUNCTION	BOOLEAN EXPRESSION	CONTROL INPUTS K_a	K_b	K_c	K_d	UNUSED INPUTS
NOR	$J = \overline{A+B+C+D+E+F+G+H}$	0	0	0	1	V_{SS}
OR	$J = A+B+C+D+E+F+G+H$	0	0	1	1	V_{SS}
OR/AND	$J = (A+B+C+D)\cdot(E+F+G+H)$	0	1	0	1	V_{SS}
OR/NAND	$J = \overline{(A+B+C+D)\cdot(E+F+G+H)}$	0	1	1	1	V_{SS}
AND	$J = A\cdot B\cdot C\cdot D\cdot E\cdot F\cdot G\cdot H$	1	0	0	1	V_{DD}
NAND	$J = \overline{A\cdot B\cdot C\cdot D\cdot E\cdot F\cdot G\cdot H}$	1	0	1	1	V_{DD}
AND/NOR	$J = \overline{(A\cdot B\cdot C\cdot D)+(E\cdot F\cdot G\cdot H)}$	1	1	0	1	V_{DD}
AND/OR	$J = (A\cdot B\cdot C\cdot D)+(E\cdot F\cdot G\cdot H)$	1	1	1	1	V_{DD}
Hi-Z		X	X	X	0	X

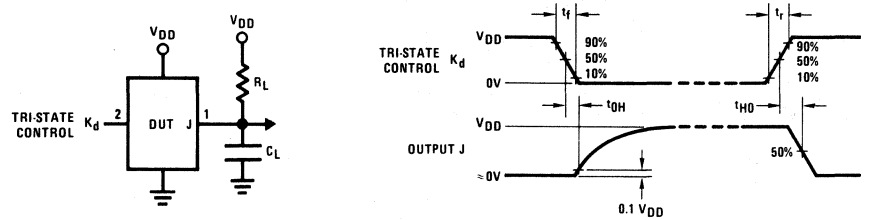
Positive logic: 0 = low level, 1 = high level, X = irrelevant, EXPAND input tied to V_{SS}.

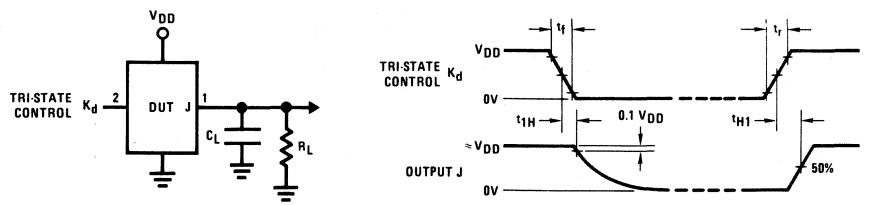
ac test circuits and switching time waveforms

Logic Propagation Delay Time Tests



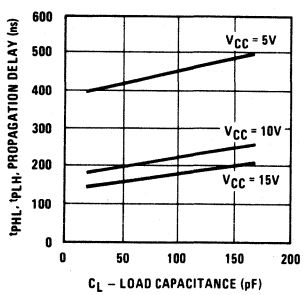
TRI-STATE Propagation Delay Time Tests



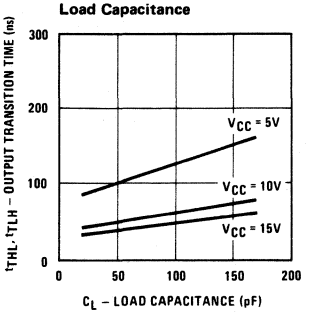


typical performance characteristics

Propagation Delay vs Load Capactiance

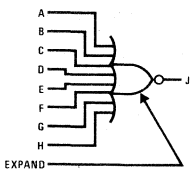


Output Transition Time vs Load Capacitance



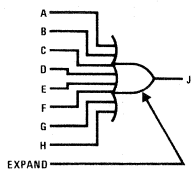
basic logic configurations

NOR



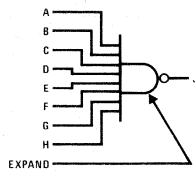
$K_aK_bK_c = 000$

OR



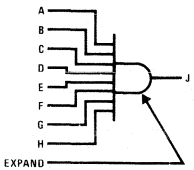
= 001

NAND



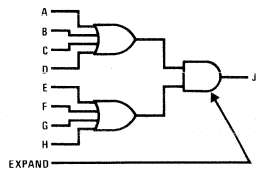
= 101

AND



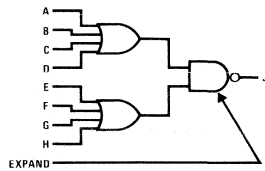
= 100

OR/AND



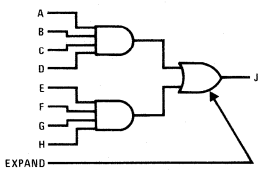
= 010

OR/NAND



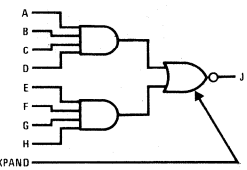
= 011

AND/OR



= 111

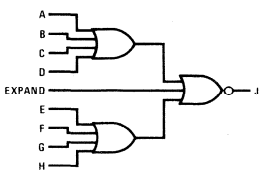
AND/NOR



= 110

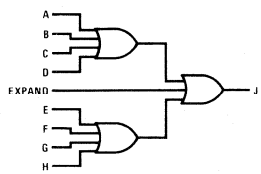
actual circuit configurations

NOR



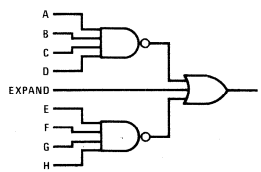
$K_aK_bK_c = 000$

OR



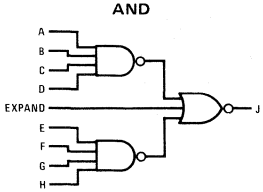
= 001

NAND



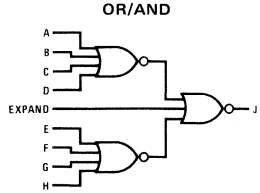
= 101

AND



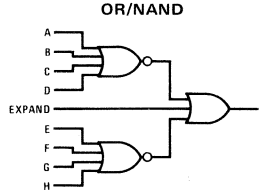
= 100

OR/AND



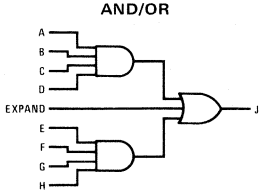
= 010

OR/NAND



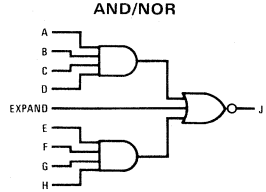
= 011

AND/OR



= 111

AND/NOR



= 110

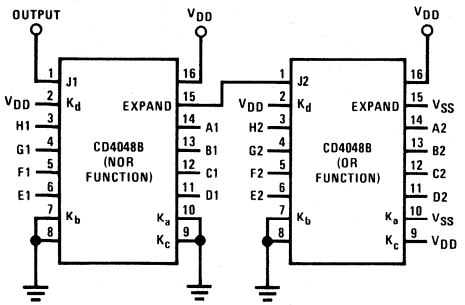
truth table for EXPAND feature

COMBINED OUTPUT FUNCTION	FUNCTION NEEDED AT EXPAND INPUT	OUTPUT BOOLEAN EXPRESSION
NOR	OR	$J = \overline{(A + B + C + D + E + F + G + H) + (EXP)}$
OR	OR	$J = (A + B + C + D + E + F + G + H) + (EXP)$
AND	NAND	$J = (ABCDEFGH) \cdot \overline{(EXP)}$
NAND	NAND	$J = \overline{(ABCDEFGH) \cdot (EXP)}$
OR/AND	NOR	$J = (A + B + C + D) \cdot (E + F + G + H) \cdot \overline{(EXP)}$
OR/NAND	NOR	$J = \overline{(A + B + C + D) \cdot (E + F + G + H) \cdot (EXP)}$
AND/NOR	AND	$J = \overline{(ABCD) + (EFGH) + (EXP)}$
AND/OR	AND	$J = (ABCD) + (EFGH) + (EXP)$

Note. Positive logic is assumed. (EXP) represents the logic level present at the EXPAND input.

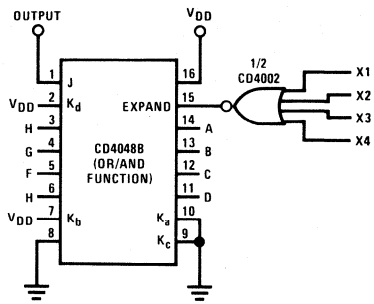
typical applications of EXPAND feature

16-Input NOR Gate



$$\text{Output} = \overline{A1 + B1 + C1 + D1 + E1 + F1 + G1 + H1 + A2 + B2 + C2 + D2 + E2 + F2 + G2 + H2}$$

12-Input OR/AND Gate



Output = (A + B + C + D) • (E + G + H) • (X1 + X2 + X3 + X4) F +

National Semiconductor

CD4049M/CD4049C Hex Inverting Buffer
CD4050BM/CD4050BC Hex Non-Inverting Buffer

general description

These hex buffers are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. These devices feature logic level conversion using only one supply voltage (V_{DD}). The input-signal high level (V_{IH}) can exceed the V_{DD} supply voltage when these devices are used for logic level conversions. These devices are intended for use as hex buffers, CMOS to DTL/TTL converters, or as CMOS current drivers, and at V_{DD} = 5V, they can drive directly two DTL/TTL loads over the full operating temperature range.

features

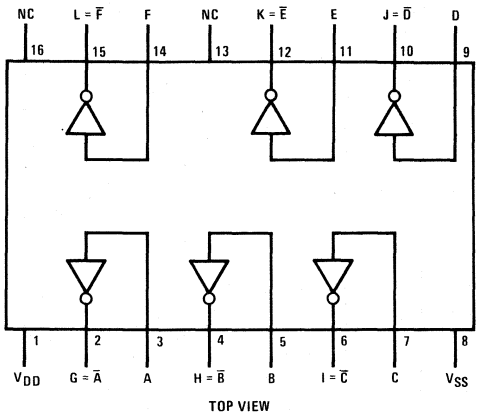
- Wide supply voltage range 3V to 15V
- Direct drive to 2 TTL loads at 5V over full temperature range
- High source and sink current capability
- Special input protection permits input voltages greater than V_{DD}

applications

- CMOS hex inverter/buffer
- CMOS to DTL/TTL hex converter
- CMOS current "sink" or "source" driver
- CMOS high-to-low logic level converter

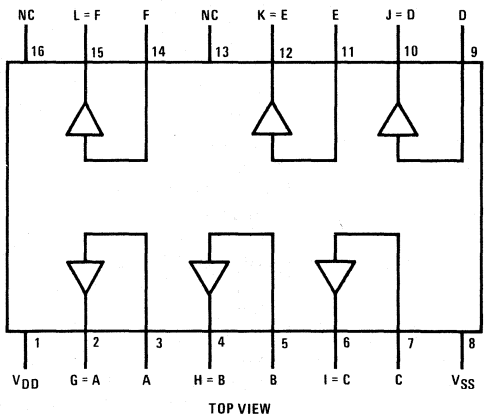
connection diagrams

CD4049M/CD4049C
Dual-In-Line and Flat Package



TOP VIEW

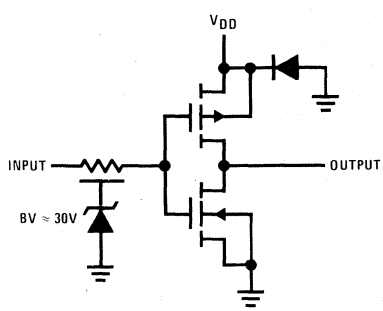
CD4050BM/CD4050BC
Dual-In-Line and Flat Package



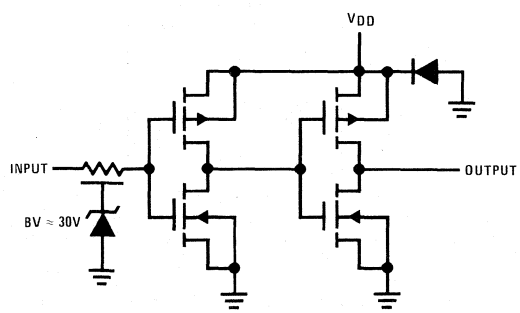
TOP VIEW

schematic diagrams

CD4049M/CD4049C
1 of 6 Identical Units



CD4050BM/CD4050BC
1 of 6 Identical Units



absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to +18V
V_{OUT} Voltage at Any Output Pin	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to 15V
V_{OUT} Voltage at Any Output Pin	0 to V_{DD}
T_A Operating Temperature Range	
CD4049M, CD4050BM	−55°C to +125°C
CD4049C, CD4050BC	−40°C to +85°C

dc electrical characteristics CD4049M, CD4050BM (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		30	μA
	V_{DD} = 10V		2.0		0.01	2.0		60	μA
	V_{DD} = 15V		4.0		0.03	4.0		120	μA
V_{OL} Low Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0, $\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{IH} = V_{DD}, V_{IL} = 0, $\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage (CD4050BM Only)	$\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL} Low Level Input Voltage (CD4049UBM Only)	$\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
	V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
	V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH} High Level Input Voltage (CD4050BM Only)	$\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH} High Level Input Voltage (CD4049UBM Only)	$\|I_O\| < 1\ \mu A$								
	V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
	V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
	V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL} Low Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
	V_{DD} = 5V, V_O = 0.4V	5.6		4.6	5		3.2		mA
	V_{DD} = 10V, V_O = 0.5V	12		9.8	12		6.8		mA
	V_{DD} = 15V, V_O = 1.5V	35		29	40		20		mA
I_{OH} High Level Output Current (Note 3)	V_{IH} = V_{DD}, V_{IL} = 0V								
	V_{DD} = 5V, V_O = 4.6V	−1.3		−1.1	−1.6		−0.72		mA
	V_{DD} = 10V, V_O = 9.5V	−2.6		−2.2	−3.6		−1.5		mA
	V_{DD} = 15V, V_O = 13.5V	−8.0		−7.2	−12		−5.0		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: These are *peak* output current capabilities. Continuous output current is rated at 12 mA maximum. The output current should not be allowed to exceed this value for extended periods of time.

dc electrical characteristics CD4049C, CD4050BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4		0.03	4.0		30	μA
		V_{DD} = 10V		8		0.05	8.0		60	μA
		V_{DD} = 15V		16		0.07	16.0		120	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IL}	Low Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.0		1.5	1.0		1.0	V
		V_{DD} = 10V, V_O = 9V		2.0		2.5	2.0		2.0	V
		V_{DD} = 15V, V_O = 13.5V		3.0		3.5	3.0		3.0	V
V_{IH}	High Level Input Voltage (CD4050BC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
V_{IH}	High Level Input Voltage (CD4049UBC Only)	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V	4.0		4.0	3.5		4.0		V
		V_{DD} = 10V, V_O = 1V	8.0		8.0	7.5		8.0		V
		V_{DD} = 15V, V_O = 1.5V	12.0		12.0	11.5		12.0		V
I_{OL}	Low Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	4.6		4.0	5		3.2		mA
		V_{DD} = 10V, V_O = 0.5V	9.8		8.5	12		6.8		mA
		V_{DD} = 15V, V_O = 1.5V	29		25	40		20		mA
I_{OH}	High Level Output Current (Note 3)	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−1.0		−0.9	−1.6		−0.72		mA
		V_{DD} = 10V, V_O = 9.5V	−2.1		−1.9	−3.6		−1.5		mA
		V_{DD} = 15V, V_O = 13.5V	−7.1		−6.2	−12		−5		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V	−0.3		−0.3	-10^{-5}			−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V	0.3		0.3	10^{-5}			1.0	μA

ac electrical characteristics CD4049M/CD4049C

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

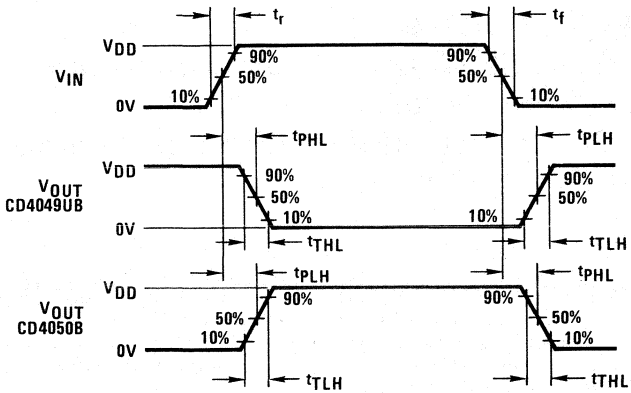
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		30	65	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		45	85	ns
		$V_{DD} = 10V$		25	45	ns
		$V_{DD} = 15V$		20	35	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		15	22.5	pF

ac electrical characteristics CD4050BM/CD4050BC

$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_r = t_f = 20$ ns, unless otherwise specified.

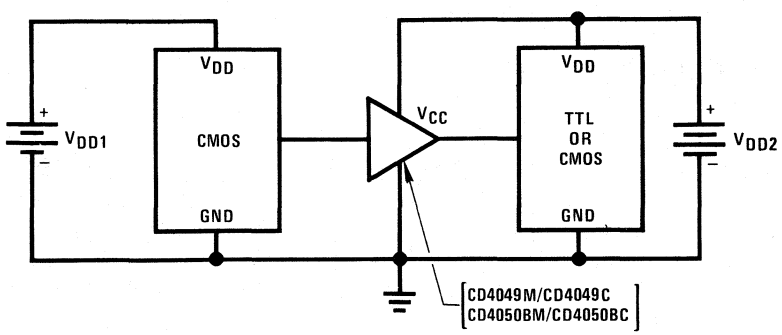
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time High-to-Low Level	$V_{DD} = 5V$		60	110	ns
		$V_{DD} = 10V$		25	55	ns
		$V_{DD} = 15V$		20	30	ns
t_{PLH}	Propagation Delay Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
t_{THL}	Transition Time High-to-Low Level	$V_{DD} = 5V$		30	60	ns
		$V_{DD} = 10V$		20	40	ns
		$V_{DD} = 15V$		15	30	ns
t_{TLH}	Transition Time Low-to-High Level	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		30	55	ns
		$V_{DD} = 15V$		25	45	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

switching time waveforms



typical application

CMOS to TTL or CMOS at a Lower V_{DD}



Note: $V_{DD1} \geq V_{DD2}$

Note: In the case of the CD4049M/CD4049C the output drive capability increases with increasing input voltage. E.g., If V_{DD1}= 10V the CD4049M/CD4049C could drive 4 TTL loads.

National Semiconductor

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

general description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to 15 Vp-p can be achieved by digital signal amplitudes of 3-15 V. For example, if V_{DD} = 5 V, V_{SS} = 0 V and V_{EE} = −5 V, analog signals from −5 V to +5 V can be controlled by digital inputs of 0-5 V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD} - V_{SS}$ and $V_{DD} - V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF."

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 of 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

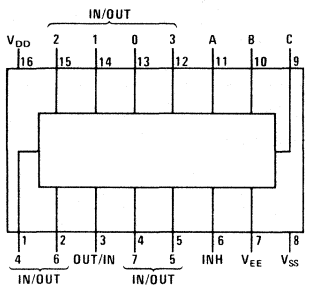
CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

features

- Wide range of digital and analog signal levels: digital 3-15 V, analog to 15 Vp-p
- Low "ON" resistance: 80 Ω (typ) over entire 15 Vp-p signal-input range for $V_{DD} - V_{EE}$ = 15 V
- High "OFF" resistance: channel leakage of ±10 pA (typ) at $V_{DD} - V_{EE}$ = 10 V
- Logic level conversion for digital addressing signals of 3-15 V ($V_{DD} - V_{SS}$ = 3-15 V) to switch analog signals to 15 Vp-p ($V_{DD} - V_{EE}$ = 15 V)
- Matched switch characteristics: ΔR_{ON} = 5 Ω (typ) for $V_{DD} - V_{EE}$ = 15 V
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ) at $V_{DD} - V_{SS} = V_{DD} - V_{EE}$ = 10 V
- Binary address decoding on chip

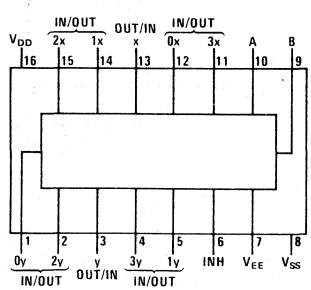
connection diagrams

CD4051BM/CD4051BC



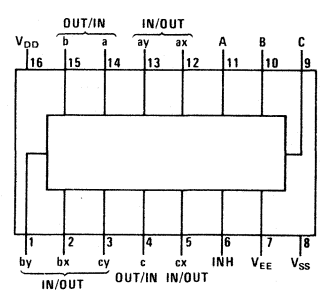
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

absolute maximum rating

V_{DD}	DC Supply Voltage	−0.5 Vdc to +18 Vdc
V_{IN}	Input Voltage	−0.5 Vdc to V_{DD} + 0.5 Vdc
T_S	Storage Temperature Range	−65°C to +150°C
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

recommended operating conditions

V_{DD}	DC Supply Voltage	+5 Vdc to +15 Vdc
V_{IN}	Input Voltage	0 V to V_{DD} Vdc
T_A	Operating Temperature Range	
	4051BM/4052BM/4053BM	−55°C to +125°C
	4051BC/4052BC/4053BC	−40°C to +85°C

dc electrical characteristics (Note 2)

	Parameter	Conditions		−55°C Min	−55°C Max	+25°C Min	+25°C Typ	+125°C Max	+125°C Min	+125°C Max	Units
I_{DD}	Quiescent Device Current	V_{DD} = 5 V			5			5		150	μA
		V_{DD} = 10 V			10			20		600	μA
		V_{DD} = 15 V			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5 V, V_{EE} = −2.5 V or V_{DD} = 5 V, V_{EE} = 0 V		2000		270	2500		3500	Ω
			V_{DD} = 5 V, V_{EE} = −5 V or V_{DD} = 10 V, V_{EE} = 0 V		310		120	400		580	Ω
			V_{DD} = 7.5 V, V_{EE} = −7.5 V or V_{DD} = 15 V, V_{EE} = 0 V		220		80	280		400	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5 V, V_{EE} = −2.5 V or V_{DD} = 5 V, V_{EE} = 0 V				10				Ω
			V_{DD} = 5 V, V_{EE} = −5 V or V_{DD} = 10 V, V_{EE} = 0 V				10				Ω
			V_{DD} = 7.5 V, V_{EE} = −7.5 V or V_{DD} = 15 V, V_{EE} = 0 V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5 V, V_{EE} = −7.5 V O/I = ±7.5 V, I/O = 0 V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5 V V_{DD} = 7.5 V, V_{EE} = −7.5 V, O/I = 0 V, I/O = ±7.5 V	CD4051		±200		±0.08	±200		±2000	nA
			CD4052		±200		±0.04	±200		±2000	nA
			CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1kΩ to V_{SS} I_{IS} < 2 μA on all OFF channels V_{IS} = V_{DD} thru 1kΩ									
		V_{DD} = 5 V			1.5			1.5		1.5	V
		V_{DD} = 10 V			3.0			3.0		3.0	V
		V_{DD} = 15 V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15 V, V_{EE} = 0 V V_{IN} = 0 V			-0.1		-10^{-5}	-0.1		-1.0	μA
		V_{DD} = 15 V, V_{EE} = 0 V V_{IN} = 15 V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

dc electrical characteristics (con't) (Note 2)

	Parameter	Conditions		−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+85°C Max	+85°C Min	+85°C Max	Units
I_{DD}	Quiescent Device Current	V_{DD} = 5V			20			20		150	μA
		V_{DD} = 10V			40			40		300	μA
		V_{DD} = 15V			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \leq V_{IS} \leq V_{DD}$)	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V		2100		270	2500		3200	Ω
			V_{DD} = 5V, V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V		330		120	400		520	Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V		230		80	280		360	Ω
ΔR_{ON}	Δ "ON" Resistance Between Any Two Channels	R_L = 10 kΩ (any channel selected)	V_{DD} = 2.5V, V_{EE} = −2.5V or V_{DD} = 5V, V_{EE} = 0V				10				Ω
			V_{DD} = 5V V_{EE} = −5V or V_{DD} = 10V, V_{EE} = 0V				10				Ω
			V_{DD} = 7.5V, V_{EE} = −7.5V or V_{DD} = 15V, V_{EE} = 0V				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	V_{DD} = 7.5V, V_{EE} = −7.5V O/I = ±7.5V, I/O = 0V			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V CD4051			±200		±0.08	±200		±2000	nA
		V_{DD} = 7.5V, V_{EE} = −7.5V, O/I = 0V	CD4052		±200		±0.04	±200		±2000	nA
		I/O = ±7.5V	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	V_{EE} = V_{SS} R_L = 1 kΩ to V_{SS} I_{IS} < 2μA on all OFF Channels V_{IS} = V_{DD} thru 1kΩ									
		V_{DD} = 5V			1.5			1.5		1.5	V
		V_{DD} = 10V			3.0			3.0		3.0	V
		V_{DD} = 15V			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5		3.5		3.5			3.5		V
		V_{DD} = 10		7		7			7		V
		V_{DD} = 15		11		11			11		V
I_{IN}	Input Current	V_{DD} = 15V, V_{EE} = 0V V_{IN} = 0V			−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{EE} = 0V V_{IN} = 15V			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings' are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

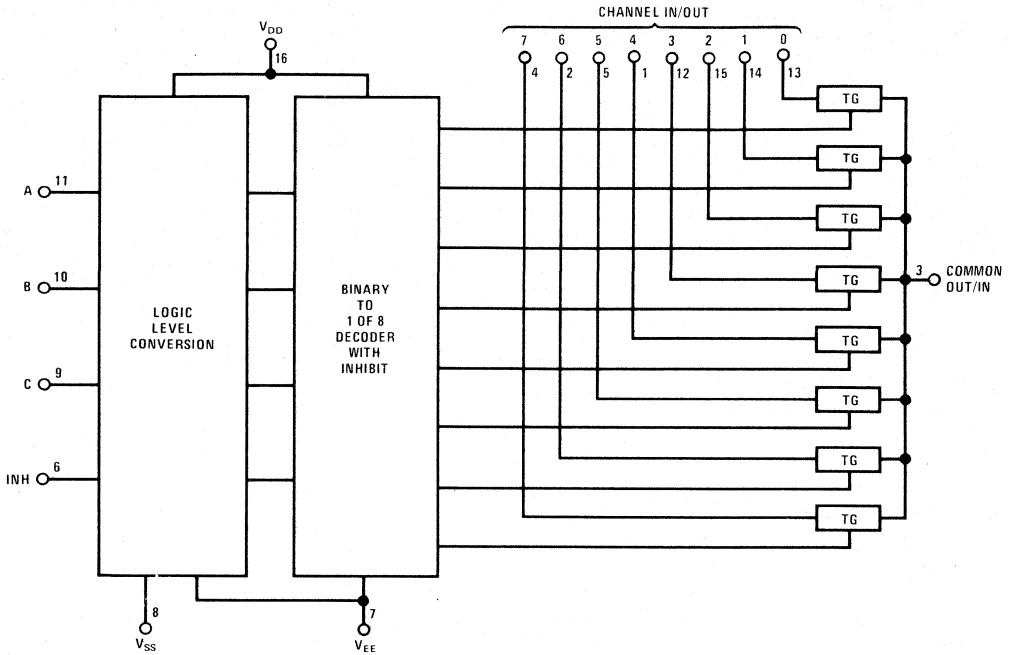
ac electrical characteristics

$T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

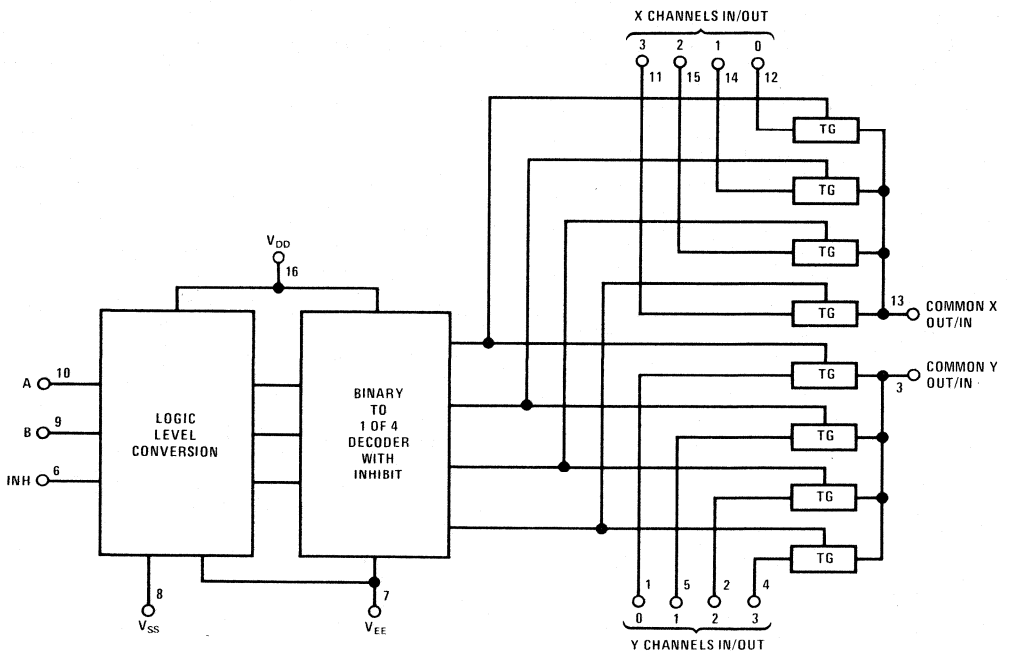
Parameter		Conditions	V_{pp}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0$ V $R_L = 1$ kΩ $C_L = 50$ pF	5 V 10 V 15 V		600 225 160	1200 450 320	ns ns ns
t_{PHZ} t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0$ V $R_L = 1$ kΩ $C_L = 50$ pF	5 V 10 V 15 V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance Control Input Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0$ V	10 V 10 V 10 V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10$ kΩ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0$ V	10 V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1$ kΩ, $V_{EE} = V_{SS} = 0$ V, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -3$ dB	10 V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1$ kΩ, $V_{EE} = V_{SS} = 0$ V, $V_{IS} = 5V_{p-p}$, $20\log_{10} V_{OS}/V_{IS} = -40$ dB	10 V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1$ kΩ, $V_{EE} = V_{SS} = 0$ V, $V_{IS}(A) = 5V_{p-p}$, $20\log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10 V		3		MHz
t_{PHL}, t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0$ V $C_L = 50$ pF	5 V 10 V 15 V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0$ V, $R_L = 10$ kΩ at both ends of channel. Input Square Wave Amplitude = 10 V	10 V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0$ V $C_L = 50$ pF	5 V 10 V 15 V		500 180 120	1000 360 240	ns ns ns

Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

block diagrams

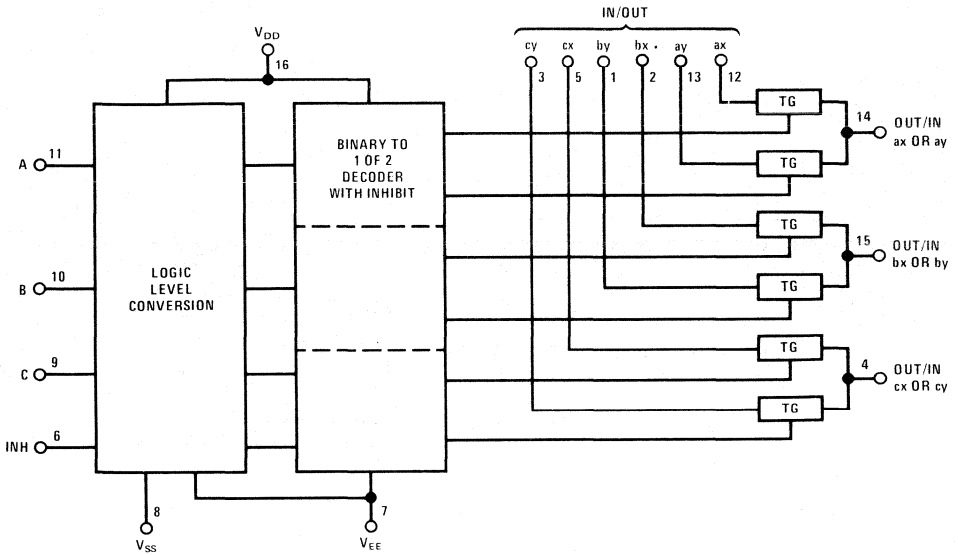


CD4051BM/CD4051BC



CD4052BM/CD4052BC

block diagram (cont)

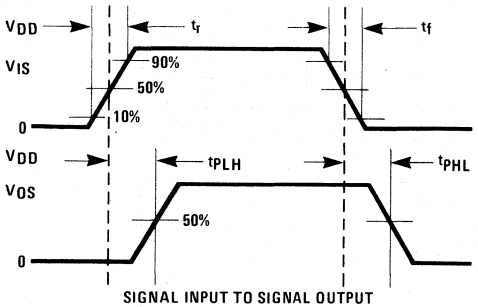


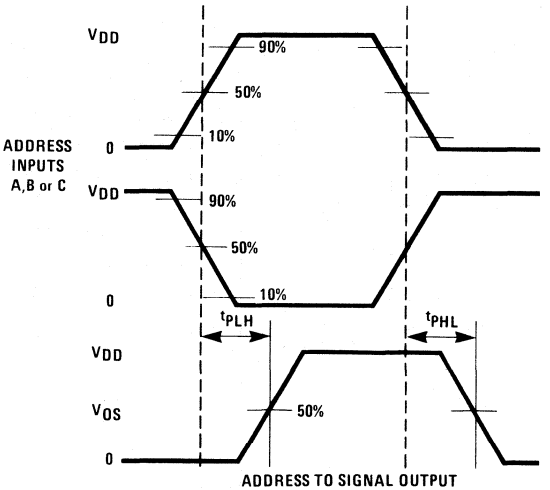
CD4053BM/CD4053BC

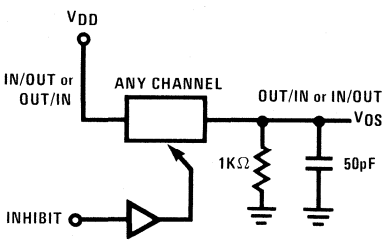
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

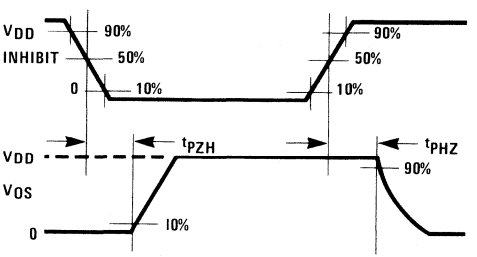
* Don't Care condition.

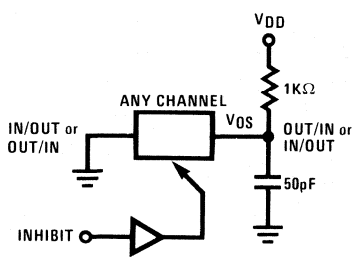
switching time waveforms

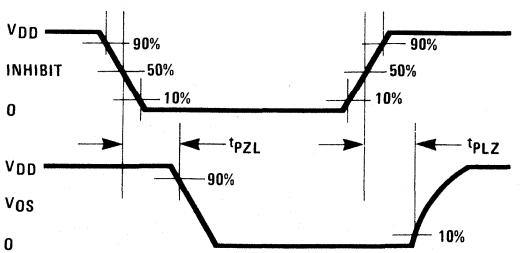










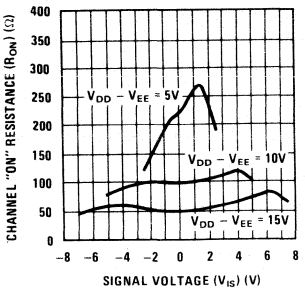


special considerations

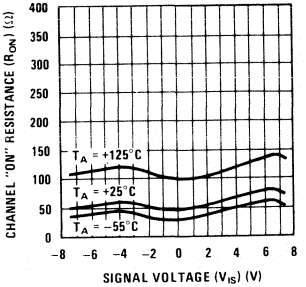
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6 V at $T_A \leq 25°C$, or 0.4 V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

typical performance characteristics

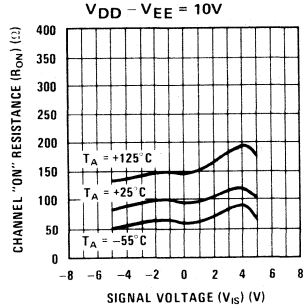
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



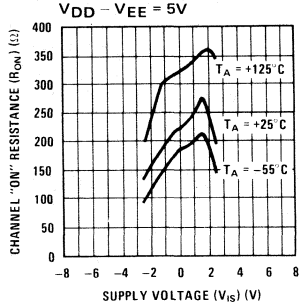
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



National Semiconductor

CD4066BM/CD4066BC Quad Bilateral Switch

general description

The CD4066BM/CD4066BC is a quad bilateral switch intended for the transmission or multiplexing of analog or digital signals. It is pin-for-pin compatible with CD4016BM/CD4016BC, but has a much lower "ON" resistance, and "ON" resistance is relatively constant over the input-signal range.

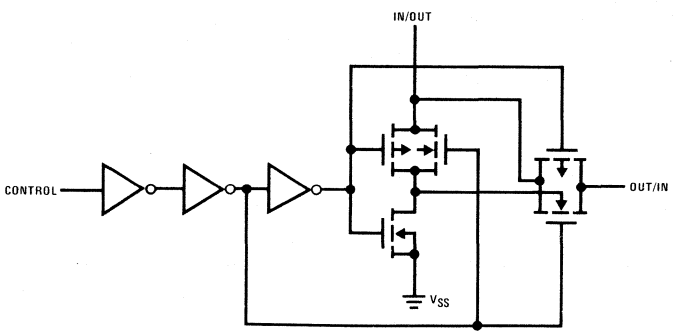
features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Wide range of digital and analog switching — ±7.5 V_{PEAK}
- "ON" resistance for 15V operation — 80Ω typ
- Matched "ON" resistance over 15V signal input — ΔR_{ON} = 5Ω typ
- "ON" resistance flat over peak-to-peak signal range
- High "ON"/"OFF" output voltage ratio — 65 dB typ @ f_{is} = 10 kHz, R_L = 10 kΩ
- High degree of linearity — < 0.4% distortion typ @ f_{is} = 1 kHz, V_{is} = 5 Vp-p, $V_{DD} - V_{SS}$ = 10V, R_L = 10 kΩ
- Extremely low "OFF" switch leakage — 0.1 nA typ @ $V_{DD} - V_{SS}$ = 10V, T_A = 25°C
- Extremely high control input impedance — 10^{12}Ω typ
- Low crosstalk between switches — −50 dB typ @ f_{is} = 0.9 MHz, R_L = 1 kΩ
- Frequency response, switch "ON" — 40 MHz typ

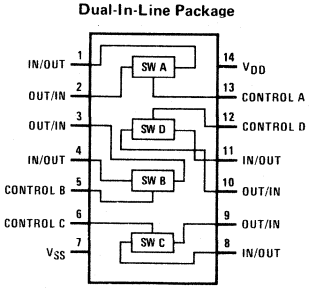
applications

- Analog signal switching/multiplexing
  - Signal gating
  - Squelch control
  - Chopper
  - Modulator/Demodulator
  - Commutating switch
- Digital signal switching/multiplexing
- CMOS logic implementation
- Analog-to-digital/digital-to-analog conversion
- Digital control of frequency, impedance, phase, and analog-signal gain

schematic and connection diagrams



Dual-In-Line Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4066BM	−55°C to +125°C
CD4066BC	−40°C to +85°C

dc electrical characteristics CD4066BM (Note 2)

Parameter		Conditions	−55°C		25°C			125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.01	0.25		7.5	μA
		V_{DD} = 10V		0.5		0.01	0.5		15	μA
		V_{DD} = 15V		1.0		0.01	1.0		30	μA
Signal Inputs and Outputs										
R_{ON}	"ON" Resistance	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
		V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
		V_{DD} = 5V		2000		270	2500		3500	Ω
		V_{DD} = 10V		400		120	500		550	Ω
		V_{DD} = 15V		220		80	280		320	Ω
ΔR_{ON}	Δ "ON" Resistance Between any 2 of 4 Switches	R_L = 10 kΩ to $\frac{V_{DD}-V_{SS}}{2}$								
		V_C = V_{DD}, V_{IS} = V_{SS} to V_{DD}								
		V_{DD} = 10V				10				Ω
		V_{DD} = 15V				5				Ω
I_{IS}	Input or Output Leakage Switch "OFF"	V_C = 0		±50		±0.1	±50		±500	nA
		V_{IS} = 15V and 0V,								
		V_{OS} = 0V and 15V								
Control Inputs										
V_{ILC}	Low Level Input Voltage	V_{IS} = V_{SS} and V_{DD}								
		V_{OS} = V_{DD} and V_{SS}								
		I_{IS} = ±10μA								
		V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IHC}	High Level Input Voltage	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V (see note 6)	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} − V_{SS} = 15V		±0.1		$\pm 10^{-5}$	±0.1		±1.0	μA
		$V_{DD} \geq V_{IS} \geq V_{SS}$								
		$V_{DD} \geq V_C \geq V_{SS}$								

dc electrical characteristics CD4066BC (Note 2)

Parameter		Conditions	−40°C		25°C			85°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.01	1.0		7.5	μA
		V_{DD} = 10V		2.0		0.01	2.0		15	μA
		V_{DD} = 15V		4.0		0.01	4.0		30	μA

dc electrical characteristics (Continued) CD4066BC (Note 2)

Parameter	Conditions	−40°C		25°C			85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
Signal Inputs and Outputs									
R_{ON} "ON" Resistance	$R_L = 10\ k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_C = V_{DD}$, V_{SS} to V_{DD}								
	$V_{DD} = 5V$		2000		270	2500		3200	Ω
	$V_{DD} = 10V$		450		120	500		520	Ω
	$V_{DD} = 15V$		250		80	280		300	Ω
ΔR_{ON} Δ"ON" Resistance Between Any 2 of 4 Switches	$R_L = 10\ k\Omega$ to $\frac{V_{DD} - V_{SS}}{2}$ $V_{CC} = V_{DD}$, $V_{IS} = V_{SS}$ to V_{DD}								
	$V_{DD} = 10V$				10				Ω
	$V_{DD} = 15V$				5				Ω
I_{IS} Input or Output Leakage Switch "OFF"	$V_C = 0$		±50		±0.1	±50		±200	nA
Control Inputs									
V_{ILC} Low Level Input Voltage	$V_{IS} = V_{SS}$ and V_{DD} $V_{OS} = V_{DD}$ and V_{SS} $I_{IS} = \pm 10\mu A$								
	$V_{DD} = 5V$		1.5		2.25	1.5		1.5	V
	$V_{DD} = 10V$		3.0		4.5	3.0		3.0	V
	$V_{DD} = 15V$		4.0		6.75	4.0		4.0	V
V_{IHC} High Level Input Voltage	$V_{DD} = 5V$	3.5		3.5	2.75		3.5		V
	$V_{DD} = 10V$ (See note 6)	7.0		7.0	5.5		7.0		V
	$V_{DD} = 15V$	11.0		11.0	8.25		11.0		V
I_{IN} Input Current	$V_{DD} - V_{SS} = 15V$ $V_{DD} \geq V_{IS} \geq V_{SS}$ $V_{DD} \geq V_C \geq V_{SS}$		±0.3		$\pm 10^{-5}$	±0.3		±1.0	μA

ac electrical characteristics $T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time Signal Input to Signal Output	$V_C = V_{DD}$, $C_L = 50$ pF, *(Figure 1)* $R_L = 200k$				
		$V_{DD} = 5V$		25	55	ns
		$V_{DD} = 10V$		15	35	ns
		$V_{DD} = 15V$		10	25	ns
t_{PZH}, t_{PZL}	Propagation Delay Time Control Input to Signal Output High Impedance to Logical Level	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time Control Input to Signal Output Logical Level to High Impedance	$R_L = 1.0\ k\Omega$, $C_L = 50$ pF, *(Figures 2 and 3)*				
		$V_{DD} = 5V$			125	ns
		$V_{DD} = 10V$			60	ns
		$V_{DD} = 15V$			50	ns
	Sine Wave Distortion	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$ $R_L = 10\ k\Omega$, $V_{IS} = 5\ V_{p-p}$, f = 1 kHz, *(Figure 4)*		0.4		%
	Frequency Response–Switch "ON" (Frequency at −3 dB)	$V_C = V_{DD} = 5V$, $V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$, 20 Log_{10} V_{OS}/V_{OS}(1kHz)−dB, *(Figure 4)*		40		MHz

ac electrical characteristics (Continued)

$T_A = 25°C$, $t_r = t_f = 20$ ns and $V_{SS} = 0V$ unless otherwise specified

	Parameter	Conditions	Min	Typ	Max	Units
	Feedthrough – Switch "OFF" (Frequency at –50 dB)	$V_{DD} = 5V$, $V_C = V_{SS} = -5V$, $R_L = 1\ k\Omega$, $V_{IS} = 5V_{p-p}$, 20 Log_{10}, $V_{OS}/V_{IS} = -50$ dB, *(Figure 4)*		1.25		
	Crosstalk Between Any Two Switch (Frequency at –50 dB)	$V_{DD} = V_{C(1)} = 5V$; $V_{SS} = V_{C(2)} = -5V$, $R_L = 1\ k\Omega$, $V_{IS(A)} = 5V_{p-p}$, 20 Log_{10} $V_{OS(2)}/V_{IS(1)} = -50$ dB, *(Figure 5)*		0.9		MHz
	Crosstalk; Control Input to Signal Output	$V_{DD} = 10V$, $R_L = 10\ k\Omega$ $R_{IN} = 1\ k\Omega$, $V_{CC} = 10V$ Square Wave, $C_L = 50$pF *(Figure 6)*		150		mV_{p-p}
	Maximum Control Input	$R_L = 1\ k\Omega$, $C_L = 50$ pF, *(Figure 7)* $V_{OS(f)} = \frac{1}{2}V_{OS(1kHz)}$				
		$V_{DD} = 5V$		6.0		MHz
		$V_{DD} = 10V$		8.0		MHz
		$V_{DD} = 15V$		8.5		MHz
C_{is}	Signal Input Capacitance			8		pF
C_{OS}	Signal Output Capacitance	$V_{DD} = 10V$		8		pF
C_{ios}	Feedthrough Capacitance	$V_C = 0V$		0.5		pF
C_{IN}	Control Input Capacitance			5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: These devices should not be connected to circuits with the power "ON".

Note 4: In all cases, there is approximately 5 pF of probe and jig capacitance on the output; however, this capacitance is included in C_L wherever it is specified.

Note 5: V_{IS} is the voltage at the in/out pin and V_{OS} is the voltage at the out/in pin. V_C is the voltage at the control input.

Note 6: Conditions for V_{IHC}:
a) $V_{IS} = V_{DD}$, I_{OS} = standard B series I_{OH} b) $V_{IS} = 0V$, I_{OS} = standard B series I_{OL}

ac test circuits and switching time waveforms

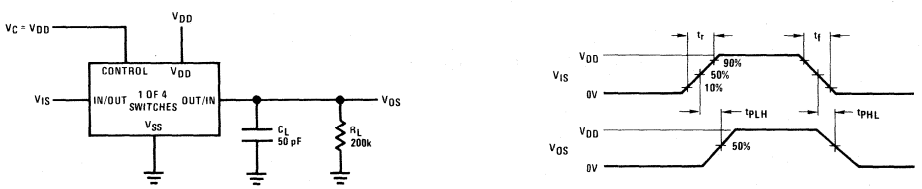


FIGURE 1. t_{PHL}, t_{PLH} Propagation Delay Time Signal Input to Signal Output

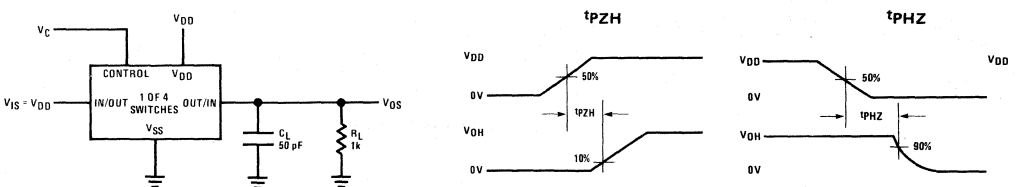


FIGURE 2. t_{PZH}, t_{PHZ} Propagation Delay Time Control to Signal Output

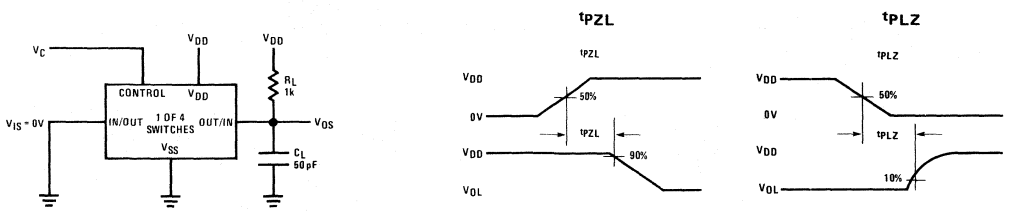


FIGURE 3. t_{PZL}, t_{PLZ} Propagation Delay Time Control to Signal Output

ac test circuits and switching time waveforms (Continued)

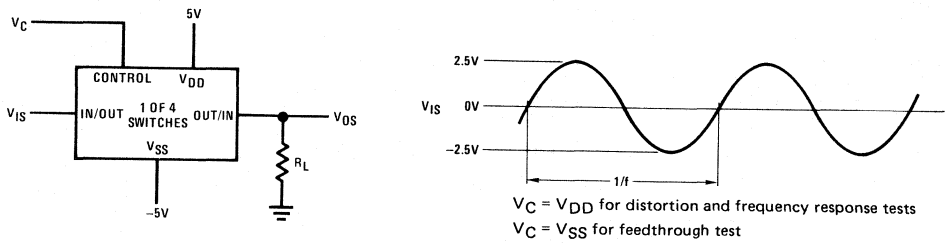


FIGURE 4. Sine Wave Distortion, Frequency Response and Feedthrough

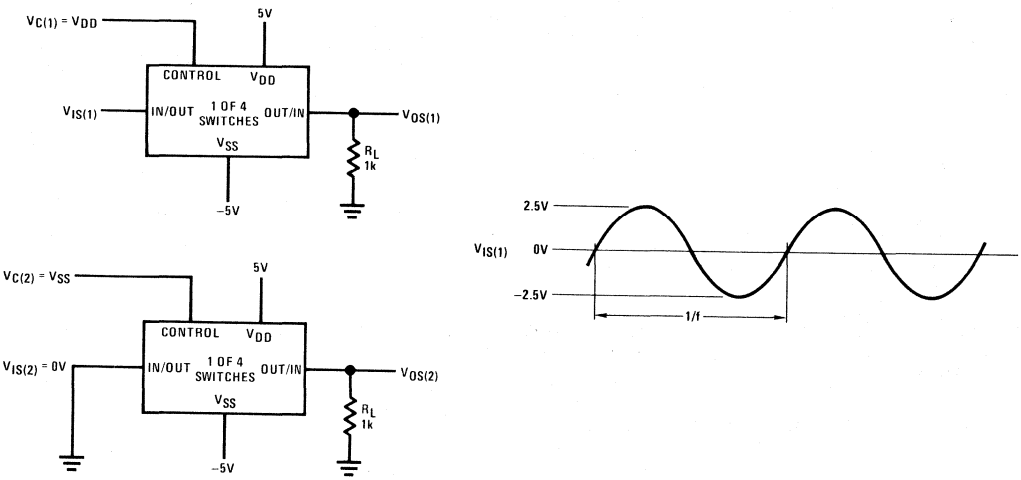


FIGURE 5. Crosstalk Between Any Two Switches

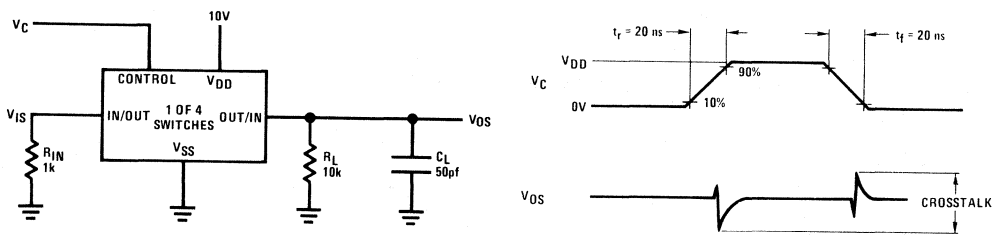


FIGURE 6. Crosstalk: Control Input to Signal Output

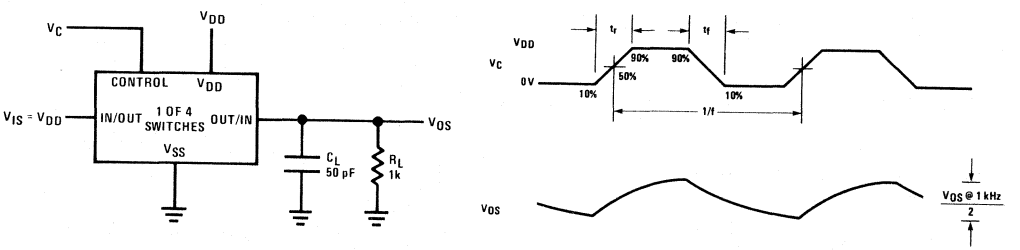
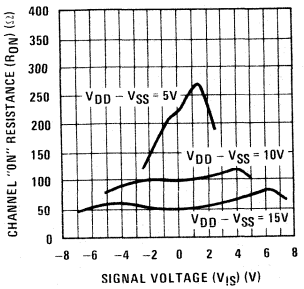


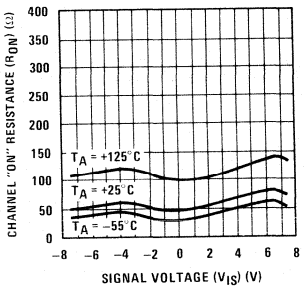
FIGURE 7. Maximum Control Input Frequency

typical performance characteristics

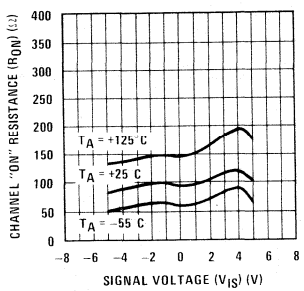
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



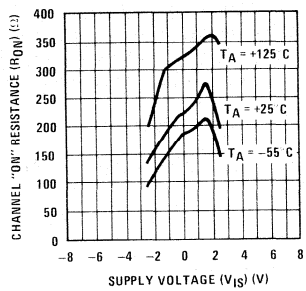
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{SS} = 5V$



special considerations

In applications where separate power sources are used to drive V_{DD} and the signal input, the V_{DD} current capability should exceed V_{DD}/R_L (R_L = effective external load of the 4 CD4066BM/CD4066BC bilateral switches). This provision avoids any permanent current flow or clamp action on the V_{DD} supply when power is applied or removed from CD4066BM/CD4066BC.

In certain applications, the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into terminals 1, 4, 8 or 11, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown).

No V_{DD} current will flow through R_L if the switch current flows into terminals 2, 3, 9 or 10.

National Semiconductor

CD4069M/CD4069C Inverter Circuits

general description

The CD4069B consists of six inverter circuits and is manufactured using complementary MOS (CMOS) to achieve wide power supply operating range, low power consumption, high noise immunity and symmetric controlled rise and fall times.

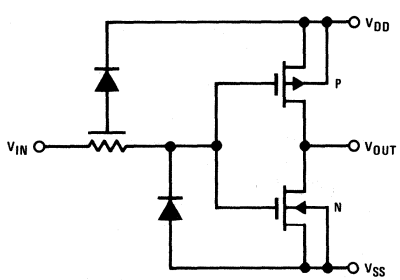
This device is intended for all general purpose inverter applications where the special characteristics of the MM74C901, MM74C903, MM74C907 and CD4049A Hex Inverter/Buffers are not required. In those applications requiring larger noise immunity the MM74C14 or MM74C914 Hex Schmitt Trigger is suggested.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

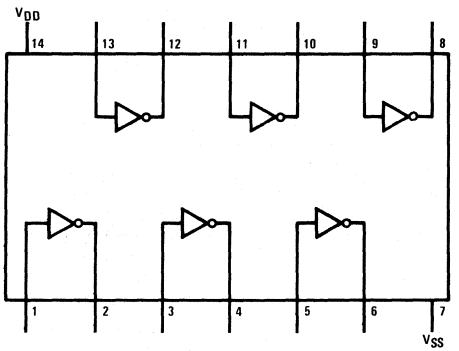
features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power — fan out of 2
  TTL compatibility — driving 74L or 1 driving 74LS
- Equivalent to MM54C04/MM74C04

schematic and connection diagrams

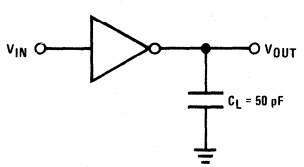


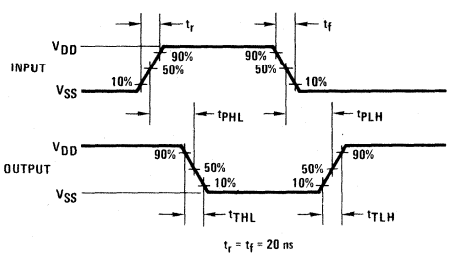
Dual-In-Line Package



TOP VIEW

ac test circuit and switching time waveforms





$t_r = t_f = 20$ ns

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4069M	−55°C to +125°C
CD4069C	−40°C to +85°C

dc electrical characteristics

CD4069M (Note 2)

PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
		MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD} Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
	V_{DD} = 10V		0.5			0.5		15	μA
	V_{DD} = 15V		1.0			1.0		30	μA
V_{OL} Low Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
	V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH} High Level Input Voltage	$\|I_O\| < 1\mu A$								
	V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
	V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
	V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
	V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
	V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

dc electrical characteristics CD4069C (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15	μA
		V_{DD} = 15V		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		8.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200kΩ, t_r and $t_f \leq$ 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		50	90	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		80	150	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Gate		6	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 3)		12		pF

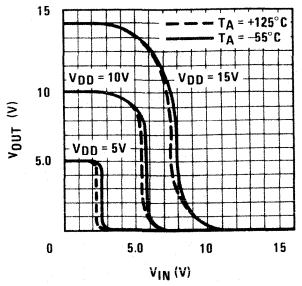
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

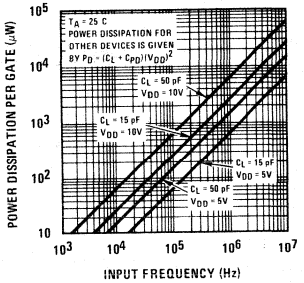
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

typical performance characteristics

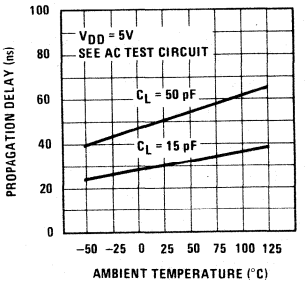
Gate Transfer Characteristics



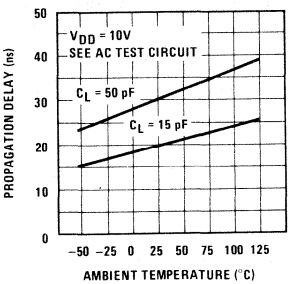
Power Dissipation vs Frequency



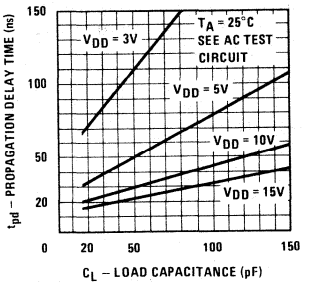
Propagation Delay vs Ambient Temperature



Propagation Delay vs Ambient Temperature



Propagation Delay Time vs Load Capacitance



National Semiconductor

CD4070BM/CD4070BC Quad 2-Input EXCLUSIVE-OR Gate

general description

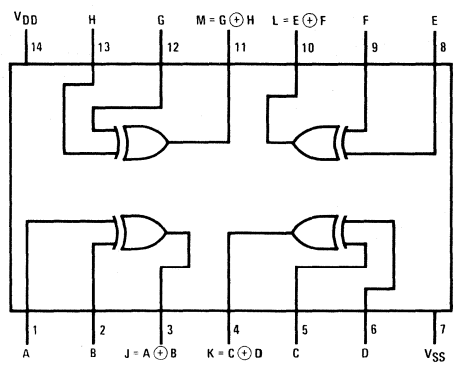
Employing complementary MOS (CMOS) transistors to achieve wide power supply operating range, low power consumption and high noise margin this gate provides basic functions used in the implementation of digital integrated circuit systems. The N and P-channel enhancement mode transistors provide a symmetrical circuit with output swing essentially equal to the supply voltage. No dc power other than that caused by leakage current is consumed during static condition. All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Pin compatible to CD4030A
- Equivalent to MM54C86/MM74C86 and MC14507B

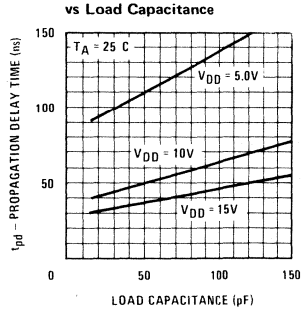
connection diagram

Dual-In-Line Package



typical performance characteristics

Propagation Delay Time vs Load Capacitance



truth table

INPUTS		OUTPUTS
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

absolute maximum ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4070BC	−40°C to +85°C
CD4070BM	−55°C to +125°C

dc electrical characteristics CD4070BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15	μA
		V_{DD} = 15V		1.0			1.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4070BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15	μA
		V_{DD} = 15V		4.0			4.0		30	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and $t_f \leq$ 20 ns, unless otherwise specified.

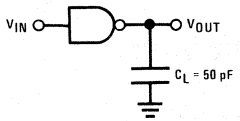
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		110	185	ns
		V_{DD} = 10V		50	90	ns
		V_{DD} = 15V		40	75	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Input (Note 3)		20		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

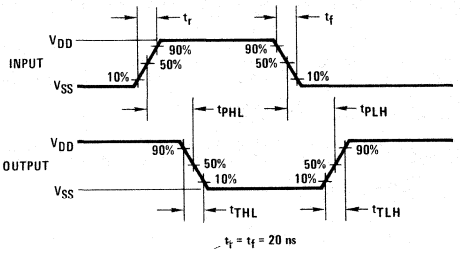
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

ac test circuit and switching time waveforms



Note: Delays measured with input t_r, t_f = 20 ns.



National Semiconductor

CD4071BM/CD4071BC Quad 2-Input OR Buffered B Series Gate
CD4081BM/CD4081BC Quad 2-Input AND Buffered B Series Gate

general description

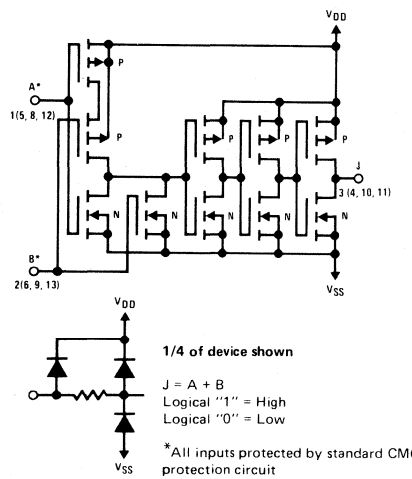
These quad gates are monoiithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain.

All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

features

- Low power TTL compatability, fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range

schematic and connection diagrams

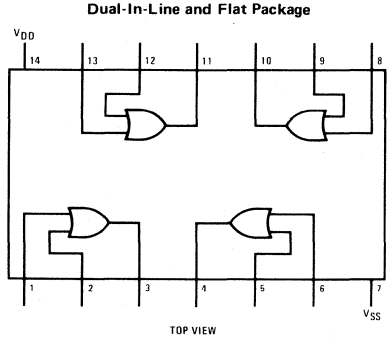


1/4 of device shown

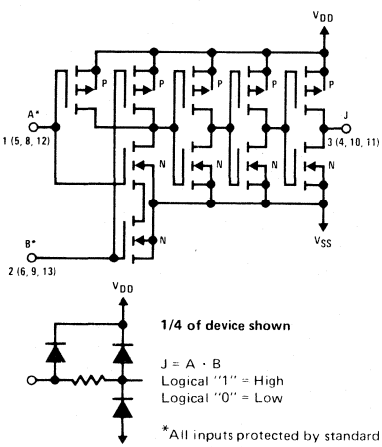
J = A + B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit

CD4071B
Dual-In-Line and Flat Package



TOP VIEW

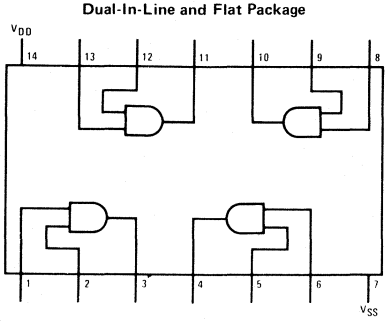


1/4 of device shown

J = A · B
Logical "1" = High
Logical "0" = Low

*All inputs protected by standard CMOS protection circuit.

CD4081B
Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings (Notes 1 and 2)

Voltage at Any Pin	−0.5V to V_{DD} + 0.5V
Package Dissipation	500 mW
V_{DD} Range	−0.5 V_{DC} to +18 V_{DC}
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

Operating V_{DD} Range	3 V_{DC} to 15 V_{DC}
Operating Temperature Range	
CD4071BM, CD4081BM	−55°C to +125°C
CD4071BC, CD4081BC	−40°C to +85°C

dc electrical characteristics CD4071BM, CD4081BM (Note 2)

PARAMETER		CONDITIONS	−55°C		+25°C			+125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25		0.004	0.25		7.5	μA
		V_{DD} = 10V		0.50		0.005	0.50		15	μA
		V_{DD} = 15V		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

dc electrical characteristics CD4071BC, CD4081BC (Note 2)

PARAMETER		CONDITIONS	−40°C MIN	−40°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+85°C MIN	+85°C MAX	UNITS
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.004	1		7.5	μA
		V_{DD} = 10V		2		0.005	2		15	μA
		V_{DD} = 15V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V, $\lvert I_O \rvert < 1\mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10V, $\lvert I_O \rvert < 1\mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15V, $\lvert I_O \rvert < 1\mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics CD4071BC, CD4071BM

T_A = 25°C, Input t_r; t_f = 20 ns. C_L = 50 pF. R_L=200KΩ Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	V_{DD} = 5V	100	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	V_{DD} = 5V	90	250	ns
		V_{DD} = 10V	40	100	ns
		V_{DD} = 15V	30	70	ns
t_{THL},t_{TLH}	Transition Time	V_{DD} = 5V	90	200	ns
		V_{DD} = 10V	50	100	ns
		V_{DD} = 15V	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

ac electrical characteristics CD4081BC, CD4081BM

$T_A = 25°C$, Input t_r; $t_f = 20$ ns. $C_L = 50$ pF. $R_L = 200K$ Typical temperature coefficient is 0.3%/°C

PARAMETER		CONDITIONS	TYP	MAX	UNITS
t_{PHL}	Propagation Delay Time, High-to-Low Level	$V_{DD} = 5V$	100	250	ns
		$V_{DD} = 10V$	40	100	ns
		$V_{DD} = 15V$	30	70	ns
t_{PLH}	Propagation Delay Time, Low-to-High Level	$V_{DD} = 5V$	120	250	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	35	70	ns
t_{THL},t_{TLH}	Transition Time	$V_{DD} = 5V$	90	200	ns
		$V_{DD} = 10V$	50	100	ns
		$V_{DD} = 15V$	40	80	ns
C_{IN}	Average Input Capacitance	Any Input	5	7.5	pF
C_{PD}	Power Dissipation Capacity	Any Gate	18		pF

typical performance characteristics

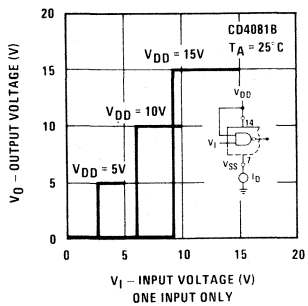


FIGURE 1. Typical Transfer Characteristics

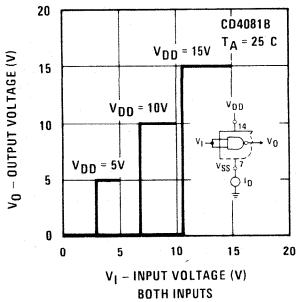


FIGURE 2. Typical Transfer Characteristics

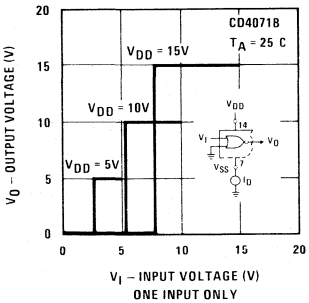


FIGURE 3. Typical Transfer Characteristics

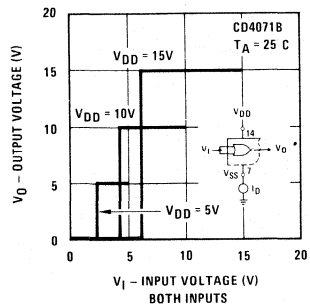


FIGURE 4. Typical Transfer Characteristics

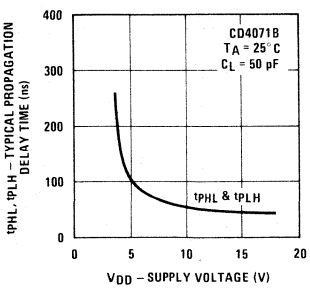


FIGURE 5

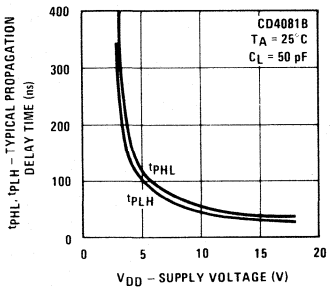


FIGURE 6

typical performance characteristics (con't)

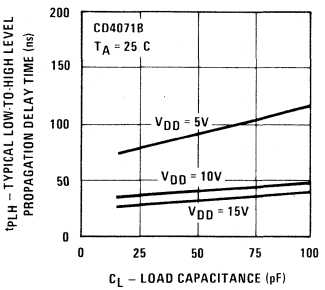


FIGURE 7

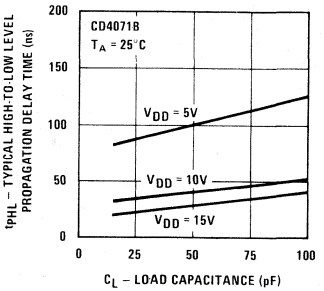


FIGURE 8

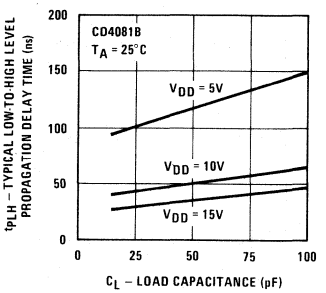


FIGURE 9

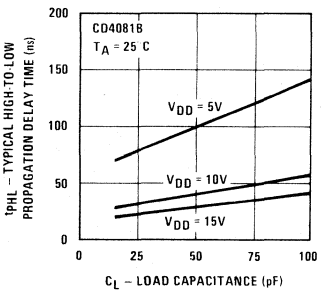


FIGURE 10

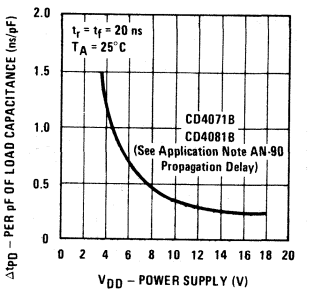


FIGURE 11

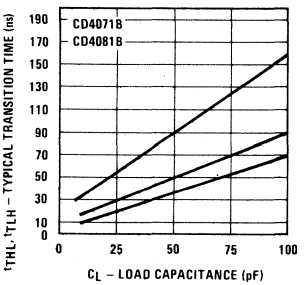


FIGURE 12

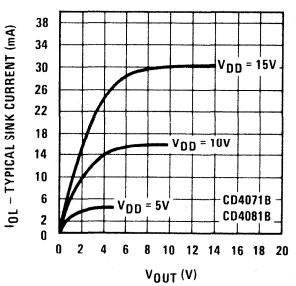


FIGURE 13

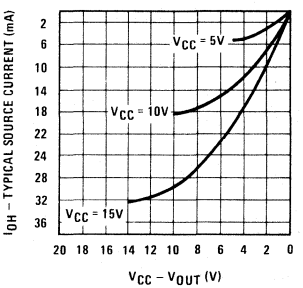


FIGURE 14

National Semiconductor

CD4073BM/CD4073BC Double Buffered Triple 3-Input AND Gate
CD4075BM/CD4075BC Double Buffered Triple 3-Input OR Gate

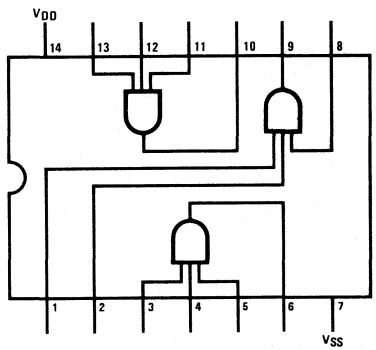
general description

These triple gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. They have equal source and sink current capabilities and conform to standard B series output drive. The devices also have buffered outputs which improve transfer characteristics by providing very high gain. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS}.

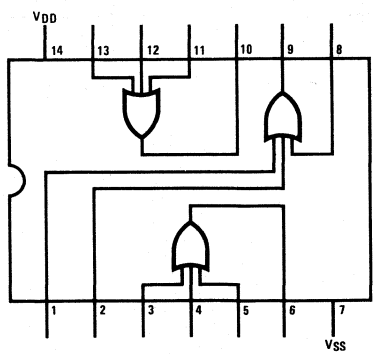
features

■ Wide supply voltage range	3.0 V to 15 V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ 5 V - 10 V - 15 V parametric ratings	
■ Symmetrical output characteristics	
■ Maximum input leakage 1 μA at 15 V over full temperature range	

connection diagrams



CD4073 Triple 3-Input AND Gate
TOP VIEW



CD4075B Triple 3-Input OR Gate
TOP VIEW

absolute maximum ratings (Notes 1 and 2)

V_{DD}	DC Supply Voltage	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
V_{IN}	Input Voltage	$-0.5\ V_{DC}$ to $V_{DD} + 0.5\ V_{DC}$
T_S	Storage Temperature Range	$-65°C$ to $+150°C$
P_D	Package Dissipation	500 mW
T_L	Lead Temperature (soldering, 10 seconds)	300°C

recommended operating conditions (Note 2)

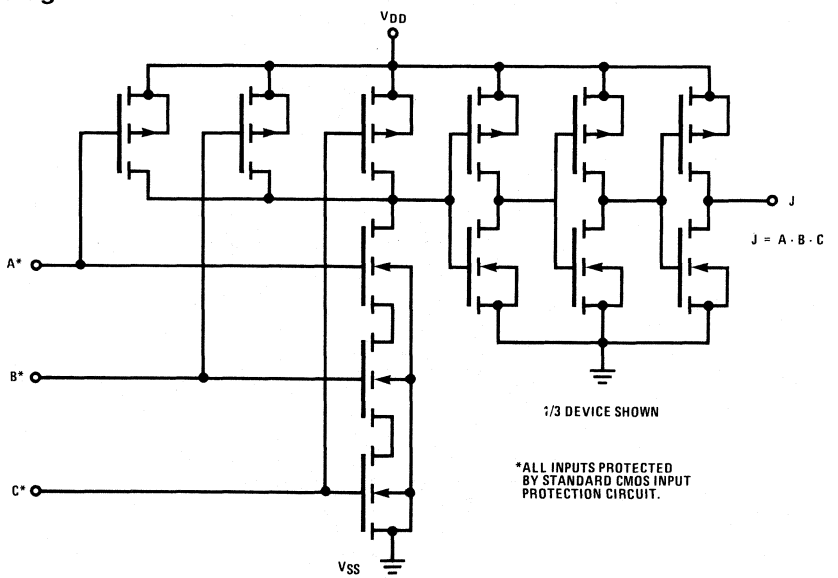
V_{DD}	DC Supply Voltage	$+5\ V_{DC}$ to $+15\ V_{DC}$
V_{IN}	Input Voltage	$0\ V_{DC}$ to $V_{DD}\ V_{DC}$
T_A	Operating Temperature Range	
CD4073BM/CD4075BM		$-55°C$ to $+125°C$
CD4073BC/CD4075BC		$-40°C$ to $+85°C$

dc electrical characteristics— CD4073BM/CD4075BM (Note 2)

PARAMETER		CONDITIONS	−55°C MIN	−55°C MAX	+25°C MIN	+25°C TYP	+25°C MAX	+125°C MIN	+125°C MAX	UNITS
I_{DD}	Quiescent Device Current	$V_{DD} = 5\ V$		0.25		0.004	0.25		7.5	μA
		$V_{DD} = 10\ V$		0.5		0.005	0.5		15	μA
		$V_{DD} = 15\ V$		1.0		0.006	1.0		30	μA
V_{OL}	Low Level Output Voltage	$V_{DD} = 5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 15\ V$ | $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{DD} = 5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10\ V$ | $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		$V_{DD} = 15\ V$ | $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$V_{DD} = 5\ V,\ V_O = 0.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		1.5		2	1.5		1.5	V
		$V_{DD} = 10\ V,\ V_O = 1.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		$V_{DD} = 15\ V,\ V_O = 1.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD} = 5\ V,\ V_O = 4.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5	3		3.5		V
		$V_{DD} = 10\ V,\ V_O = 9.0\ V$ | $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		$V_{DD} = 15\ V,\ V_O = 13.5\ V$ | $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$V_{DD} = 5\ V,\ V_O = 0.4\ V$	0.64		0.51	0.88		0.36		mA
		$V_{DD} = 10\ V,\ V_O = 0.5\ V$	1.6		1.3	2.2		0.90		mA
		$V_{DD} = 15\ V,\ V_O = 1.5\ V$	4.2		3.4	8		2.4		mA
I_{OH}	High Level Output Current	$V_{DD} = 5\ V,\ V_O = 4.6\ V$	−0.64		−0.51	−0.88		−0.36		mA
		$V_{DD} = 10\ V,\ V_O = 9.5\ V$	−1.6		−1.3	−2.2		−0.90		mA
		$V_{DD} = 15\ V,\ V_O = 13.5\ V$	−4.2		−3.4	−8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15\ V,\ V_{IN} = 0\ V$		−0.10		-10^{-5}	−0.10		−1.0	μA
		$V_{DD} = 15\ V,\ V_{IN} = 15\ V$		0.10		10^{-5}	0.10		1.0	μA

Notes on following page.

schematic diagram



CD4073BC

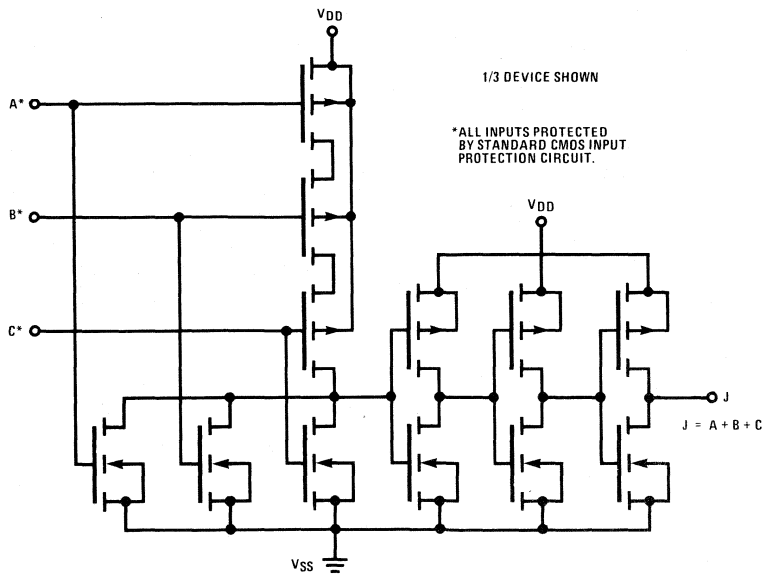
dc electrical characteristics— CD4073BC/CD4075BC (Note 2)

PARAMETER		CONDITIONS	−40°C		+25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5 V		1		0.004	1		7.5	μA
		V_{DD} = 10 V		2		0.005	2		15	μA
		V_{DD} = 15 V		4		0.006	4		30	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5 V, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 10 V, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
		V_{DD} = 15 V, $\lvert I_O \rvert < 1\ \mu A$		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5 V, $\lvert I_O \rvert < 1\ \mu A$	4.95		4.95	5		4.95		V
		V_{DD} = 10 V, $\lvert I_O \rvert < 1\ \mu A$	9.95		9.95	10		9.95		V
		V_{DD} = 15 V, $\lvert I_O \rvert < 1\ \mu A$	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5 V, V_O = 0.5 V, $\lvert I_O \rvert < 1\ \mu A$		1.5		2	1.5		1.5	V
		V_{DD} = 10 V, V_O = 1.0 V, $\lvert I_O \rvert < 1\ \mu A$		3.0		4	3.0		3.0	V
		V_{DD} = 15 V, V_O = 1.5 V, $\lvert I_O \rvert < 1\ \mu A$		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5 V, V_O = 4.5 V, $\lvert I_O \rvert < 1\ \mu A$	3.5		3.5	3		3.5		V
		V_{DD} = 10 V, V_O = 9.0 V, $\lvert I_O \rvert < 1\ \mu A$	7.0		7.0	6		7.0		V
		V_{DD} = 15 V, V_O = 13.5 V, $\lvert I_O \rvert < 1\ \mu A$	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5 V, V_O = 0.4 V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10 V, V_O = 0.5 V	1.3		1.1	2.2		0.90		mA
		V_{DD} = 15 V, V_O = 1.5 V	3.6		3.0	8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5 V, V_O = 4.6 V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10 V, V_O = 9.5 V	−1.3		−1.1	−2.2		−0.90		mA
		V_{DD} = 15 V, V_O = 13.5 V	−3.6		−3.0	−8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15 V, V_{IN} = 0 V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15 V, V_{IN} = 15 V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0 V unless otherwise specified.

schematic diagram



CD4075BC

ac electrical characteristics—CD4073BM/CD4073BC, CD4075BM/CD4075BC

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200k$, unless otherwise specified.

PARAMETER		CONDITIONS	CD4073BC CD4073BM			CD4075BC CD4075BM			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay, High to Low Level	$V_{DD} = 5\,V$		130	250		140	250	ns
		$V_{DD} = 10\,V$		60	100		70	100	ns
		$V_{DD} = 15\,V$		40	70		50	70	ns
t_{PLH}	Propagation Delay, Low to High Level	$V_{DD} = 5\,V$		140	250		130	250	ns
		$V_{DD} = 10\,V$		70	100		50	100	ns
		$V_{DD} = 15\,V$		50	70		40	70	ns
t_{THL} t_{TLH}	Transition Time	$V_{DD} = 5\,V$		90	200		90	200	ns
		$V_{DD} = 10\,V$		50	100		50	100	ns
		$V_{DD} = 15\,V$		40	80		40	80	ns
C_{IN}	Average Input Capacitance (See Note 3)	Any Input		5	7.5		5	7.5	pF
C_{PD}	Power Dissipation Capacity (See Note 4)	Any Gate		17			17		pF

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see 54C/74C Family characteristics Application Note AN-90.

National Semiconductor

CD4076BM/CD4076BC TRI-STATE® Quad D Flip-Flop

general description

The CD4076BM/CD4076BC TRI-STATE quad D flip-flop is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The four D type flip-flops operate synchronously from a common clock. The TRI-STATE output allows the device to be used in bus organized systems. The outputs are placed in the TRI-STATE mode when either of the two output disable pins are in the logic "1" level. The input disables allow the flip-flops to remain in their present states without disrupting the clock. If either of the two input disables is taken to a logic "1" level, the Q outputs are fed back to the inputs and in this manner the flip-flops do not change state.

Clearing is enabled by taking the clear input to a logic "1" level. Clocking occurs on the positive-going transition.

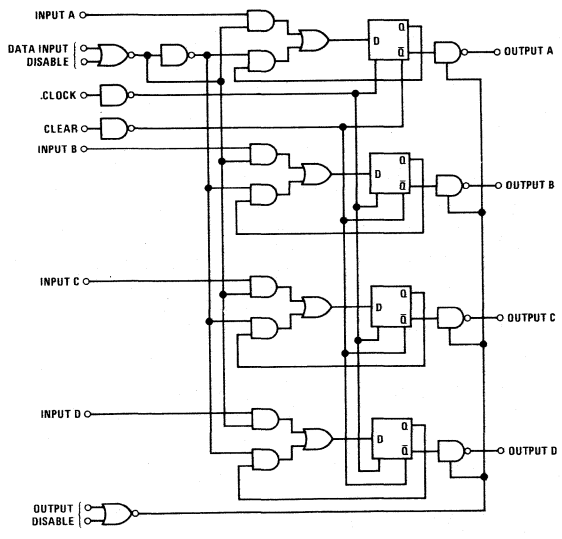
All inputs are protected against damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

features

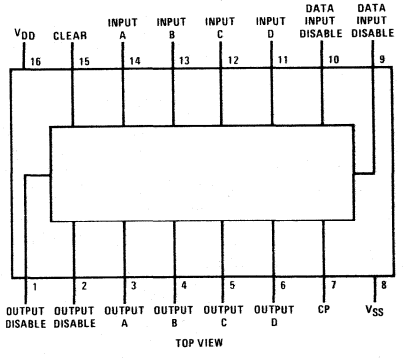
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.45 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS

- High impedance TRI-STATE outputs
- Inputs can be disabled without gating the clock
- Equivalent to MM54C173/MM74C173

logic and connection diagrams



Dual-In-Line Package



TOP VIEW

truth table

t_n		t_{n+1}
DATA INPUT DISABLE	DATA INPUT	OUTPUT
Logic "1" on One or Both Inputs	X	Q_n
Logic "0" on Both Inputs	1	1
Logic "0" on Both Inputs	0	0

absolute maximum ratings (Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions (Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4076BM	−55°C to +125°C
CD4076BC	−40°C to +85°C

dc electrical characteristics CD4076BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4076BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA

dc electrical characteristics (con't) CD4076BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	Output Current in High Impedance State	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200kΩ, and $t_r = t_f$ = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		65	160	ns
t_{PHL}	Propagation Delay Time From Clear to Output	V_{DD} = 5V		240	490	ns
		V_{DD} = 10V		90	180	ns
		V_{DD} = 15V		70	145	ns
t_{SU}	Minimum Input Data Set-Up Time	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		15	30	ns
		V_{DD} = 15V		12	25	ns
t_H	Minimum Input Data Hold Time	V_{DD} = 5V		−40	0	ns
		V_{DD} = 10V		−12	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SU}	Minimum Input Disable Set-Up Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		35	70	ns
		V_{DD} = 15V		28	55	ns
t_H	Minimum Input Disable Hold Time	V_{DD} = 5V		−75	0	ns
		V_{DD} = 10V		−30	0	ns
		V_{DD} = 15V		−25	0	ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time From Output Disable to High Impedance State	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L 1.0k		70	140	ns
		V_{DD} = 15V, R_L 1.0k		56	115	ns
t_{PZH}, t_{PZL}	Propagation Delay From Output Disable to Logical "1" Level or Logical "0" Level (From High Impedance State)	V_{DD} = 5V, R_L = 1.0k		170	340	ns
		V_{DD} = 10V, R_L = 1.0k		70	140	ns
		V_{DD} = 15V, R_L = 1.0k		56	115	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	3.0	4.0		MHz
		V_{DD} = 10V	7.0	12.0		MHz
		V_{DD} = 15V	8.75	15.0		MHz
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		150		ns
		V_{DD} = 10V		70		ns
		V_{DD} = 15V		56		ns
t_{RCL}, t_{FCL}	Maximum Clock Rise and Fall Time	V_{DD} = 5V	10			μs
		V_{DD} = 10V	5			μs
		V_{DD} = 15V	2			μs
C_{IN}	Average Input Capacitance	Data Inputs (A, B, C, D)		3	7.5	pF
		Other Inputs		6	15	pF
C_{PD}	Power Dissipation Capacity	All Four Flip-Flops, (Note 3)		100		pF
C_{OUT}	TRI-STATE® Output Capacitance	Any Output			15	pF

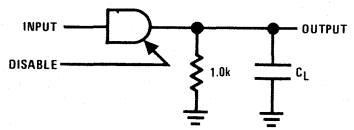
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

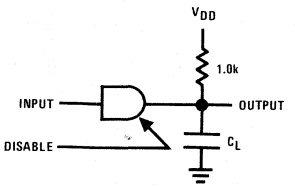
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN–90.

ac test circuits and switching time waveforms

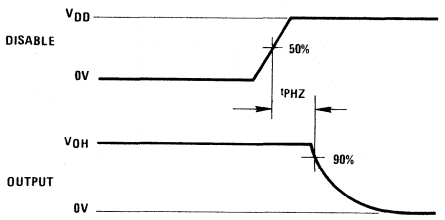
t_{PHZ} and t_{PZH}



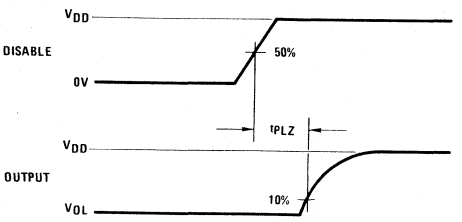
t_{PLZ} and t_{PZL}



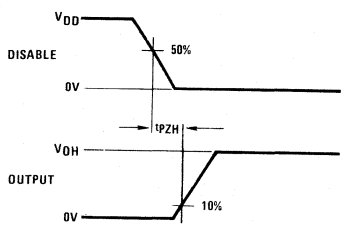
t_{PHZ}



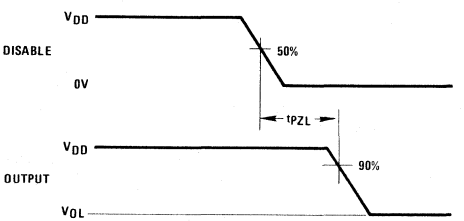
t_{PLZ}

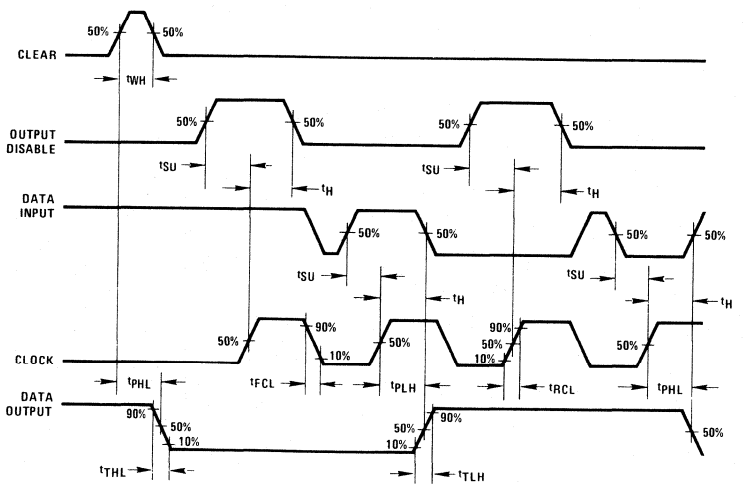


t_{PZH}



t_{PZL}





National Semiconductor

CD4089BM/CD4089BC Binary Rate Multiplier
CD4527BM/CD4527BC BCD Rate Multiplier

general description

The CD4089B is a 4-bit binary rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/16 times the binary input number. For example, if 5 is the binary input number, there will be 5 output pulses for every 16 clock pulses.

The CD4527B is a 4-bit BCD rate multiplier that provides an output pulse rate which is the input clock pulse rate multiplied by 1/10 times the BCD input number. For example, if 5 is the BCD input number, there will be 5 output pulses for every 10 clock pulses.

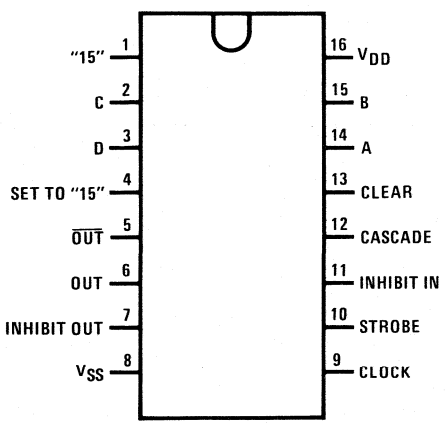
These devices may be used to perform arithmetic operations including multiplication and division, A/D and D/A conversion and frequency division.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internally synchronous 4-bit counter
- Output clocked on the negative-going edge of clock
- STROBE for inhibiting and enabling outputs
- INHIBIT IN and CASCADE inputs for cascade operation
- Complementary output
- CLEAR and SET inputs
- "9" or "15" output and INHIBIT OUT output

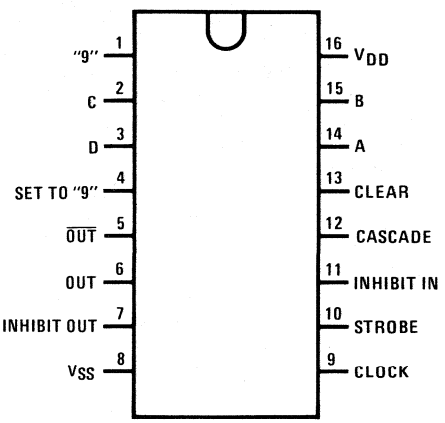
connection diagrams

CD4089B
Dual-In-Line and Flat Package



TOP VIEW

CD4527B
Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5 to +18V
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3 to 15 V
V_{IN} Input Voltage	0 to V_{DD}V
T_A Operating Temperature Range	
CD4089BM, CD4527BM	−55°C to +125°C
CD4089BC, CD4527BC	−40°C to +85°C

dc electrical characteristics CD4089BM, CD4527BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4089BC, CD4527BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA

dc electrical characteristics (Continued) CD4089BC, CD4527BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to Out or $\overline{Out}$	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		60	120	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to E_{OUT}	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	240	ns
		V_{DD} = 15V		75	150	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Clock to "9" or "15"	V_{DD} = 5V		280	560	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Set or Clear to Out or $\overline{Out}$	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		200	400	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Cascade to Out	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		35	70	ns
t_{PLH}, t_{PHL}	Propagation Delay Time, Strobe to Out	V_{DD} = 5V		220	440	ns
		V_{DD} = 10V		85	170	ns
		V_{DD} = 15V		65	130	ns
t_{TLH}, t_{THL}	Transition Time, All Outputs	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
$t_{W(CL)}$	Minimum Clock Pulse Width	V_{DD} = 5V		250	500	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		70	140	ns
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V		2	1	MHz
		V_{DD} = 10V		5	2.5	MHz
		V_{DD} = 15V		7	3.5	MHz
t_r	Maximum Clock Rise Time	V_{DD} = 5V			5	μs
		V_{DD} = 10V			1.5	μs
		V_{DD} = 15V			1.0	μs
t_f	Maximum Clock Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			15	μs
		V_{DD} = 15V			15	μs
$t_{W(S,R)}$	Minimum Set or Clear Pulse Width	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		25	55	ns
t_{REM}	Set Removal Time	V_{DD} = 5V		−45	0	ns
		V_{DD} = 10V		−20	0	ns
		V_{DD} = 15V		−10	0	ns
t_{SET-UP}	Inhibit In Set-Up Time	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		60	120	ns
		V_{DD} = 15V		45	90	ns
C_I	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 3)		80		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

truth tables

CD4089B
Binary Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "15"
0	0	0	0	16	0	0	0	0	0	L	H	1	1
0	0	0	1	16	0	0	0	0	0	1	1	1	1
0	0	1	0	16	0	0	0	0	0	2	2	1	1
0	0	1	1	16	0	0	0	0	0	3	3	1	1
0	1	0	0	16	0	0	0	0	0	4	4	1	1
0	1	0	1	16	0	0	0	0	0	5	5	1	1
0	1	1	0	16	0	0	0	0	0	6	6	1	1
0	1	1	1	16	0	0	0	0	0	7	7	1	1
1	0	0	0	16	0	0	0	0	0	8	8	1	1
1	0	0	1	16	0	0	0	0	0	9	9	1	1
1	0	1	0	16	0	0	0	0	0	10	10	1	1
1	0	1	1	16	0	0	0	0	0	11	11	1	1
1	1	0	0	16	0	0	0	0	0	12	12	1	1
1	1	0	1	16	0	0	0	0	0	13	13	1	1
1	1	1	0	16	0	0	0	0	0	14	14	1	1
1	1	1	1	16	0	0	0	0	0	15	15	1	1
X	X	X	X	16	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	16	0	1	0	0	0	L	H	1	1
X	X	X	X	16	0	0	1	0	0	H	*	1	1
1	X	X	X	16	0	0	0	1	0	16	16	H	L
0	X	X	X	16	0	0	0	1	0	L	H	H	L
X	X	X	X	16	0	0	0	0	1	L	H	L	H

*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

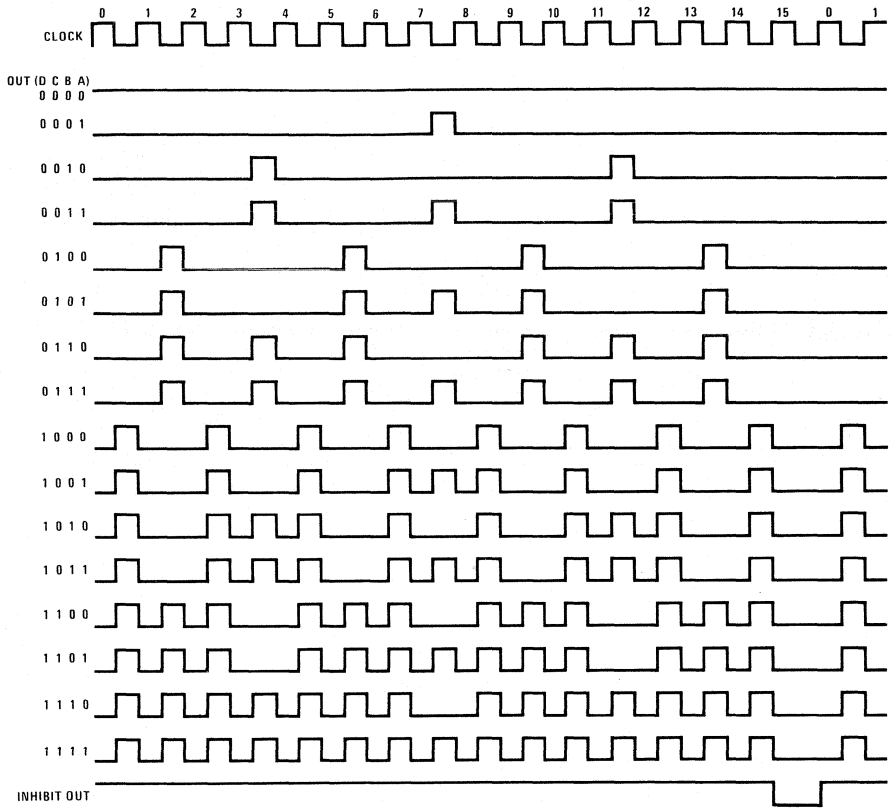
CD4527B
BCD Rate Multiplier

INPUTS										NUMBER OF PULSES OR OUTPUT LOGIC LEVEL (H OR L)			
D	C	B	A	No. of Clock Pulses	Inh_{In}	Strobe	Cascade	Clear	Set	Pin 6 Out	Pin 5 $\overline{Out}$	Pin 7 Inh Out	Pin 1 "9"
0	0	0	0	10	0	0	0	0	0	L	H	1	1
0	0	0	1	10	0	0	0	0	0	1	1	1	1
0	0	1	0	10	0	0	0	0	0	2	2	1	1
0	0	1	1	10	0	0	0	0	0	3	3	1	1
0	1	0	0	10	0	0	0	0	0	4	4	1	1
0	1	0	1	10	0	0	0	0	0	5	5	1	1
0	1	1	0	10	0	0	0	0	0	6	6	1	1
0	1	1	1	10	0	0	0	0	0	7	7	1	1
1	0	0	0	10	0	0	0	0	0	8	8	1	1
1	0	0	1	10	0	0	0	0	0	9	9	1	1
1	0	1	0	10	0	0	0	0	0	8	8	1	1
1	0	1	1	10	0	0	0	0	0	9	9	1	1
1	1	0	0	10	0	0	0	0	0	8	8	1	1
1	1	0	1	10	0	0	0	0	0	9	9	1	1
1	1	1	0	10	0	0	0	0	0	8	8	1	1
1	1	1	1	10	0	0	0	0	0	9	9	1	1
X	X	X	X	10	1	0	0	0	0	Depends on internal state of counter			
X	X	X	X	10	0	1	0	0	0	L	H	1	1
X	X	X	X	10	0	0	1	0	0	H	*	1	1
1	X	X	X	10	0	0	0	1	0	10	10	H	L
0	X	X	X	10	0	0	0	1	0	L	H	H	L
X	X	X	X	10	0	0	0	0	1	L	H	L	H

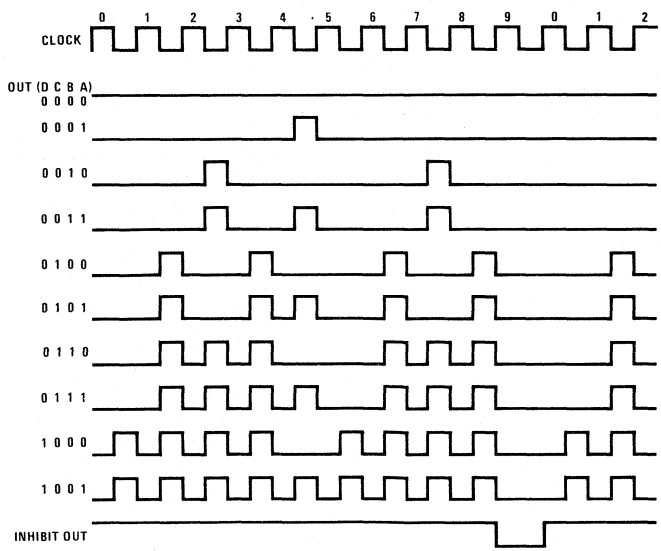
*Output same as the first 16 lines of this truth table (depending on values of A, B, C, D)

logic waveforms

CD4089B
Binary Rate Multiplier

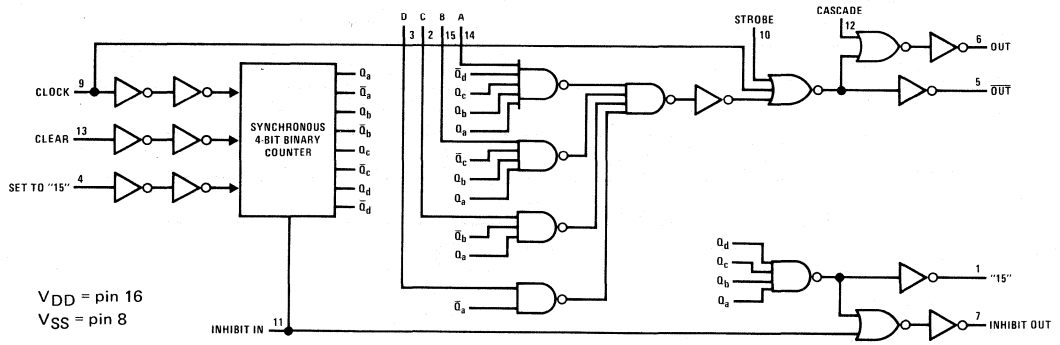


CD4527B
BCD Rate Multiplier

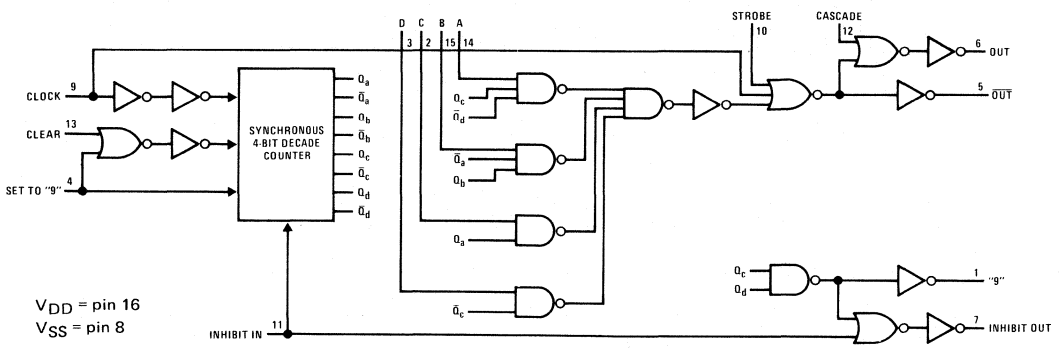


logic diagrams

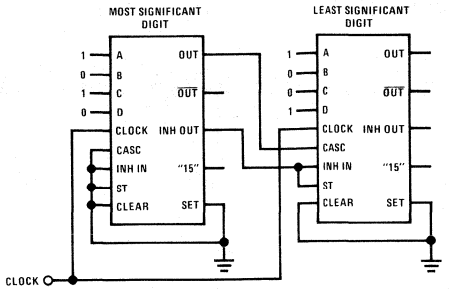
CD4089B
Binary Rate Multiplier



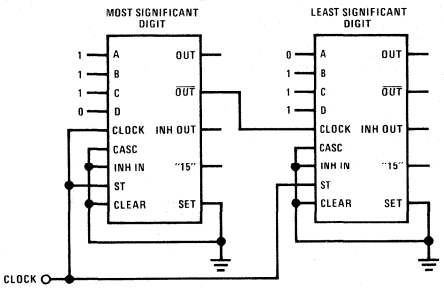
CD4527B
BCD Rate Multiplier



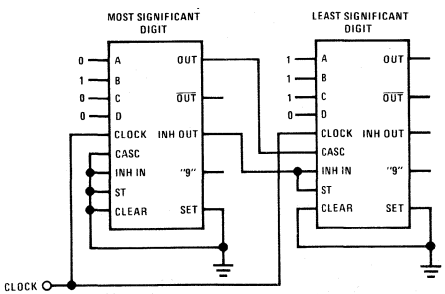
cascading packages



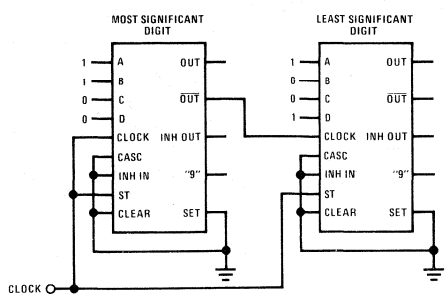
Two CD4089B's cascaded in the "add" mode with a preset number of 89 $\left(\frac{5}{16} + \frac{9}{256} = \frac{89}{256}\right)$



Two CD4089B's cascaded in the "multiply" mode with a preset number of 98 $\left(\frac{7}{16} \times \frac{14}{16} = \frac{98}{256}\right)$



Two CD4527B's cascaded in the "add" mode with a preset number of 27 $\left(\frac{2}{10} + \frac{7}{100} = \frac{27}{100}\right)$



Two CD4527B's cascaded in the "multiply" mode with a preset number of 27 $\left(\frac{3}{10} \times \frac{9}{10} = \frac{27}{100}\right)$

National Semiconductor

CD4093BM/CD4093BC Quad 2-Input NAND Schmitt Trigger

general description

The CD4093B consists of four Schmitt-trigger circuits. Each circuit functions as a 2-input NAND gate with Schmitt-trigger action on both inputs. The gate switches at different points for positive and negative-going signals. The difference between the positive (V_{T+}) and the negative voltage (V_{T-}) is defined as hysteresis voltage (V_H).

All outputs have equal source and sink currents and conform to standard B-series output drive (see Static Electrical Characteristics).

features

- Wide supply voltage range 3V to 15V
- Schmitt-trigger on each input with no external components
- Noise immunity greater than 50%
- Equal source and sink currents
- No limit on input rise and fall time
- Standard B-series output drive
- Hysteresis voltage (any input) $T_A = 25°C$

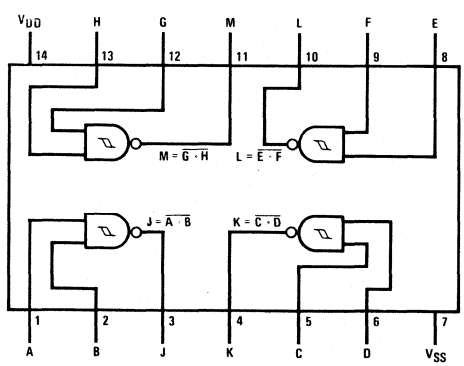
Typical	$V_{DD} = 5V$	$V_H = 1.5V$
	$V_{DD} = 10V$	$V_H = 2.2V$
	$V_{DD} = 15V$	$V_H = 2.7V$
Guaranteed		$V_H = 0.1\ V_{DD}$

applications

- Wave and pulse shapers
- High-noise-environment systems
- Monostable multivibrators
- Astable multivibrators
- NAND logic

connection diagram

Dual-In-Line Package



absolute maximum ratings

(Notes 1 and 2)

DC Supply Voltage (V_{DD})	−0.5 to +18 V_{DC}
Input Voltage (V_{IN})	−0.5 to V_{DD} +0.5 V_{DC}
Storage Temperature Range (T_S)	−65°C to +150°C
Package Dissipation (P_D)	500 mW
Lead Temperature (Soldering, 10 seconds) (T_L)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4093BM	−55°C to +125°C
CD4093BC	−40°C to +85°C

dc electrical characteristics CD4093BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		0.25			0.25		7.5	μA
		V_{DD} = 10V		0.5			0.5		15.0	μA
		V_{DD} = 15V		1.0			1.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.3	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	3.5	3.65	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	7.0	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	10.5	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.30	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.30	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
		V_{DD} = 5V, V_O = 4.6V	−0.64		0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

dc electrical characteristics CD4093BC (Note 2)

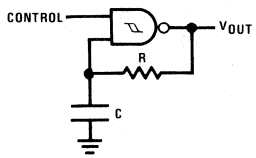
PARAMETER		CONDITIONS	−40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		7.5	μA
		V_{DD} = 10V		2.0			2.0		15.0	μA
		V_{DD} = 15V		4.0			4.0		30.0	μA
V_{OL}	Low Level Output Voltage	V_{IN} = V_{DD}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IN} = V_{SS}, $\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 4.5V	1.3	2.25	1.5	1.8	2.25	1.5	2.30	V
		V_{DD} = 10V, V_O = 9V	2.85	4.5	3.0	4.1	4.5	3.0	4.65	V
		V_{DD} = 15V, V_O = 13.5V	4.35	6.75	4.5	6.3	6.75	4.5	6.9	V
V_{T+}	Positive-Going Threshold Voltage	$\|I_O\| < 1\mu A$								
	(Any Input)	V_{DD} = 5V, V_O = 0.5V	3.5	3.6	2.75	3.3	3.5	2.65	3.5	V
		V_{DD} = 10V, V_O = 1V	7.0	7.15	5.5	6.2	7.0	5.35	7.0	V
		V_{DD} = 15V, V_O = 1.5V	10.5	10.65	8.25	9.0	10.5	8.1	10.5	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	0.5	2.35	0.5	1.5	2.0	0.35	2.0	V
	(Any Input)	V_{DD} = 10V	1.0	4.3	1.0	2.2	4.0	0.70	4.0	V
		V_{DD} = 15V	1.5	6.3	1.5	2.7	6.0	1.20	6.0	V
I_{OL}	Low Level Output Current	V_{IN} = V_{DD}								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{IN} = V_{SS}								
		V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

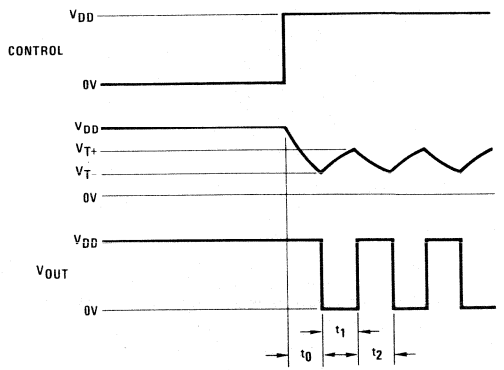
ac electrical characteristics T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 50 pF, R_L = 200k, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		300	600	ns
		V_{DD} = 10V		120	300	ns
		V_{DD} = 15V		80	240	ns
t_{THL}, t_{TLH}	Transition Time	V_{DD} = 5V		90	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance			5.0	7.5	pF
C_{PD}	Power Dissipation Capacitance			24		pF

typical applications

Gated Oscillator





Assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$ then:

$t_0 = RC \ln [V_{DD}/V_{T-}]$

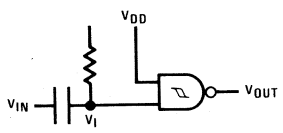
$t_1 = RC \ln [(V_{DD} - V_{T-})/(V_{DD} + V_{T+})]$

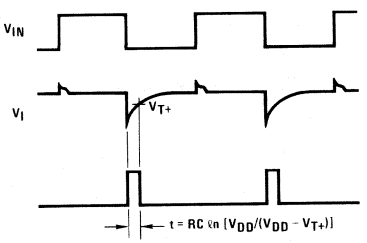
$t_2 = RC \ln [V_{T+}/V_{T-}]$

$$f = \frac{1}{t_1 + t_2} = \frac{1}{RC \ln \dfrac{(V_{T+})(V_{DD} - V_{T-})}{(V_{T-})(V_{DD} - V_{T+})}}$$

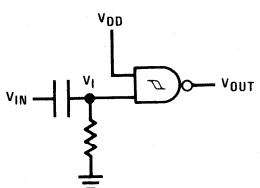
Gated One-Shot

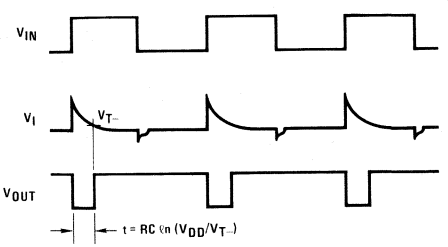
(a) Negative-Edge Triggered





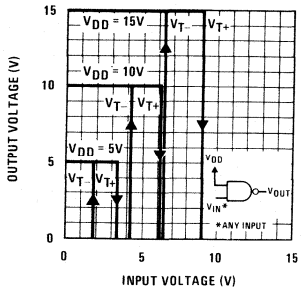
(b) Positive-Edge Triggered



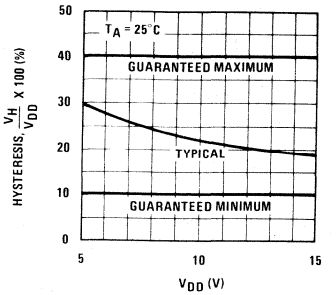


typical performance characteristics

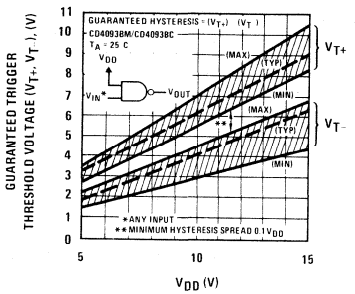
Typical Transfer Characteristics



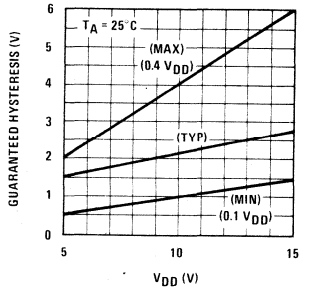
Guaranteed Hysteresis vs V_{DD}



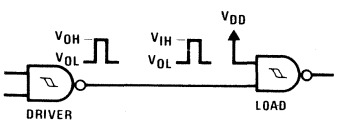
Guaranteed Trigger Threshold Voltage vs V_{DD}

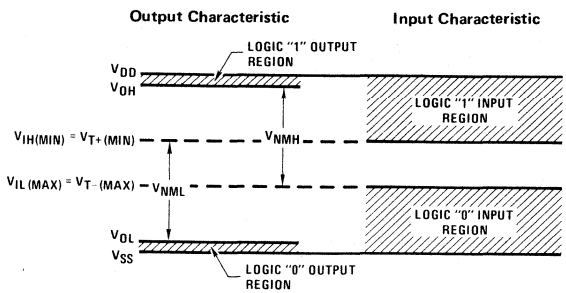


Guaranteed Hysteresis vs V_{DD}



input and output characteristics

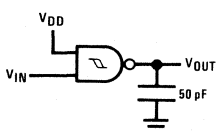


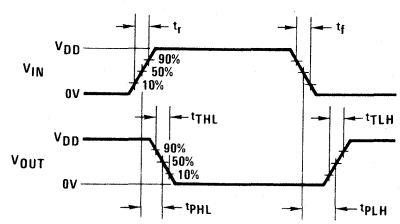


$V_{NML} = V_{IH(MIN)} - V_{OL} \cong V_{IH(MIN)} = V_{T+(MIN)}$

$V_{NMH} = V_{OH} - V_{IL(MAX)} \cong V_{DD} - V_{IL(MAX)} = V_{DD} - V_{T-(MAX)}$

ac test circuits and switching time waveforms





National Semiconductor

CD40106BM/CD40106BC Hex Schmitt Trigger

general description

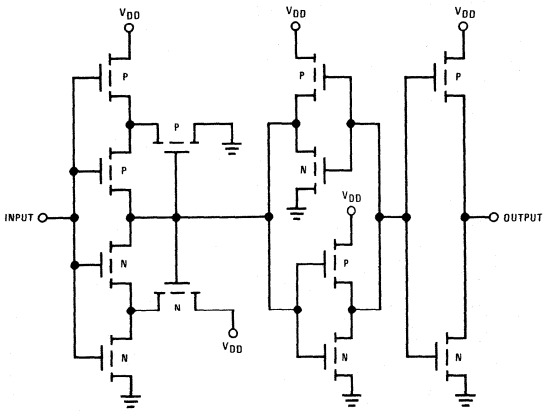
The CD40106B Hex Schmitt Trigger is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement transistors. The positive and negative-going threshold voltages, V_{T+} and V_{T-}, show low variation with respect to temperature (typ 0.0005V/°C at V_{DD} = 10V), and hysteresis, $V_{T+} - V_{T-} \geq 0.2\ V_{DD}$ is guaranteed.

All inputs are protected from damage due to static discharge by diode clamps to V_{DD} and V_{SS}.

features

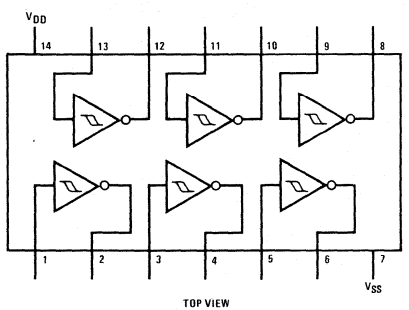
■ Wide supply voltage range	3V to 15V
■ High noise immunity	0.7 V_{DD} typ
■ Low power TTL compatibility	fan out of 2 driving 74L or 1 driving 74LS
■ Hysteresis	0.4 V_{DD} typ 0.2 V_{DD} guaranteed
■ Equivalent to MM54C14/MM74C14	
■ Equivalent to MC14584B	

schematic diagram



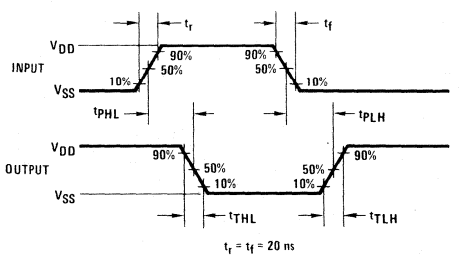
connection diagram

Dual-In-Line Package



TOP VIEW

switching time waveforms



$t_r = t_f = 20$ ns

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40106BM	−55°C to +125°C
CD40106BC	−40°C to +85°C

dc electrical characteristics CD40106BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note—AN-90.

dc electrical characteristics CD40106BC (Note 2)

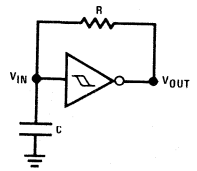
PARAMETER		CONDITIONS	−40°C		25°C			+85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4.0			4.0		30	μA
		V_{DD} = 10V		8.0			8.0		60	μA
		V_{DD} = 15V		16.0			16.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{T-}	Negative-Going Threshold Voltage	V_{DD} = 5V, V_O = 4.5V	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		V_{DD} = 10V, V_O = 9V	1.4	4.0	1.4	3.2	4.0	1.4	4.0	V
		V_{DD} = 15V, V_O = 13.5V	2.1	6.0	2.1	5.0	6.0	2.1	6.0	V
V_{T+}	Positive-Going Threshold Voltage	V_{DD} = 5V, V_O = 0.5V	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		V_{DD} = 10V, V_O = 1V	6.0	8.6	6.0	6.8	8.6	6.0	8.6	V
		V_{DD} = 15V, V_O = 1.5V	9.0	12.9	9.0	10.0	12.9	9.0	12.9	V
V_H	Hysteresis ($V_{T+} - V_{T-}$)	V_{DD} = 5V	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		V_{DD} = 10V	2.0	7.2	2.0	3.6	7.2	2.0	7.2	V
		V_{DD} = 15V	3.0	10.8	3.0	5.0	10.8	3.0	10.8	V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, t_r and t_f = 20 ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Input To Output	V_{DD} = 5V		220	400	ns
		V_{DD} = 10V		80	200	ns
		V_{DD} = 15V		70	160	ns
t_{THL} or t_{TLH}	Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Any Gate (Note 3)		14		pF

typical applications

Low Power Oscillator

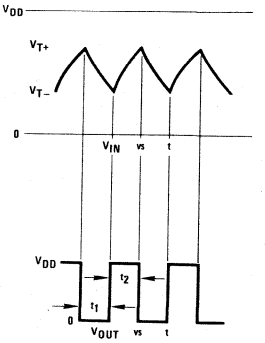


$$t_1 \approx RC\,\ell n\,\frac{V_{T+}}{V_{T-}}$$

$$t_2 \approx RC\,\ell n\,\frac{V_{DD}-V_{T-}}{V_{DD}-V_{T+}}$$

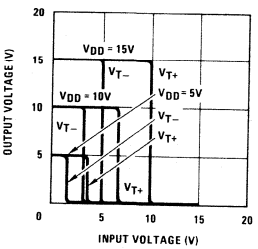
$$f \approx \frac{1}{RC\,\ell n\,\frac{V_{T+}(V_{DD}-V_{T-})}{V_{T-}(V_{DD}-V_{T+})}}$$

Note: The equations assume $t_1 + t_2 >> t_{PHL} + t_{PLH}$

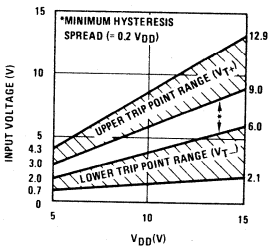


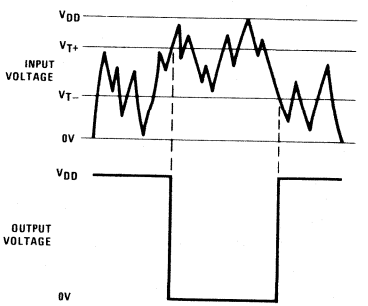
typical performance characteristics

Typical Transfer Characteristics



Guaranteed Trip Point Range





National Semiconductor

CD40160BM/CD40160BC Decade Counter with Asynchronous Clear
CD40161BM/CD40161BC Binary Counter with Asynchronous Clear
CD40162BM/CD40162BC Decade Counter with Synchronous Clear
CD40163BM/CD40163BC Binary Counter with Synchronous Clear

general description

These (synchronous presettable up) counters are monolithic complementary MOS (CMOS) integrated circuits constructed with N and P-channel enhancement mode transistors. They feature an internal carry look-ahead for fast counting schemes and for cascading packages without additional gating.

A low level at the load input disables counting and causes the outputs to agree with the data input after the next positive clock edge. The clear function for the CD40162B and CD40163B is synchronous and a low level at the clear input sets all four outputs low after the next positive clock edge. The clear function for the CD40160B and CD40161B is asynchronous and a low level at the clear input sets all four outputs low, regardless of the state of the clock.

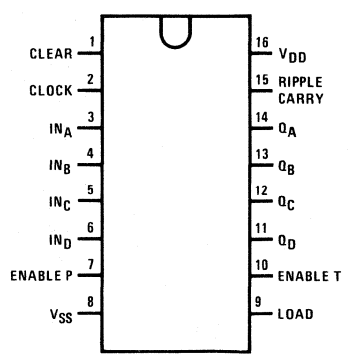
Counting is enabled when both count enable inputs are high. Input T is fed forward to also enable the carry out. The carry output is a positive pulse with a duration approximately equal to the positive portion of Q_A and can be used to enable successive cascaded stages. Logic transitions at the enable P or T inputs can occur when the clock is high or low.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Internal look-ahead for fast counting schemes
- Carry output for N-bit cascading
- Load control line
- Synchronously programmable
- Equivalent to MC14160B, MC14161B, MC14162B, MC14163B
- Equivalent to MM74C160, MM74C161, MM74C162, MM74C163

connection diagram

Dual-In-Line Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

dc electrical characteristics CD40160BM, CD40161BM, CD40162BM, CD40163BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

dc electrical characteristics CD40160BC, CD40161BC, CD40162BC, CD40163BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

dc electrical characteristics (con't) CD40160BC, CD40161BC, CD40162BC, CD40163BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

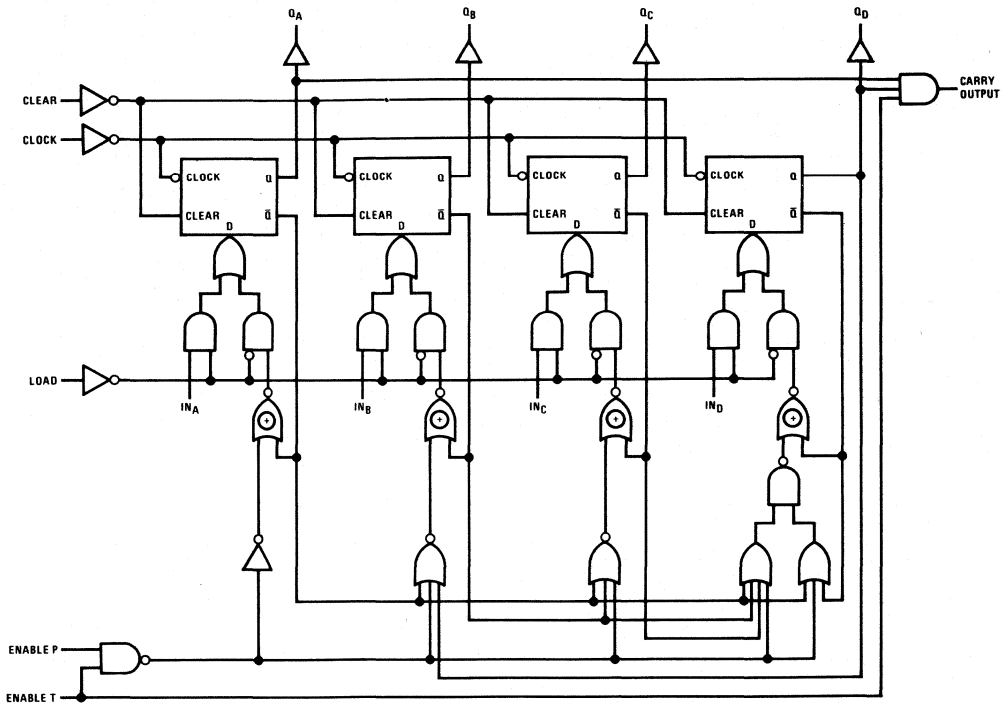
Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation see 54C/74C Family Characteristics application note, AN-90.

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, unless otherwise specified.

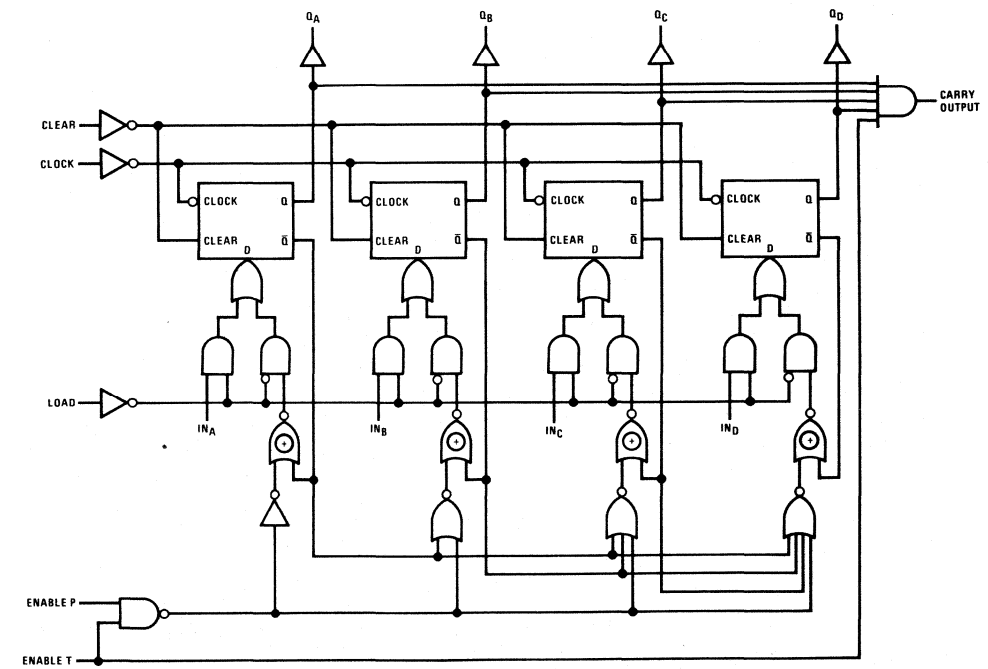
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Q	V_{DD} = 5V		250	400	ns
		V_{DD} = 10V		100	160	ns
		V_{DD} = 15V		80	130	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From Clock to Carry Out	V_{DD} = 5V		290	450	ns
		V_{DD} = 10V		120	190	ns
		V_{DD} = 15V		100	160	ns
t_{PHL} or t_{PLH}	Propagation Delay Time From T Enable to Carry Out	V_{DD} = 5V		180	290	ns
		V_{DD} = 10V		70	130	ns
		V_{DD} = 15V		60	110	ns
t_{PHL}	Propagation Time From Clear to Q (CD40160B, CD40161B Only)	V_{DD} = 5V		190	200	ns
		V_{DD} = 10V		80	80	ns
		V_{DD} = 15V		70	70	ns
t_{SU}	Minimum Time Prior to Clock that Data or Load must be Present	V_{DD} = 5V		120		ns
		V_{DD} = 10V		30		ns
		V_{DD} = 15V		25		ns
t_{SU}	Minimum Time Prior to Clock that Enable P or T must be Present	V_{DD} = 5V		170	280	ns
		V_{DD} = 10V		70	120	ns
		V_{DD} = 15V		60	100	ns
t_{SU}	Minimum Time Prior to Clock that Clear must be Present (CD40162B, CD40163B Only)	V_{DD} = 5V		120	190	ns
		V_{DD} = 10V		50	80	ns
		V_{DD} = 15V		40	70	ns
t_{WL} or t_{WH}	Clock Rise or Fall Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		45	90	ns
		V_{DD} = 15V		35	70	ns
t_{RCL}, t_{FCL}	Maximum Clock Rise or Fall Time	V_{DD} = 5V			15	μs
		V_{DD} = 10V			5.0	μs
		V_{DD} = 15V			5.0	μs
f_{CL}	Maximum Clock Frequency	V_{DD} = 5V	2	4		MHz
		V_{DD} = 10V	5.5	11		MHz
		V_{DD} = 15V	7	14		MHz
t_{THL} or t_{TLH}	Transition Time	All Outputs				
		V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input		5.0	7.5	pF
C_{PD}	Power Dissipation Capacity	(Note 3)		95		pF

logic diagrams

CD40160B, CD40162B Clear is Synchronous for the CD40162B

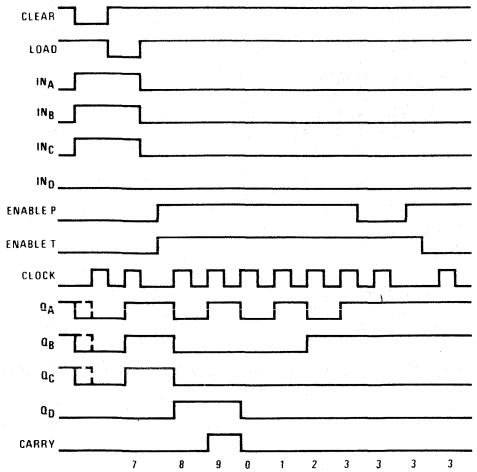


CD40161B, CD40163B Clear is Synchronous for the CD40163B

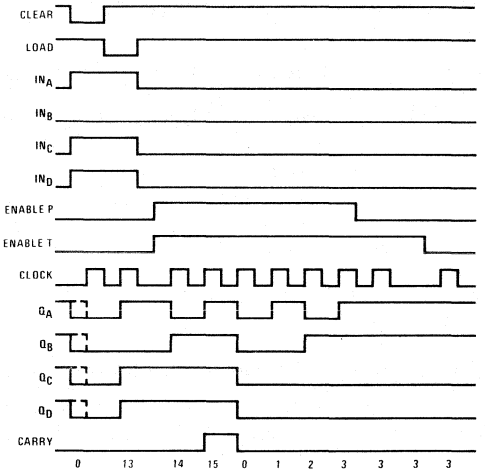


logic waveforms

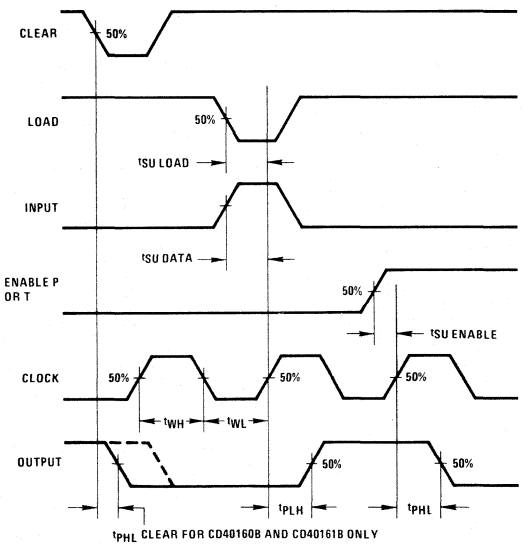
CD40160B, --- CD40162B Decade Counters



CD40161B, --- CD40163B Binary Counters



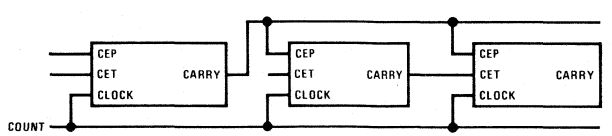
switching time waveforms



Note 1: All input pulses are from generators having the following characteristics: $t_r = t_f = 20$ ns PRR $\leq$ 1 MHz duty cycle $\leq$ 50%, $Z_{OUT} \approx 50\Omega$.

Note 2: All times are measured from 50% to 50%.

cascading packages



National Semiconductor

CD40174BM/CD40174BC Hex D Flip-Flop
CD40175BM/CD40175BC Quad D Flip-Flop

general description

The CD40174B consists of six positive-edge triggered D-type flip-flops; the true output from each flip-flop are externally available. The CD40175B consists of four positive-edge triggered D-type flip-flops; both the true and complement outputs from each flip-flop are externally available.

All flip-flops are controlled by a common clock and a common clear. Information at the D inputs meeting the set-up time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. The clearing operation, enabled by a negative pulse at Clear input, clears all Q outputs to logical "0" and $\overline{Q}$'s (CD40175B only) to logical "1."

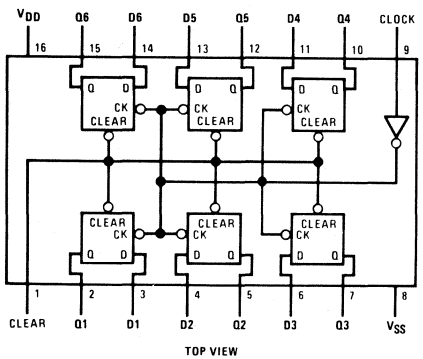
All inputs are protected from static discharge by diode clamps to V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Equivalent to MC14174B, MC14175B
- Equivalent to MM74C174, MM74C175

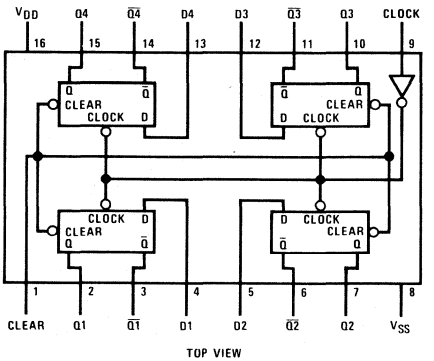
connection diagrams

CD40174B
Dual-In-Line Package



TOP VIEW

CD40175B
Dual-In-Line Package



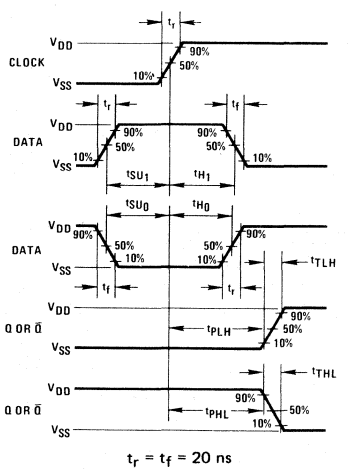
TOP VIEW

truth table

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$*
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	H	X	NC	NC
H	L	X	NC	NC

H = High level
L = Low level
X = Irrelevant
↑ = Transition from low to high level
NC = No change
* = $\overline{Q}$ for CD40175B only

switching time waveforms



$t_r = t_f = 20$ ns

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40XXXBM	−55°C to +125°C
CD40XXXBC	−40°C to +85°C

dc electrical characteristics CD40174BM, CD40175BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0			1.0		30	μA
		V_{DD} = 10V		2.0			2.0		60	μA
		V_{DD} = 15V		4.0			4.0		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}			−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}			1.0	μA

dc electrical characteristics CD40174BC, CD40175BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		8.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.41	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−8.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF $R_L = 200k$, and $t_r = t_f = 20$ ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL} or t_{PLH}	Propagation Delay Time to a Logical "0" or Logical "1" from Clock to Q or $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		190	300	ns
		$V_{DD} = 10V$		75	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PHL}	Propagation Delay Time to a Logical "0" from Clear to Q	$V_{DD} = 5V$		180	300	ns
		$V_{DD} = 10V$		70	110	ns
		$V_{DD} = 15V$		60	90	ns
t_{PLH}	Propagation Delay Time to a Logical "1" from Clear to $\overline{Q}$ (CD40175 Only)	$V_{DD} = 5V$		230	400	ns
		$V_{DD} = 10V$		90	150	ns
		$V_{DD} = 15V$		75	120	ns
t_{SU}	Time Prior to Clock Pulse that Data must be Present	$V_{DD} = 5V$	100	45		ns
		$V_{DD} = 10V$	40	16		ns
		$V_{DD} = 15V$	35	13		ns
t_H	Time after Clock Pulse that Data must be Held	$V_{DD} = 5V$		−11	0	ns
		$V_{DD} = 10V$		−4	0	ns
		$V_{DD} = 15V$		−3	0	ns
t_{THL} or t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}, t_{WL}	Minimum Clock Pulse Width	$V_{DD} = 5V$		130	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}	Minimum Clear Pulse Width	$V_{DD} = 5V$		120	250	ns
		$V_{DD} = 10V$		45	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{RCL}	Maximum Clock Rise Time	$V_{DD} = 5V$	15	450		μs
		$V_{DD} = 10V$	5.0	125		μs
		$V_{DD} = 15V$	5.0	125		μs
t_{fCL}	Maximum Clock Fall Time	$V_{DD} = 5V$	15	50		μs
		$V_{DD} = 10V$	5.0	50		μs
		$V_{DD} = 15V$	5	50		μs
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	2.0	3.5		MHz
		$V_{DD} = 10V$	5.0	10		MHz
		$V_{DD} = 15V$	6.0	12		MHz
C_{IN}	Input Capacitance	Clear Input,		10	15	pF
		Other Input		5.0	7.5	pF
C_{PD}	Power Dissipation	Per Package, (Note 3)		130		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

National Semiconductor

CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

general description

These up/down counters are monolithic complementary MOS (CMOS) integrated circuits. The CD40192BM and CD40192BC are BCD counters. While the CD40193BM and CD40193BC are binary counters.

Counting up and counting down is performed by two count inputs, one being held high while the other is clocked. The outputs change on the positive-going transition of this clock.

These counters feature preset inputs that are enabled when load is a logical "0" and a clear which forces all outputs to "0" when it is at logical "1". The counters also have carry and borrow outputs so that they can be cascaded using no external circuitry.

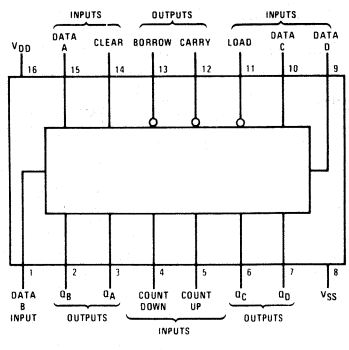
All inputs are protected against damage due to static discharge by clamps to V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Carry and borrow outputs for easy expansion to N-bit by cascading
- Asynchronous clear
- Equivalent to — MM54C192/MM74C192 and MM54C193/MM74C193

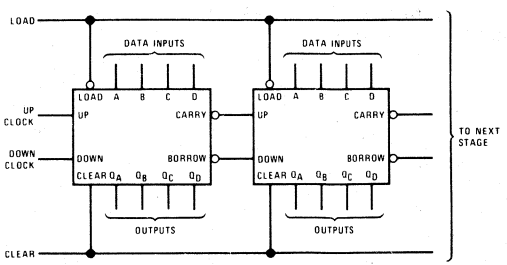
connection diagram

Dual-In-Line Package



TOP VIEW

cascading packages



absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature, (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD40192BM, CD40193BM	−55°C to +125°C
CD40192BC, CD40193BC	−40°C to +85°C

dc electrical characteristics (Note 2) CD40192BM, CD40193BM

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics (Note 2) CD40192BC, CD40193BC

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95			4.95		V
		V_{DD} = 10V	9.95		9.95			9.95		V
		V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200K\Omega$, $t_r = t_f = 20$ns, unless otherwise specified.

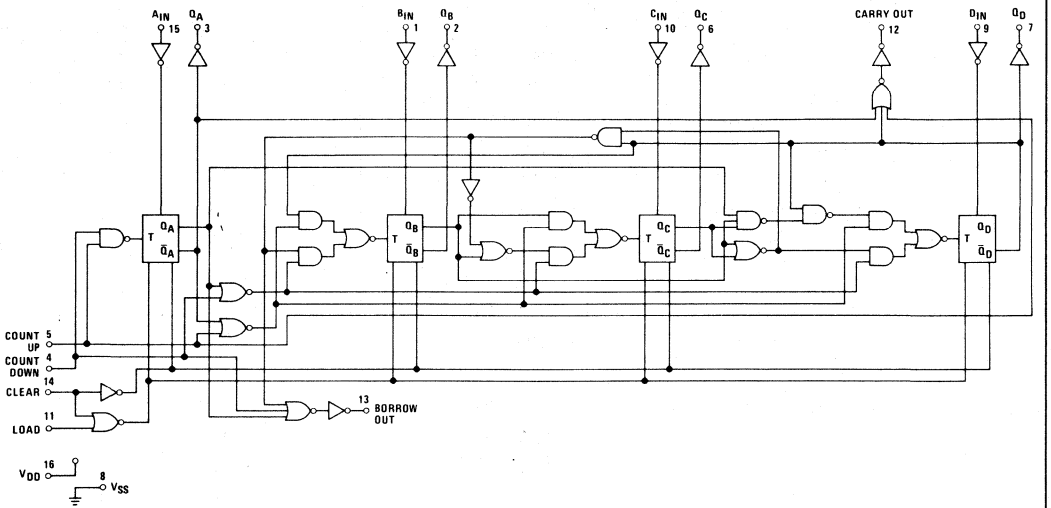
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up Or Count Down To Q	$V_{DD} = 5V$		250	400	ns
		$V_{DD} = 10V$		100	160	ns
		$V_{DD} = 15V$		80	130	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Up To Carry	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Count Down To Borrow	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		50	80	ns
		$V_{DD} = 15V$		40	65	ns
t_{SU}	Time Prior To Load That Data Must Be Present	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		30	50	ns
		$V_{DD} = 15V$		25	40	ns
t_{PHL}	Propagation Delay Time From Clear To Q	$V_{DD} = 5V$		130	220	ns
		$V_{DD} = 10V$		60	100	ns
		$V_{DD} = 15V$		50	80	ns
t_{PLH} or t_{PHL}	Propagation Delay Time From Load To Q	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{TLH} or t_{THL}	Output Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Count Frequency	$V_{DD} = 5V$	2.5	4		MHz
		$V_{DD} = 10V$	6	10		MHz
		$V_{DD} = 15V$	7.5	12.5		MHz
t_{RCL} or t_{fCL}	Maximum Count Rise Or Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	5			μs
		$V_{DD} = 15V$	2			μs
t_{WH}, t_{WL}	Minimum Count Pulse Width	$V_{DD} = 5V$		120	200	ns
		$V_{DD} = 10V$		35	80	ns
		$V_{DD} = 15V$		28	65	ns
t_{WH}	Minimum Clear Pulse Width	$V_{DD} = 5V$		300	480	ns
		$V_{DD} = 10V$		120	190	ns
		$V_{DD} = 15V$		95	150	ns
t_{WL}	Minimum Load Pulse Width	$V_{DD} = 5V$		100	160	ns
		$V_{DD} = 10V$		40	65	ns
		$V_{DD} = 15V$		32	55	ns
C_{IN}	Average Input Capacitance	Load and Data Inputs (A,B,C,D)		5	7.5	pF
		Count Up, Count Down and Clear		10	15	pF
C_{PD}	Power Dissipation Capacity	(Note 3)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

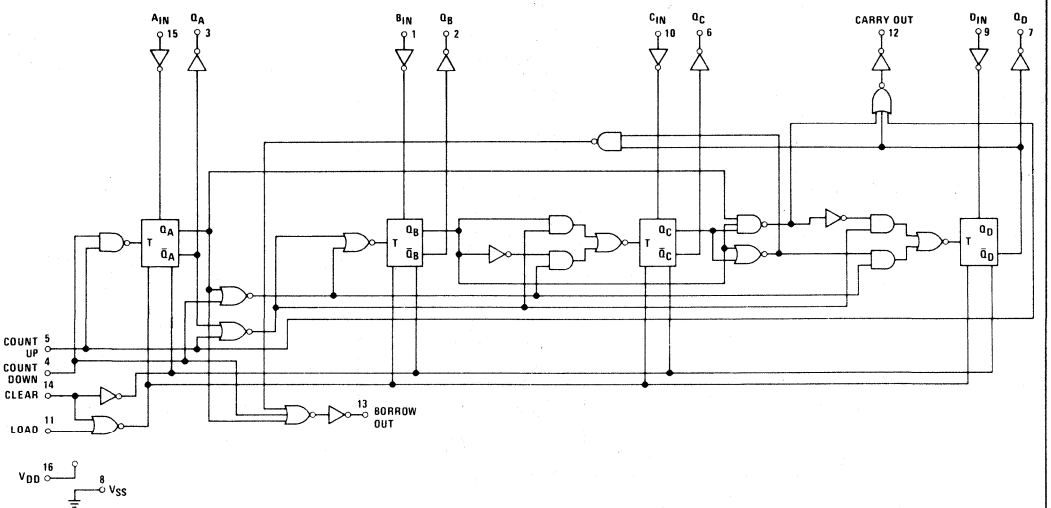
Note 2: $V_{SS} = 0V$ unless otherwise specified.

Note 3: C_{PD} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

schematic diagrams

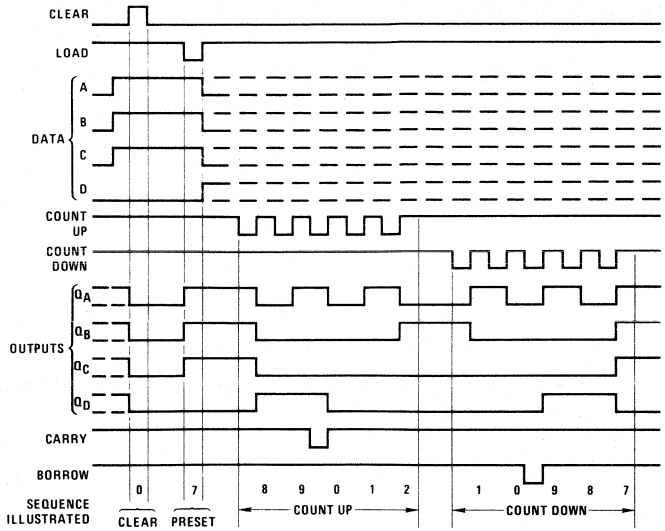


CD40192BM/CD40192BC Synchronous 4-Bit Up/Down Decade Counter



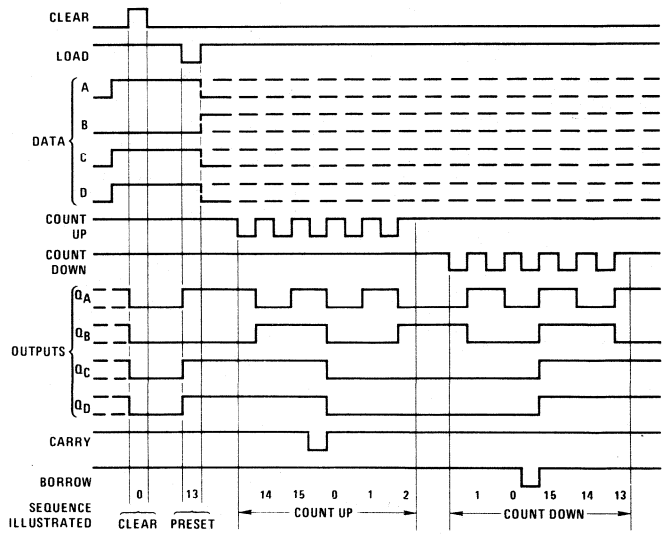
CD40193BM/CD40193BC Synchronous 4-Bit Up/Down Binary Counter

timing diagrams



Sequence:
1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one and two.
4. Count down to one, zero, borrow, nine, eight and seven.

CD40192BM/CD40192BC



Sequence:
1. Clear outputs to zero.
2. Load (preset) to binary thirteen.
3. Count up to fourteen, fifteen, carry, zero, one and two.
4. Count down to one, zero, borrow, fifteen, fourteen and thirteen.

CD40193BM/CD40193BC

National Semiconductor

CD4503BM/CD4503BC Hex Non-Inverting TRI-STATE® Buffer

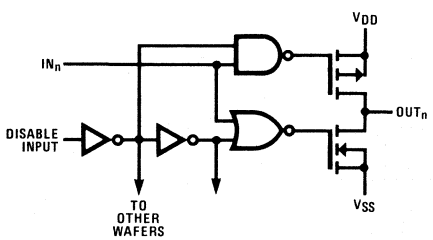
general description

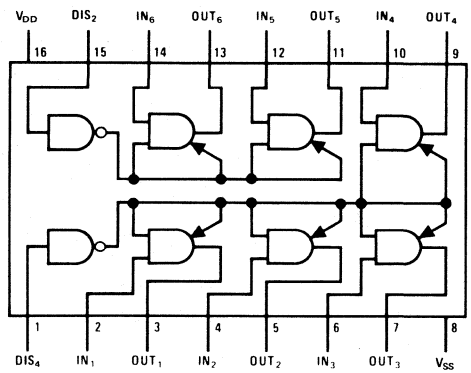
The CD4503B is a hex non-inverting TRI-STATE® buffer with high output current sink and source capability. TRI-STATE outputs make it useful in bus oriented applications. Two separate disable inputs are provided. Buffers 1 through 4 are controlled by the disable 4 input. Buffers 5 and 6 are controlled by the disable 2 input. A high level on either disable input will cause those gates on its control line to go into a high impedance state.

features

- Wide supply voltage range 3.0V_{DC} to 18V_{DC}
- TRI-STATE outputs
- Symmetrical turn on/turn off delays
- Symmetrical output rise and fall times
- Pin-for-pin replacement for MM80C97 and MC14503

schematic and connection diagrams





TOP VIEW

truth table

In	Disable Input	Out
0	0	0
1	0	1
X	1	TRI-STATE

X = Don't Care

absolute maximum ratings

(Notes 1 and 2)

V_{DD} – Supply Voltage	−0.5V to +18V
V_{IN} – Input Voltage	−0.5V to +0.5V
T_S – Storage Temperature Range	−65°C to +150°C
P_D – Power Dissipation	500 mW
T_L – Lead Temperature (soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} – Supply Voltage	3V to 15V
T_A – Operating Temperature Range	
CD4503BM	−55°C to +125°C
CD4503BC	−40°C to +85°C

dc electrical characteristics CD4503BM (Note 2)

Parameter	Conditions	−55°C		+25°C			+125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		1			1		30	μA
	V_{DD} = 10V		2			2		60	μA
	V_{DD} = 15V		4			4		120	μA
V_{OL} Low Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V	4.95		4.95	5		4.95		V
	V_{DD} = 10V	9.95		9.95	10		9.95		V
	V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Input Current	V_{DD} = 4.5V, V_{OL} = 0.4V	2.80		2.30	2.55		1.60		mA
	V_{DD} = 5.0V, V_{OL} = 0.4V	3.00		2.40	2.75		1.75		mA
	V_{DD} = 10V, V_{OL} = 0.5V	7.85		6.35	7.00		4.45		mA
	V_{DD} = 15V, V_{OL} = 1.5V	19.95		16.10	25.00		11.30		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_{OH} = 4.6V	−1.28		−1.02	−1.76		−0.72		mA
	V_{DD} = 10V, V_{OH} = 9.5V	−3.20		−2.60	−4.5		−1.8		mA
	V_{DD} = 15V, V_{OH} = 13.5V	−8.20		−6.80	−17.6		−4.8		mA
I_{OZ} TRI-STATE Leakage Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA
I_{IN} Input Current	V_{DD} = 15V		±0.1		$\pm 10^{-4}$	±0.1		±1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

dc electrical characteristics CD4503BC (Note 2)

Parameter	Conditions	−40°C		+25°C			+85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		4		4			30	μA
	V_{DD} = 10V		8		8			60	μA
	V_{DD} = 15V		16		16			120	μA
V_{OL} Low Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V		0.05		0	0.05		0.05	V
	V_{DD} = 10V		0.05		0	0.05		0.05	V
	V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH} High Level Output Voltage	V_{IN} = V_{DD} or 0								
	V_{DD} = 5V	4.95		4.95			4.95		V
	V_{DD} = 10V	9.95		9.95			9.95		V
	V_{DD} = 15V	14.95		14.95			14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 4.5V or 0.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 9.0V or 1.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 13.5V or 1.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.5		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Input Current	V_{DD} = 4.5V, V_{OL} = 0.4V	2.30		1.95	2.65		1.60		mA
	V_{DD} = 5.0V, V_{OL} = 0.4V	2.5		2.10	2.75		1.75		mA
	V_{DD} = 10V, V_{OL} = 0.5V	6.5		5.45	7.0		4.45		mA
	V_{DD} = 15V, V_{OL} = 1.5V	16.50		13.80	25.00		11.30		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_{OH} = 4.6V	−1.04		−0.88	−1.76				mA
	V_{DD} = 10V, V_{OH} = 9.5V	−2.60		−2.2	−4.50				mA
	V_{DD} = 15V, V_{OH} = 13.5V	−7.2		−6.0	−17.6				mA
I_{TL} TRI-STATE Leakage Current	V_{DD} = 15V		±0.3		$\pm 10^{-4}$	±0.3		±1.0	μA
I_{IN} Input Current	V_{DD} = 15V		±0.3		$\pm 10^{-5}$	±0.3		±1.0	

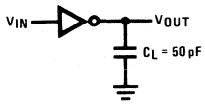
ac electrical characteristics CD4503B

T_A = 25°C, C_L = 50 pF, R_L = 200 kΩ, Input t_r = t_f = 20 ns, unless otherwise specified.

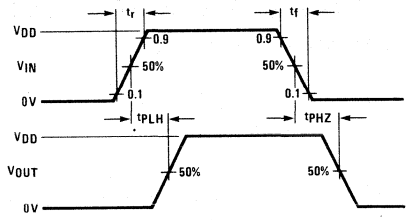
Parameter		Conditions	Min	Typ	Max	Units
t_{PHL}, t_{PLH}	Propagation Delay Time	V_{DD} = 5V		75	100	ns
		V_{DD} = 10V		35	40	ns
		V_{DD} = 15V		25	30	ns
t_{PLZ}, t_{PHZ}	Propagation Delay Time, Logical Level to High Impedance State	V_{DD} = 5V		80	125	ns
		V_{DD} = 10V		40	90	ns
		V_{DD} = 15V		35	70	ns
t_{PZL}, t_{PZH}	Propagation Delay Time, High Impedance State to Logical Level	V_{DD} = 5V		95	175	ns
		V_{DD} = 10V		40	80	ns
		V_{DD} = 15V		35	70	ns
t_{TLH}	Output Rise Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns
t_{THL}	Output Fall Time	V_{DD} = 5V		45	80	ns
		V_{DD} = 10V		23	40	ns
		V_{DD} = 15V		18	35	ns

ac test circuits and switching time waveforms

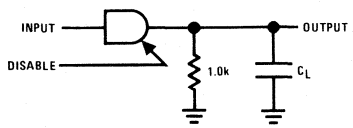
t_{PHL}, t_{PLH}



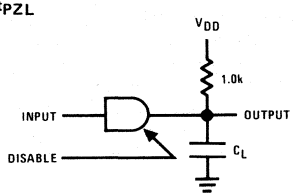
CMOS to CMOS



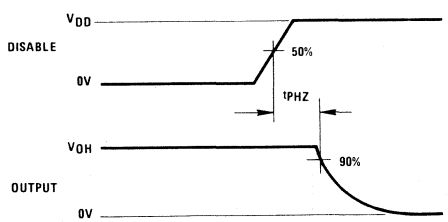
t_{PHZ} and t_{PZH}



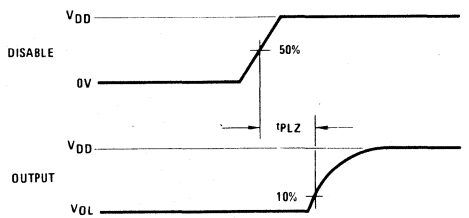
t_{PLZ} and t_{PZL}



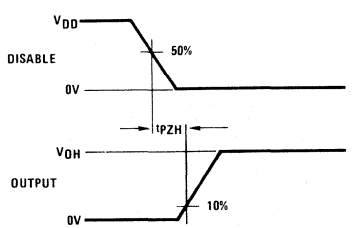
t_{PHZ}



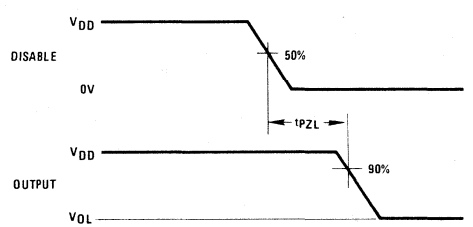
t_{PLZ}



t_{PZH}



t_{PZL}



Note: Delays measured with input t_r, $t_f \leq 20$ ns.

National Semiconductor

CD4510BM/CD4510BC BCD Up/Down Counter
CD4516BM/CD4516BC Binary Up/Down Counter

general description

The CD4510BM/CD4510BC and CD4516BM/CD4516BC are monolithic CMOS up/down counters which count in BCD and binary, respectively.

The counters count up when the up/down input is at logical "1" and vise versa. A logical "1" preset enable signal allows information at the parallel inputs to preset the counters to any state asynchronously with the clock. The counters are advanced one count at the positive-going edge of the clock if the carry in, preset enable, and reset inputs are at logical "0". Advancement is inhibited when any of these three inputs are at logical "1". The carry out signal is normally at logical "1" state and goes to logical "0" when the counter reaches its maximum count in the "up" mode or its minimum count in the "down" mode, provided the carry input is at logical "0" state. The counters are cleared asynchronously by applying a logical "1" voltage level at the reset input.

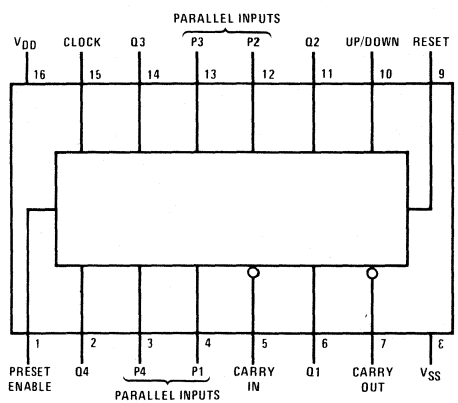
All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Parallel load "jam" inputs
- Low quiescent power dissipation — 0.25 μW/package typ @ V_{CC} = 5V
- Motorola MC14510, MC14516 second source

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

truth table

CLOCK	RESET	PRESET ENABLE	CARRY IN	UP/DOWN	OUTPUT FUNCTION
X	1	X	X	X	Reset to zero
X	0	1	X	X	Set to P1, P2, P3, P4
⎍	0	0	0	1	Count up
⎍	0	0	0	0	Count down
⎎	0	0	X	X	No change
X	0	0	1	X	No change

⎍ = positive transition
⎎ = negative transition
X = don't care

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

dc electrical characteristics CD4510BM, CD4516BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.05	5		150	μA
		V_{DD} = 10V		10		0.1	10		300	μA
		V_{DD} = 15V		20		0.15	20		600	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1$ μA								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4510BC, CD4516BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.05	20		150	μA
		V_{DD} = 10V		40		0.1	40		300	μA
		V_{DD} = 15V		80		0.15	80		600	μA
V_{OL}	Low Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$V_{IH} = V_{DD}$, V_{IL} = 0V, $\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (Continued) CD4510BC, CD4516BC (Note 2)

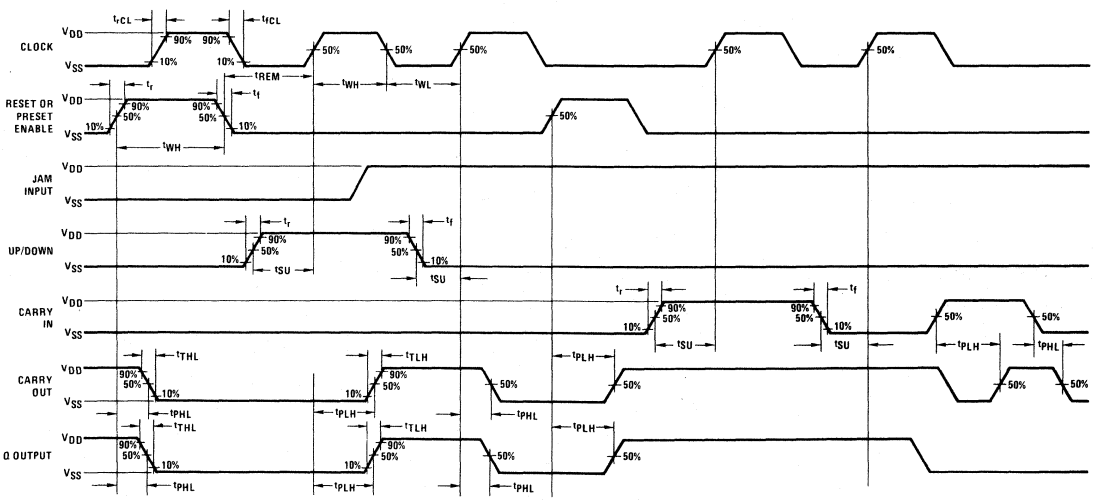
PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.8		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.0		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	7.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.8		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.0		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−7.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed, they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Devices should not be connected while power is "ON."

switching time waveforms



ac electrical characteristics CD4510BM/CD4510BC, CD4516BM/CD4516BC

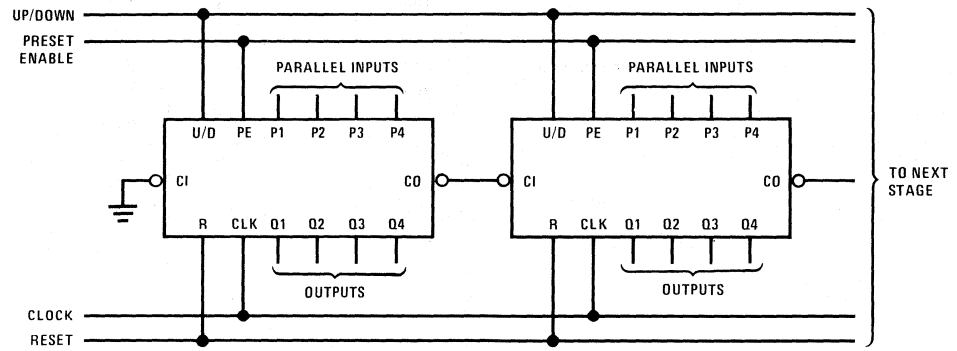
$T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k$, $t_{rCL} = t_{fCL} = t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CLOCKED OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Q Outputs	$V_{DD} = 5V$		220	500	ns
		$V_{DD} = 10V$		100	200	ns
		$V_{DD} = 15V$		80	180	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Clock to Carry Output	$V_{DD} = 5V$		315	630	ns
		$V_{DD} = 10V$		130	260	ns
		$V_{DD} = 15V$		100	200	ns
t_{THL}, t_{TLH}	Transition Time Q and Carry Outputs	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		160	315	ns
		$V_{DD} = 10V$		65	130	ns
		$V_{DD} = 15V$		50	100	ns
t_{rCL}, t_{fCL}	Maximum Clock Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	15			μs
		$V_{DD} = 15V$	15			μs
t_{SU}	Minimum Carry In Set-Up Time	$V_{DD} = 5V$		100	220	ns
		$V_{DD} = 10V$		40	80	ns
		$V_{DD} = 15V$		35	70	ns
t_{SU}	Minimum Up/Down Set-Up Time	$V_{DD} = 5V$		200	420	ns
		$V_{DD} = 10V$		70	170	ns
		$V_{DD} = 15V$		60	150	ns
f_{CL}	Maximum Clock Frequency	$V_{DD} = 5V$	1.5	3.1		MHz
		$V_{DD} = 10V$	3.8	7.6		MHz
		$V_{DD} = 15V$	5.0	10.0		MHz
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance (Note 4)	Per Package,		65		pF
RESET/PRESET ENABLE OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Q Output	$V_{DD} = 5V$		285	570	ns
		$V_{DD} = 10V$		115	230	ns
		$V_{DD} = 15V$		95	195	ns
t_{PHL}, t_{PLH}	Propagation Delay Time Reset/ Preset Enable to Carry Output	$V_{DD} = 5V$		420	860	ns
		$V_{DD} = 10V$		170	350	ns
		$V_{DD} = 15V$		140	290	ns
t_{WH}	Minimum Reset/Preset Enable Pulse Width	$V_{DD} = 5V$		90	200	ns
		$V_{DD} = 10V$		40	100	ns
		$V_{DD} = 15V$		35	80	ns
t_{REM}	Minimum Reset/Preset Enable Removal Time	$V_{DD} = 5V$		170	330	ns
		$V_{DD} = 10V$		70	140	ns
		$V_{DD} = 15V$		60	120	ns
CARRY INPUT OPERATION						
t_{PHL}, t_{PLH}	Propagation Delay Time Carry In to Carry Output	$V_{DD} = 5V$		260	500	ns
		$V_{DD} = 10V$		110	220	ns
		$V_{DD} = 15V$		90	180	ns

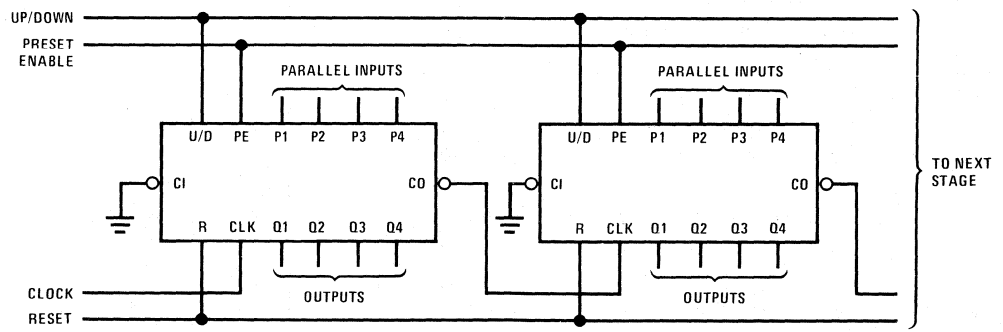
Note 4: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L)V_{DD}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; P_Q = Quiescent Power Dissipation. For further details, see application note AN-90, "54C/74C Family characteristics."

cascading packages

Parallel Clocking



Ripple Clocking



schematic diagrams

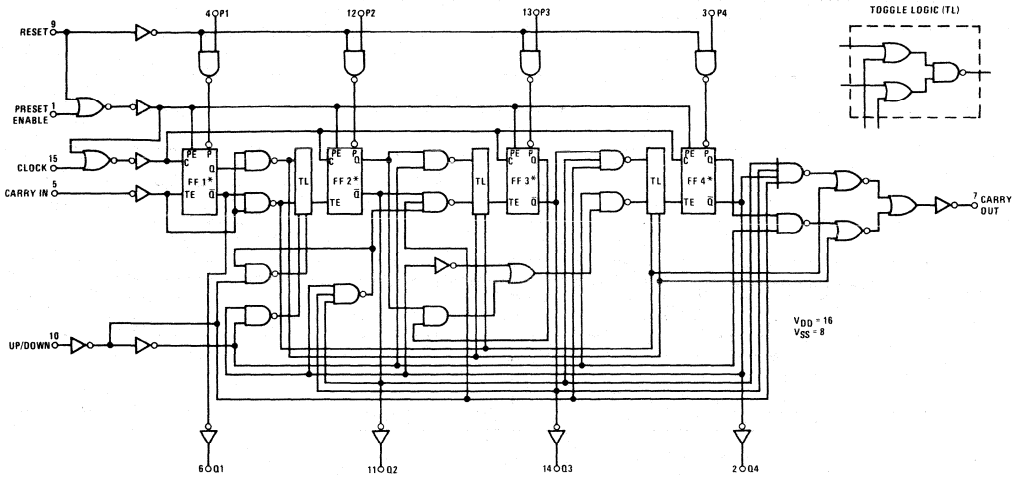
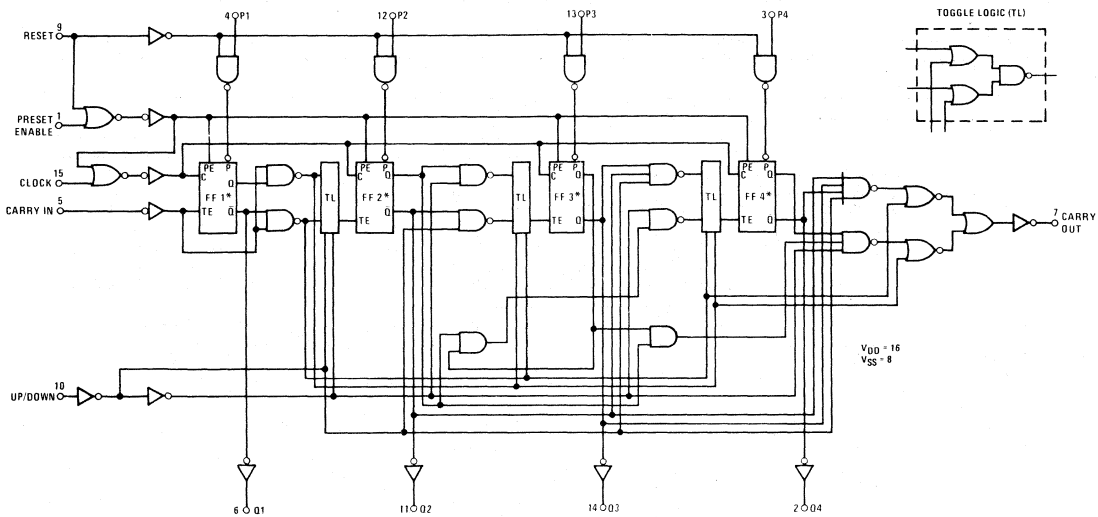


FIGURE 1. CD4510

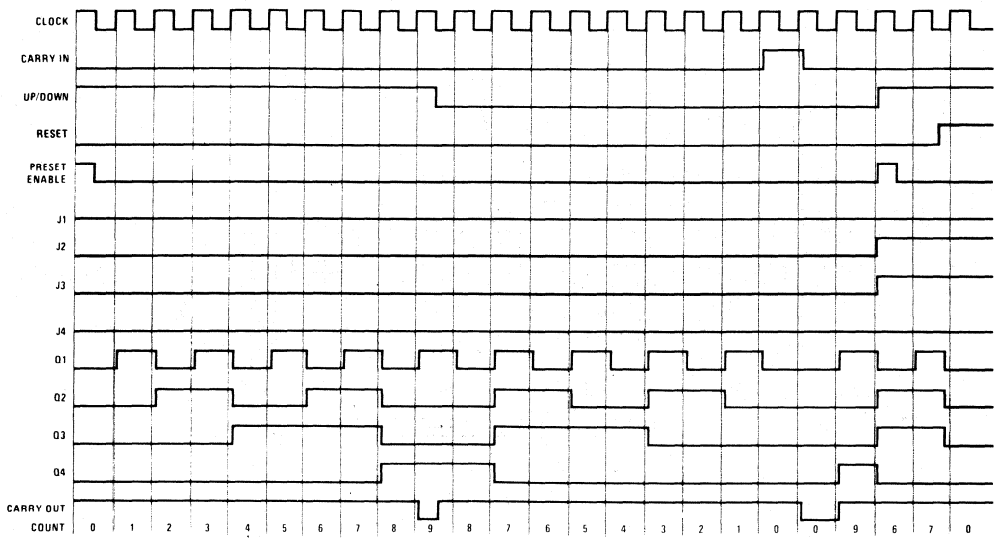


*Flip-flop toggles at the positive-going edge of clock (C) if Toggle Enable (TE) is at logical "1" and Preset Enable (PE) is at logical "0"

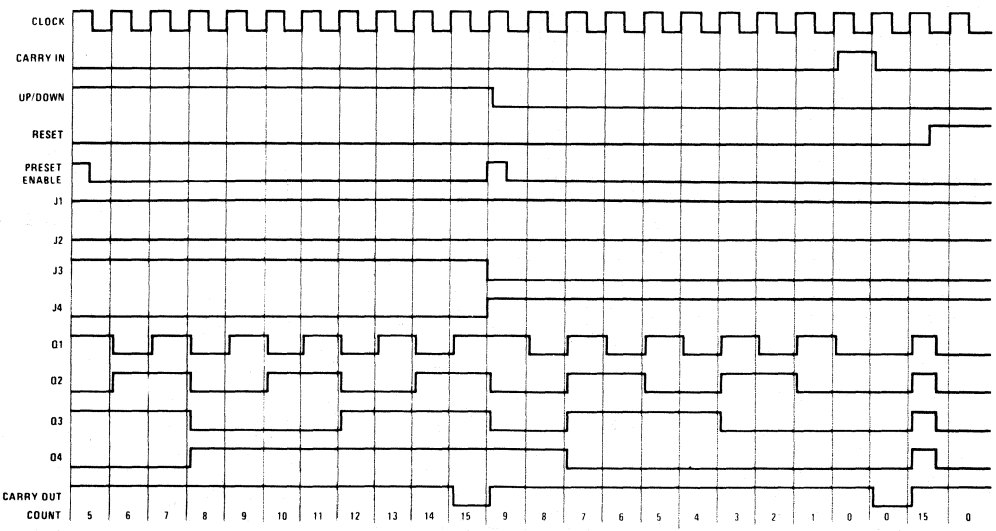
FIGURE 2. CD4516

logic waveforms

CD4510BM/CD4510BC



CD4516BM/CD4516BC



National Semiconductor

CD4511BM/CD4511BC BCD-to-7 Segment Latch/Decoder/Driver

general description

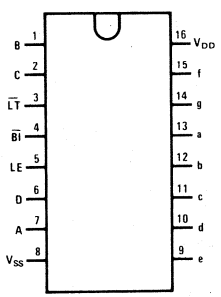
The CD4511BM/CD4511BC BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and an output drive capability. Lamp test (LT), blanking (BI), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

features

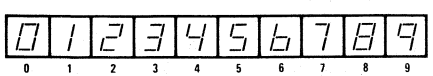
- Low logic circuit power dissipation
- High current sourcing outputs (up to 25 mA)
- Latch storage of code
- Blanking input
- Lamp test provision
- Readout blanking on all illegal input combinations
- Lamp intensity modulation capability
- Time share (multiplexing) facility
- Equivalent to Motorola MC14511

connection diagram

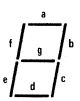


TOP VIEW

Display



Segment Identification



truth table

INPUTS							OUTPUTS							
LE	$\overline{BI}$	$\overline{LT}$	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	
0	1	1	1	0	1	1	0	0	0	0	0	0	0	
0	1	1	1	1	0	0	0	0	0	0	0	0	0	
0	1	1	1	1	0	1	0	0	0	0	0	0	0	
0	1	1	1	1	1	0	0	0	0	0	0	0	0	
0	1	1	1	1	1	1	0	0	0	0	0	0	0	
1	1	1	X	X	X	X				*				

X = Don't care

*Depends upon the BCD code applied during the 0 to 1 transition of LE.

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} +0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4510BM, CD4516BM	−55°C to +125°C
CD4510BC, CD4516BC	−40°C to +85°C

dc electrical characteristics CD4511BM

PARAMETER	CONDITIONS	−55°C			+25°C			+125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V	14.1			14.1	14.59		14.1			V
Low Level Input Voltage (V_{IL})	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V			1.5		2	1.5			1.5	V
	V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V			3.0		4	3.0			3.0	V
	V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V			4.0		6	4.0			4.0	V
High Level Input Voltage (V_{IH})	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5			3.5	3		3.5			V
	V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0			7.0	6		7.0			V
	V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0			11.0	9		11.0			V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0mA	4.1			4.1	4.57		4.1			V
	V_{DD} = 5V, I_{OH} = 5mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10mA	3.9			3.9	4.12		3.5			V
	V_{DD} = 5V, I_{OH} = 15mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20mA	3.4			3.4	3.75		3.0			V
	V_{DD} = 5V, I_{OH} = 25mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0mA	9.1			9.1	9.58		9.1			V
	V_{DD} = 10V, I_{OH} = 5mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10mA	9.0			9.0	9.17		8.6			V
	V_{DD} = 10V, I_{OH} = 15mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20mA	8.6			8.6	8.9		8.2			V
	V_{DD} = 10V, I_{OH} = 25mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0mA	14.1			14.1	14.59		14.1			V
	V_{DD} = 15V, I_{OH} = 5mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10mA	14.0			14.0	14.18		13.6			V
	V_{DD} = 15V, I_{OH} = 15mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20mA	13.6			13.6	13.95		13.2			V
	V_{DD} = 15V, I_{OH} = 25mA					13.8					V
Low Level Output Current (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.64			0.51	0.88		0.36			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.6			1.3	2.25		0.9			mA
	V_{DD} = 15V, V_{OL} = 1.5V	4.2			3.4	8.8		2.4			mA
Input Current (I_{IN})	V_{DD} = 15V, V_{IN} = 0V			−0.10		-10^{-5}	−0.10			−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V			0.10		10^{-5}	0.10			1.0	μA

Note 1: Devices should not be connected with power on.

dc electrical characteristics CD4511BC

PARAMETER	CONDITIONS	−40°C			+25°C			+85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage Logical "0" Level (V_{OUT})	V_{DD} = 5V			0.01		0	0.01			0.05	V
	V_{DD} = 10V			0.01		0	0.01			0.05	V
	V_{DD} = 15V					0					V
Output Voltage Logical "1" Level (V_{OUT})	V_{DD} = 5V	4.1			4.1	4.57		4.1			V
	V_{DD} = 10V	9.1			9.1	9.58		9.1			V
	V_{DD} = 15V	14.1			14.1	14.59		14.1			V
Low Level Input Voltage (V_{IL})	V_{DD} = 5V, V_{OUT} = 3.8V or 0.5V			1.5		2	1.5			1.5	V
	V_{DD} = 10V, V_{OUT} = 8.8V or 1.0V			3.0		4	3.0			3.0	V
	V_{DD} = 15V, V_{OUT} = 13.8V or 1.5V			4.0		6	4.0			4.0	V
High Level Input Voltage (V_{IH})	V_{DD} = 5V, V_{OUT} = 0.5V or 3.8V	3.5			3.5	3		3.5			V
	V_{DD} = 10V, V_{OUT} = 1.0V or 8.8V	7.0			7.0	6		7.0			V
	V_{DD} = 15V, V_{OUT} = 1.5V or 13.8V	11.0			11.0	9		11.0			V
Output (Source) Drive Voltage (V_{OH})	V_{DD} = 5V, I_{OH} = 0 mA	4.1			4.1	4.57		4.1			V
	V_{DD} = 5V, I_{OH} = 5 mA					4.24					V
	V_{DD} = 5V, I_{OH} = 10 mA	3.6			3.6	4.12		3.3			V
	V_{DD} = 5V, I_{OH} = 15 mA					3.94					V
	V_{DD} = 5V, I_{OH} = 20 mA	2.8			2.8	3.75		2.5			V
	V_{DD} = 5V, I_{OH} = 25 mA					3.54					V
	V_{DD} = 10V, I_{OH} = 0 mA	9.1			9.1	9.58		9.1			V
	V_{DD} = 10V, I_{OH} = 5 mA					9.26					V
	V_{DD} = 10V, I_{OH} = 10 mA	8.75			8.75	9.17		8.45			V
	V_{DD} = 10V, I_{OH} = 15 mA					9.04					V
	V_{DD} = 10V, I_{OH} = 20 mA	8.1			8.1	8.9		7.8			V
	V_{DD} = 10V, I_{OH} = 25 mA					8.75					V
	V_{DD} = 15V, I_{OH} = 0 mA	14.1			14.1	14.59		14.1			V
	V_{DD} = 15V, I_{OH} = 5 mA					14.27					V
	V_{DD} = 15V, I_{OH} = 10 mA	13.75			13.75	14.18		13.45			V
	V_{DD} = 15V, I_{OH} = 15 mA					14.07					V
	V_{DD} = 15V, I_{OH} = 20 mA	13.1			13.1	13.95		12.8			V
	V_{DD} = 15V, I_{OH} = 25 mA					13.8					V
Low Level Output Current (I_{OL})	V_{DD} = 5V, V_{OL} = 0.4V	0.52			0.44	0.88		0.36			mA
	V_{DD} = 10V, V_{OL} = 0.5V	1.3			1.1	2.25		0.9			mA
	V_{DD} = 15V, V_{OL} = 1.5V	3.6			3.0	8.8		2.4			mA
Input Current (I_{IN})	V_{DD} = 15V, V_{IN} = 0V			−0.30		-10^{-5}	−0.30			−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V			0.30		10^{-5}	0.30			1.0	μA

ac electrical characteristics

$T_A = 25°C$ and $C_L = 50\,pF$, typical temperature coefficient for all values of $V_{DD} = 0.3\%/°C$.

PARAMETER	CONDITIONS	CD4511BX			UNITS
		MIN	TYP	MAX	
Input Capacitance (C_{IN})	$V_{IN} = 0$		5.0	7.5	pF
Output Rise Time (t_r) *(Figure 1a)*	$V_{DD} = 5V$		40	80	ns
	$V_{DD} = 10V$		30	60	ns
	$V_{DD} = 15V$		25	50	ns
Output Fall Time (t_f) *(Figure 1a)*	$V_{DD} = 5V$		125	250	ns
	$V_{DD} = 10V$		75	150	ns
	$V_{DD} = 15V$		65	130	ns
Turn-Off Delay Time (Data) (t_{PLH}) *(Figure 1a)*	$V_{DD} = 5V$		640	1280	ns
	$V_{DD} = 10V$		250	500	ns
	$V_{DD} = 15V$		175	350	ns
Turn-On Delay Time (Data) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		720	1440	ns
	$V_{DD} = 10V$		290	580	ns
	$V_{DD} = 15V$		195	400	ns
Turn-Off Delay Time (Blank) (t_{PLH}) *(Figure 1a)*	$V_{DD} = 5V$		320	640	ns
	$V_{DD} = 10V$		130	260	ns
	$V_{DD} = 15V$		100	200	ns
Turn-On Delay Time (Blank) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		485	970	ns
	$V_{DD} = 10V$		200	400	ns
	$V_{DD} = 15V$		160	320	ns
Turn-Off Delay Time (Lamp Test) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
	$V_{DD} = 10V$		125	250	ns
	$V_{DD} = 15V$		90	180	
Turn-On Delay Time (Lamp Test) (t_{PHL}) *(Figure 1a)*	$V_{DD} = 5V$		313	625	ns
	$V_{DD} = 10V$		125	250	ns
	$V_{DD} = 15V$		90	180	ns
Setup Time (t_{SETUP}) *(Figure 1b)*	$V_{DD} = 5V$	180	90		ns
	$V_{DD} = 10V$	76	38		ns
	$V_{DD} = 15V$	40	20		ns
Hold Time (t_{HOLD}) *(Figure 1b)*	$V_{DD} = 5V$	0	−90		ns
	$V_{DD} = 10V$	0	−38		ns
	$V_{DD} = 15V$	0	−20		ns
Minimum Latch Enable Pulse Width (PW_{LE}) *(Figure 1c)*	$V_{DD} = 5V$	520	260		ns
	$V_{DD} = 10V$	220	110		ns
	$V_{DD} = 15V$	130	65		ns

switching time waveforms

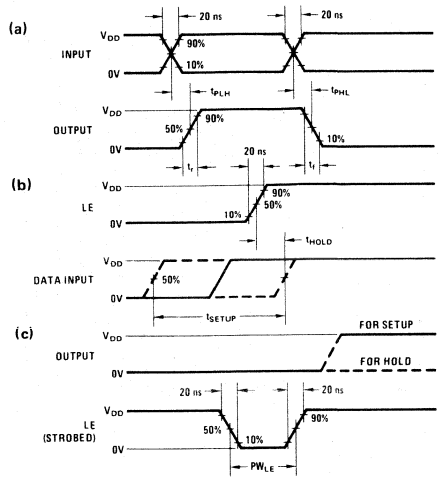
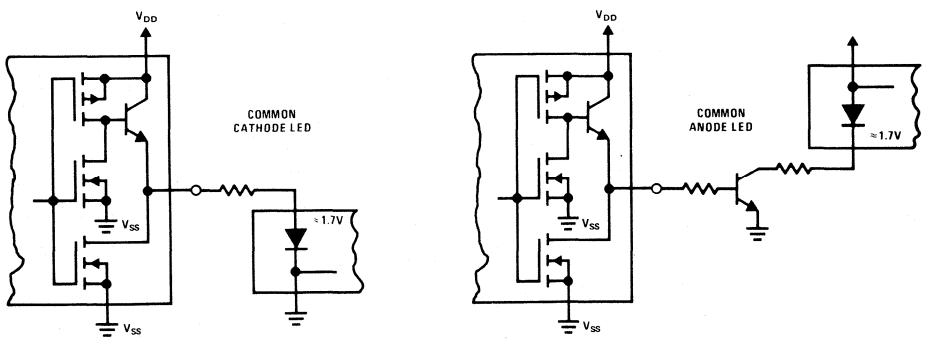


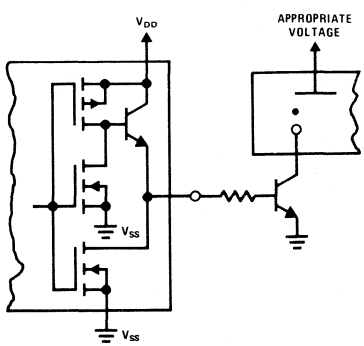
FIGURE 1.

typical applications

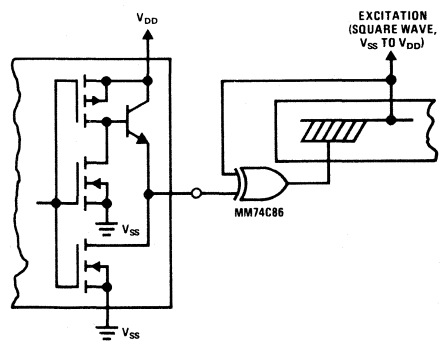
Light Emitting Diode (LED) Readout



Gas Discharge Readout



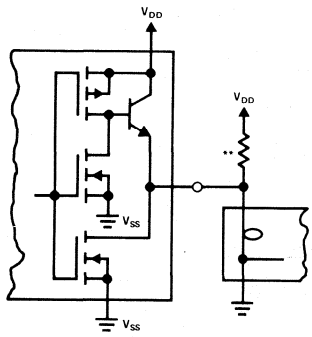
Liquid Crystal (LC) Readout



Direct dc drive of LC's not recommended for life of LC readouts.

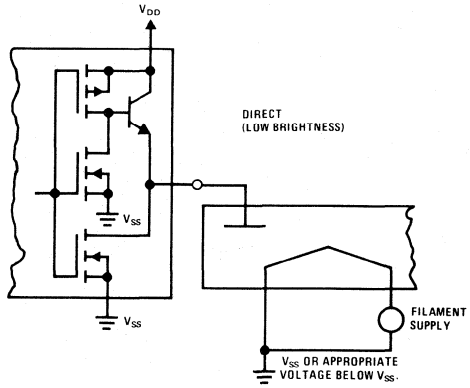
typical applications continued

Incandescent Readout



**A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Fluorescent Readout



National Semiconductor

CD4512M/CD4512C 8-Channel Data Selector

General Description

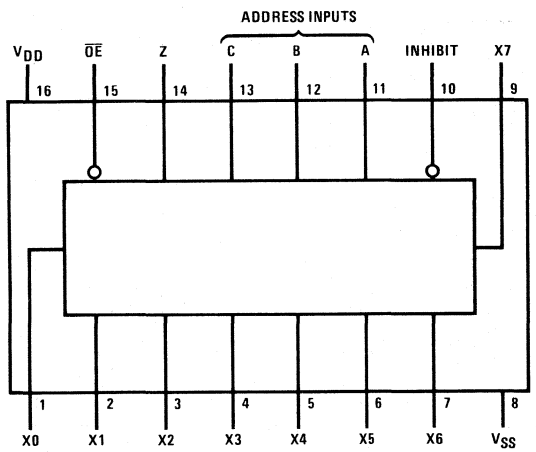
The CD4512M/CD4512C 8-channel data selector is a complementary MOS (CMOS) circuit constructed with N and P-channel enhancement mode transistors. This data selector is primarily used as a digital signal multiplexer selecting 1 of 8 inputs and routing the signal to a TRI-STATE® output. A high level at the Inhibit input forces a low level at the output. A high level at the Output Enable ($\overline{OE}$) input forces the output into the TRI-STATE condition. Low Levels at both the Inhibit and $\overline{OE}$ inputs allow normal operation.

Features

- Wide supply voltage range — 3V–15V
- High noise immunity — 0.45 V_{DD} typ
- TRI-STATE output
- Low quiescent power dissipation — 0.25 μW/package typ @ V_{CC} = 5V
- Plug in replacement for Motorola MC14512

Connection Diagram and Truth Table

Dual-In-Line Package



TOP VIEW

ADDRESS INPUTS			CONTROL INPUTS		OUTPUT
C	B	A	INHIBIT	$\overline{OE}$	Z
0	0	0	0	0	X0
0	0	1	0	0	X1
0	1	0	0	0	X2
0	1	1	0	0	X3
1	0	0	0	0	X4
1	0	1	0	0	X5
1	1	0	0	0	X6
1	1	1	0	0	X7
Ø	Ø	Ø	1	0	0
Ø	Ø	Ø	Ø	1	Hi-Z

Ø = Don't care
Hi-Z = TRI-STATE condition
Xn = Data at input n

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} + 0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4512M	−55°C to +125°C
CD4512C	−40°C to +85°C

DC Electrical Characteristics CD4512M (Note 2)

	PARAMETER	CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.010	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.50		0.40	0.78		0.28		mA
		V_{DD} = 10V, V_O = 0.5V	1.1		0.90	2.0		0.65		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	7.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 2.5V	−0.62		−0.50	−1.7		−0.35		mA
		V_{DD} = 10V, V_O = 9.5V	−0.62		−0.50	−0.9		−0.35		mA
		V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
I_{OZ}	TRI-STATE Output Current	V_{DD} = 15V, V_O = 0V or 15V		±0.1		-10^{-5} 10^{-5}	±0.1		±3	μA

DC Electrical Characteristics CD4512C (Note 2)

	PARAMETER	CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 13.5V	11.0		11.0	8.25		11.0		V

DC Electrical Characteristics CD4512C (Note 2) (Continued)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.23		0.20	0.78		0.16		mA
		V_{DD} = 10V, V_O = 0.5V	0.60		0.50	2.0		0.40		mA
		V_{DD} = 15V, V_O = 1.5V	1.8		1.5	7.8		1.2		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 2.5V	−0.23		−0.20	−1.7		−0.16		mA
		V_{DD} = 10V, V_O = 9.5V	−0.23		−0.20	−0.9		−0.16		mA
		V_{DD} = 15V, V_O = 13.5V	−0.69		−0.60	−3.5		−0.48		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
I_{OZ}	TRI-STATE Output Current	V_{DD} = 15V, V_O = 0V or 15V		±1		$\pm10^{-5}$	±1		±7.5	μA

AC Electrical Characteristics T_A = 25°C, $t_r = t_f$ = 20 ns, C_L = 15 pF

PARAMETER		CONDITIONS	CD4512M			CD4512C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PHL}	Propagation Delay	V_{DD} = 5V		225	500		225	750	ns
	High-to-Low Level	V_{DD} = 10V		75	175		75	200	ns
		V_{DD} = 15V		57	130		57	150	ns
t_{PLH}	Propagation Delay	V_{DD} = 5V		225	500		225	750	ns
	Low-to-High Level	V_{DD} = 10V		75	175		75	200	ns
		V_{DD} = 15V		57	130		57	150	ns
t_{THL}	Transition Time	V_{DD} = 5V		70	175		70	175	ns
t_{TLH}		V_{DD} = 10V		35	75		35	75	ns
		V_{DD} = 15V		25	55		25	55	ns
t_{PHZ}	Propagation Delay into	V_{DD} = 5V		50	125		50	125	ns
t_{PLZ}	TRI-STATE from Logic	V_{DD} = 15V		25	75		25	75	ns
	Level	V_{DD} = 15V		19	60		19	60	ns
t_{PZH}	Propagation Delay to	V_{DD} = 5V		50	125		50	125	ns
t_{PZL}	Logic Level from	V_{DD} = 10V		25	75		25	75	ns
	TRI STATE	V_{DD} = 15V		19	60		19	60	ns
C_{IN}	Input Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{OUT}	TRI-STATE Output Capacitance	(Note 3)		7.5	15		7.5	15	pF
C_{PD}	Power Dissipation Capacity	(Note 4)		150			150		pF

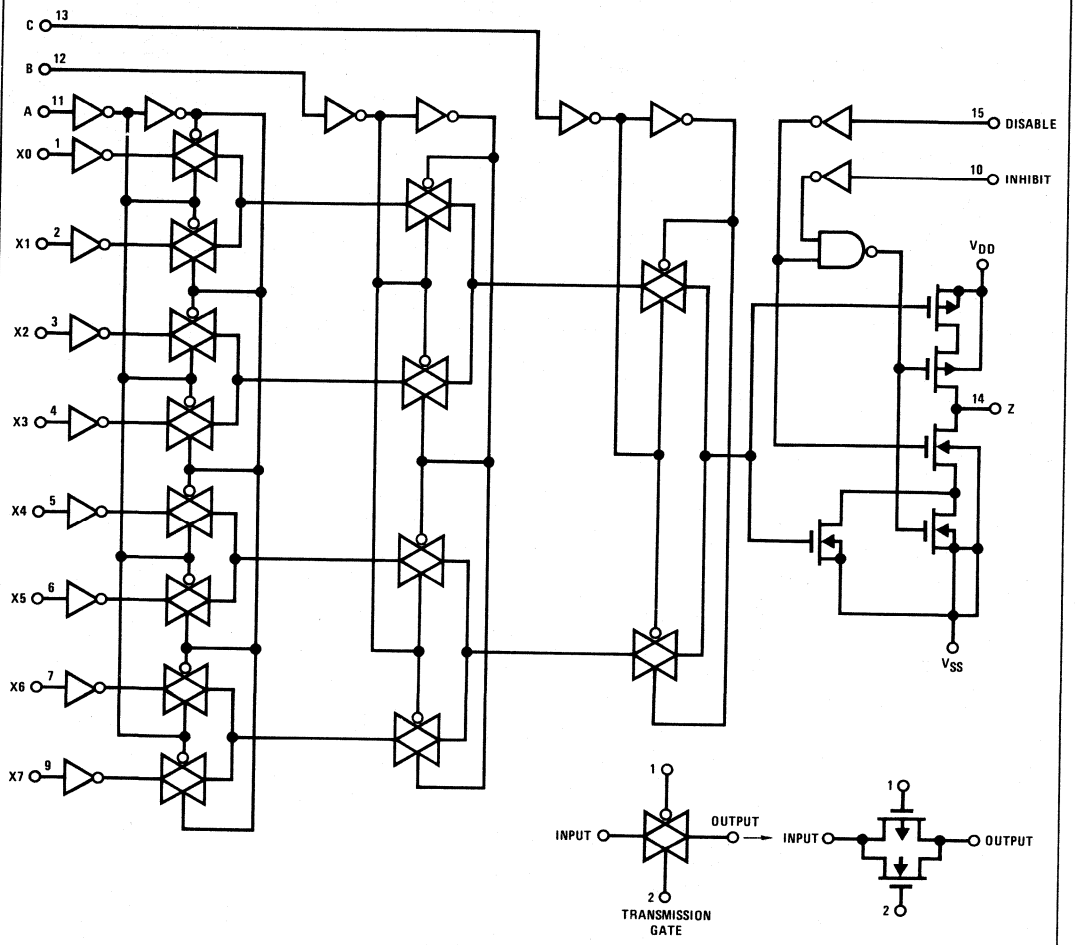
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance guaranteed by periodic testing.

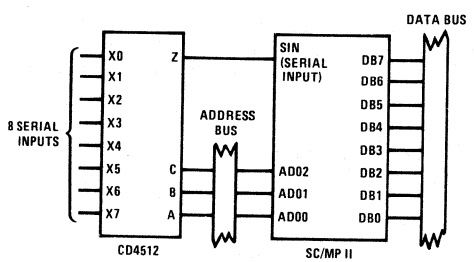
Note 4: C_{PD} determines the no load AC power of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note AN-90.

Logic Diagram

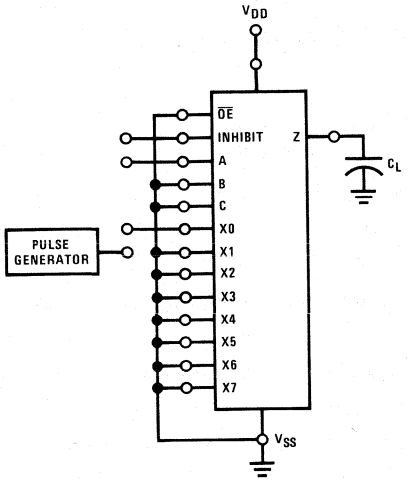


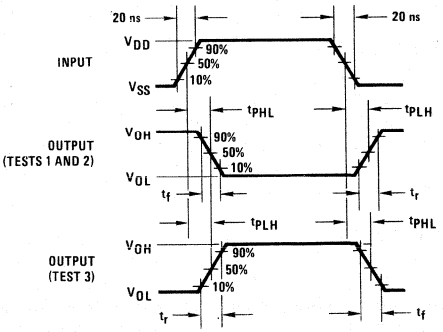
Typical Application

Serial Data Routing Interface



AC Test Circuit and Switching Time Waveforms

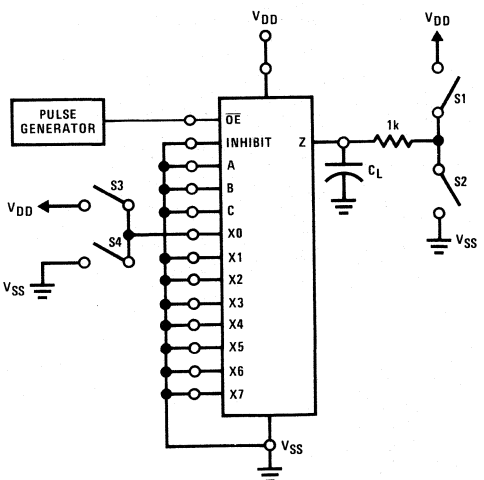


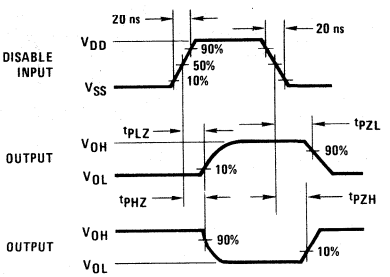


INPUT CONNECTIONS FOR t_r, t_f, t_{PLH}, t_{PHL}

TEST	INHIBIT	A	X0
1	PG	GND	V_{DD}
2	GND	PG	V_{DD}
3	GND	GND	PG

TRI-STATE AC Test Circuit and Switching Time Waveforms





SWITCH POSITIONS FOR TRI-STATE TEST

TEST	S1	S2	S3	S4
t_{PHZ}	Open	Closed	Closed	Open
t_{PLZ}	Closed	Open	Open	Closed
t_{PZL}	Closed	Open	Open	Closed
t_{PZH}	Open	Closed	Closed	Open

National Semiconductor

CD4514BM/CD4514BC, CD4515BM/CD4515BC 4-Bit Latched/4-to-16 Line Decoders

General Description

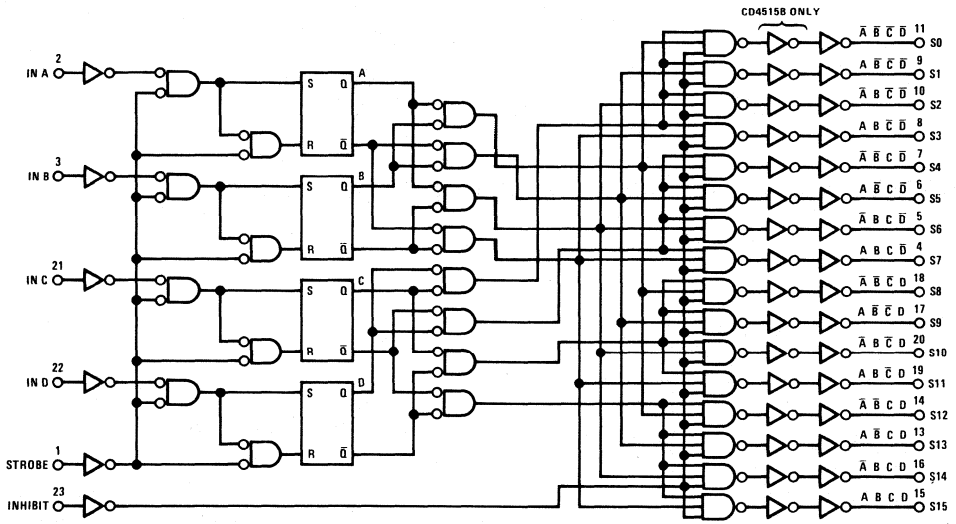
The CD4514B and CD4515B are 4-to-16 line decoders with latched inputs implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors. These circuits are primarily used in decoding applications where low power dissipation and/or high noise immunity is required.

The CD4514B (output active high option) presents a logical "1" at the selected output, whereas the CD4515B presents a logical "0" at the selected output. The input latches are R-S type flip-flops which hold the last input data presented prior to the strobe transition from "1" to "0". This input data is decoded and the corresponding output is activated. An output inhibit line is also available.

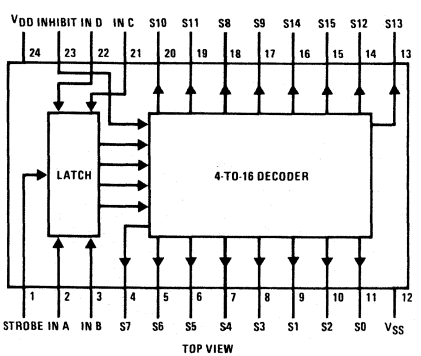
Features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{CC} typ
- Low power TTL compatibility — fan out of 2 driving 74L
- Low quiescent power dissipation — 0.025 μW/package typical @ 5 V_{DC}
- Single supply operation
- Input impedance = $10^{12}\Omega$ typically
- Plug-in replacement for MC14514, MC14515

Logic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4514BM, CD4515BM	−55°C to +125°C
CD4514BC, CD4515BC	−40°C to +85°C

DC Electrical Characteristics CD4514BM, CD4515BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.005	5.0		150	μA
		V_{DD} = 10V		10.0		0.010	10.0		300	μA
		V_{DD} = 15V		20.0		0.015	20.0		600	μA
V_{OL}	Low Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_{IL} = 0V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_O = 0.5V or 4.5V								
		V_{DD} = 5V, $\|I_O\| < 1\ \mu A$	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.80		2.40		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.80		−2.40		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4514BC, CD4515BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V

DC Electrical Characteristics (Continued) CD4514BC, CD4515BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.90		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.90		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics All types C_L = 50 pF, T_A = 25°C, $t_r = t_f$ = 20 ns unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL}, t_{TLH}	Transition Times	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}, t_{PHL}	Propagation Delay Times	V_{DD} = 5V		550	1100	ns
		V_{DD} = 10V		225	450	ns
		V_{DD} = 15V		150	300	ns
t_{PLH}, t_{PHL}	Inhibit Propagation Delay Times	V_{DD} = 5V		400	800	ns
		V_{DD} = 10V		150	300	ns
		V_{DD} = 15V		100	200	ns
t_{SU}	Set Up Time	V_{DD} = 5V		125	250	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
t_{WH}	Strobe Pulse Width	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		38	75	ns
C_{PD}	Power Dissipation Capacitance	Per Package, (Note 4)		150		pF
C_{IN}	Input Capacitance	Any Input, (Note 3)		5	7.5	pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and 'Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C&74C Family Characteristics application note, AN-90.

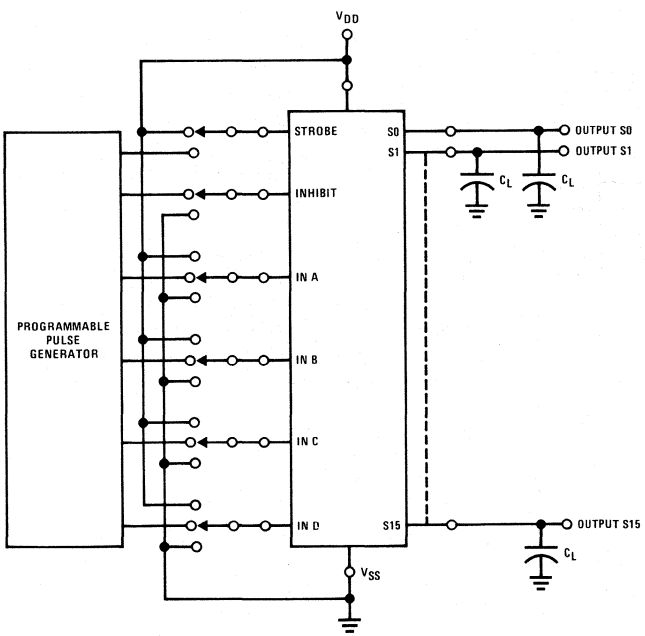
Truth Table

DECODE TRUTH TABLE (Strobe = 1)

INHIBIT	DATA INPUTS				SELECTED OUTPUT CD4514 = LOGIC "1" CD4515 = LOGIC "0"
	D	C	B	A	
0	0	0	0	0	S0
0	0	0	0	1	S1
0	0	0	1	0	S2
0	0	0	1	1	S3
0	0	1	0	0	S4
0	0	1	0	1	S5
0	0	1	1	0	S6
0	0	1	1	1	S7
0	1	0	0	0	S8
0	1	0	0	1	S9
0	1	0	1	0	S10
0	1	0	1	1	S11
0	1	1	0	0	S12
0	1	1	0	1	S13
0	1	1	1	0	S14
0	1	1	1	1	S15
1	X	X	X	X	All Outputs = 0, CD4514 All Outputs = 1, CD4515

X = Don't care

AC Test Circuit and Switching Time Waveforms



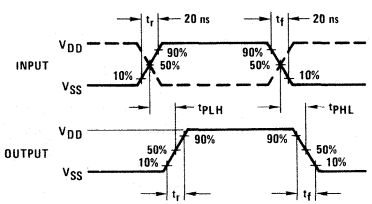


FIGURE 1

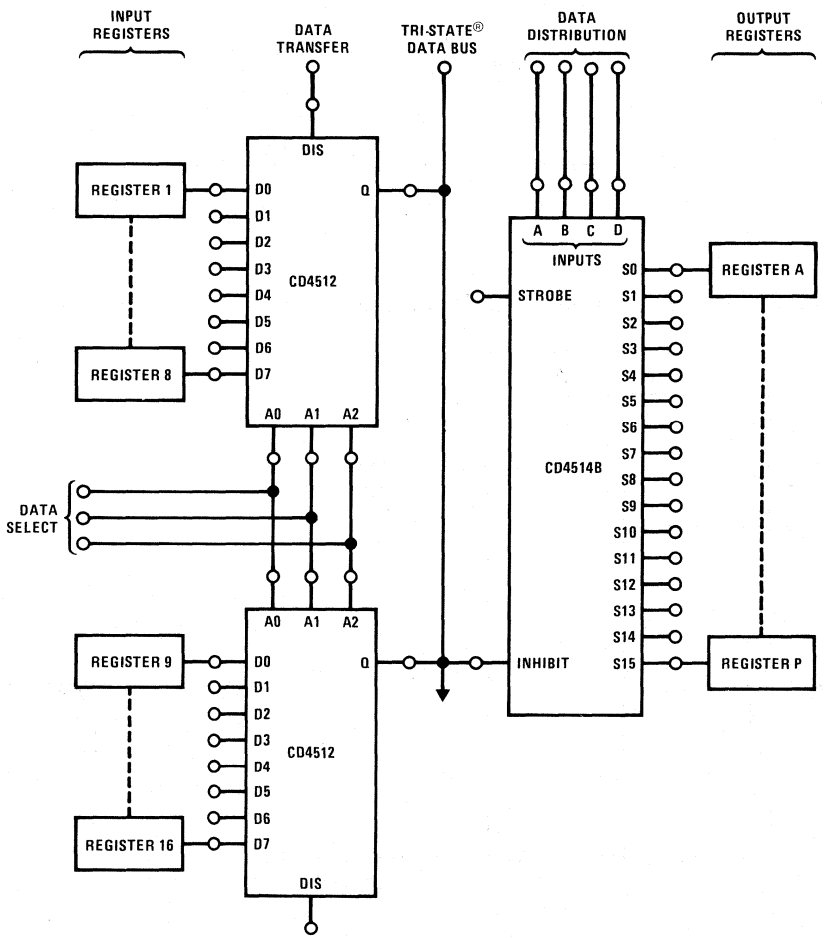
Applications

Two CD4512 8-channel data selectors are used here with the CD4514B 4-bit latch/decoder to effect a complex data routing system. A total of 16 inputs from data registers are selected and transferred via a TRI-STATE® data bus to a data distributor for rearrangement and entry into 16 output registers. In this way sequential data can be re-routed or intermixed according to patterns determined by data select and distribution inputs.

Data is placed into the routing scheme via the 8 inputs on both CD4512 data selectors. One register is assigned to each input. The signals on A0, A1 and A2 choose 1-of-8 inputs for transfer out to the TRI-STATE data bus. A fourth signal, labelled Dis, disables one of the CD4512 selectors, assuring transfer of data from only one register.

In addition to a choice of input registers, 1–16, the rate of transfer of the sequential information can also be varied. That is, if the CD4512 were addressed at a rate that is 8 times faster than the shift frequency of the input registers, the most significant bit (MSB) from each register could be selected for transfer to the data bus. Therefore, all of the most significant bits from all of the registers can be transferred to the data bus before the next most significant bit is presented for transfer by the input registers.

Information from the TRI-STATE bus is redistributed by the CD4514B 4-bit latch/decoder. Using the 4-bit address, INA–IND, the information on the inhibit line can be transferred to the addressed output line to the desired output registers, A–P. This distribution of data bits to the output registers can be made in many complex patterns. For example, all of the most significant bits from the input registers can be routed into output register A, all of the next most significant bits into register B, etc. In this way horizontal, vertical, or other methods of data slicing can be implemented.



National Semiconductor

CD4518BM/CD4518BC, CD4520BM/CD4520BC
Dual Synchronous Up Counters

general description

The CD4518BM/CD4518BC dual BCD counter and the CD4520BM/CD4520BC dual binary counter are implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors.

Each counter consists of two identical, independent, synchronous, 4-stage counters. The counter stages are toggle flip-flops which increment on either the positive-edge of CLOCK or negative-edge of ENABLE, simplifying cascading of multiple stages. Each counter can be asynchronously cleared by a high level on the RESET line. All inputs are protected against static discharge by diode clamps to both V_{DD} and V_{SS}.

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 6 MHz counting rate (typ) at V_{DD} = 10V

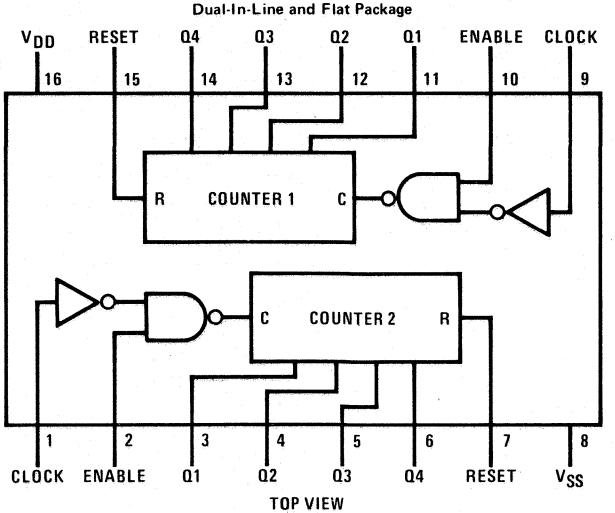
truth table

CLOCK	ENABLE	RESET	ACTION
↗	1	0	Increment counter
0	↘	0	Increment counter
↘	X	0	No change
X	↗	0	No change
↗	0	0	No change
1	↘	0	No change
X	X	1	Q1 thru Q4 = 0

X = Don't Care

connection diagram

Dual-In-Line and Flat Package



TOP VIEW

absolute maximum ratings

(Notes 1 and 2)

V_{DD} Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} Supply Voltage	3V to 15V
V_{IN} Input Voltage	0V to V_{DD}
T_A Operating Temperature Range	
CD4518BM, CD4520BM	−55°C to +125°C
CD4518BC, CD4520BC	−40°C to +85°C

dc electrical characteristics CD4518BM, CD4520BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.01	5		150	μA
		V_{DD} = 10V		10		0.01	10		300	μA
		V_{DD} = 15V		20		0.01	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4518BC, CD4520BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.01	20		150	μA
		V_{DD} = 10V		40		0.01	40		300	μA
		V_{DD} = 15V		80		0.01	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$, $V_{IH} = V_{DD}$, V_{IL} = 0V								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (Continued) CD4518BC, CD4520BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$		1.5		2.25	1.5		1.5	V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$		3.0		4.5	3.0		3.0	V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\ \mu A$								
		$V_{DD} = 5V$, $V_O = 0.5V$ or $4.5V$	3.5		3.5	2.75		3.5		V
		$V_{DD} = 10V$, $V_O = 1V$ or $9V$	7.0		7.0	5.5		7.0		V
		$V_{DD} = 15V$, $V_O = 1.5V$ or $13.5V$	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 0.4V$	0.52		0.44	0.88		0.36		mA
		$V_{DD} = 10V$, $V_O = 0.5V$	1.3		1.1	2.25		0.9		mA
		$V_{DD} = 15V$, $V_O = 1.5V$	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	$V_{IH} = V_{DD}$, $V_{IL} = 0V$								
		$V_{DD} = 5V$, $V_O = 4.6V$	−0.52		−0.44	−0.88		−0.36		mA
		$V_{DD} = 10V$, $V_O = 9.5V$	−1.3		−1.1	−2.25		−0.9		mA
		$V_{DD} = 15V$, $V_O = 13.5V$	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	$V_{DD} = 15V$, $V_{IN} = 0V$		−0.3		-10^{-5}	−0.3		−1.0	μA
		$V_{DD} = 15V$, $V_{IN} = 15V$		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics $T_A = 25°C$, $C_L = 50$ pF, $R_L = 200k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay Time, Clock → Q	$V_{DD} = 5V$		325	650	ns
		$V_{DD} = 10V$		110	225	ns
		$V_{DD} = 15V$		85	170	ns
t_{PHL}	Propagation Delay Time Reset → Q	$V_{DD} = 5V$		220	560	ns
		$V_{DD} = 10V$		90	230	ns
		$V_{DD} = 15V$		65	160	ns
t_{THL}, t_{TLH}	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		40	80	ns
f_{CL}	Maximum Clock Input Frequency	$V_{DD} = 5V$	1.5	3		MHz
		$V_{DD} = 10V$	3.0	6		MHz
		$V_{DD} = 15V$	4.0	8		MHz
t_{WL}, t_{WH}	Minimum Clock Pulse Width	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	ns
		$V_{DD} = 15V$		35	70	ns
t_{RCL}, t_{FCL}	Maximum Clock or Enable Rise and Fall Time	$V_{DD} = 5V$	15			μs
		$V_{DD} = 10V$	10			μs
		$V_{DD} = 15V$	5			μs
t_{WH}, t_{WL}	Minimum Enable Pulse Width	$V_{DD} = 5V$		125	250	ns
		$V_{DD} = 10V$		55	110	ns
		$V_{DD} = 15V$		40	80	ns
t_{WH}	Minimum Reset Pulse Width	$V_{DD} = 5V$		180	375	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		65	130	ns
C_{IN}	Input Capacitance	Any Input		5	7.5	pF
C_{PD}	Power Dissipation Capacity	Either Counter, (Note 3)		50		pF

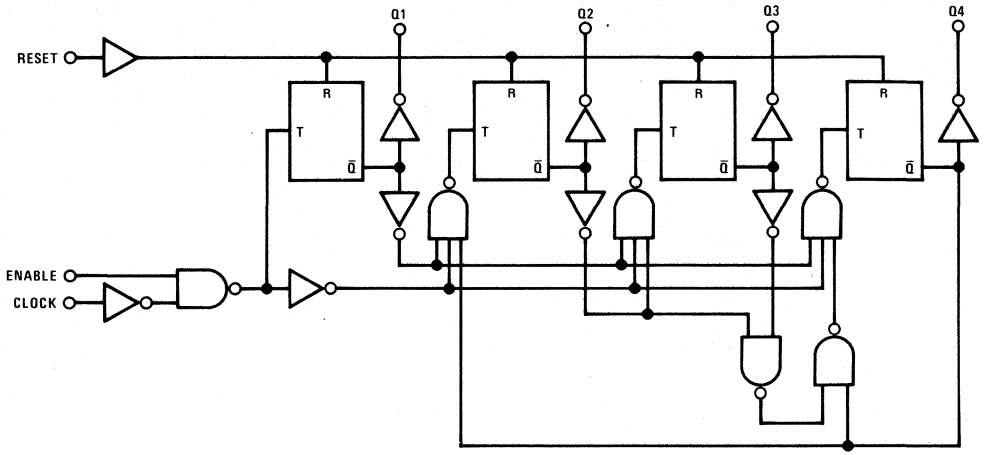
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: $V_{SS} = 0V$ unless otherwise specified.

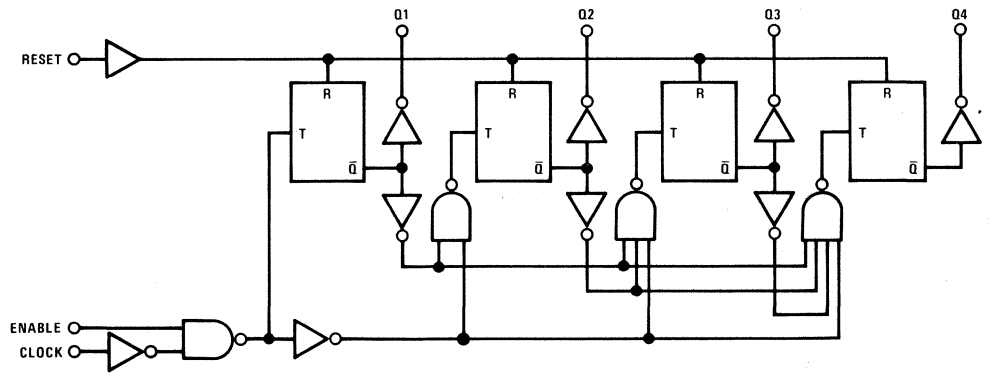
Note 3: C_{PD} determines the no load ac power consumption of a CMOS device. For a complete explanation, see "54C/74C Family Characteristics," application note AN-90.

logic diagrams

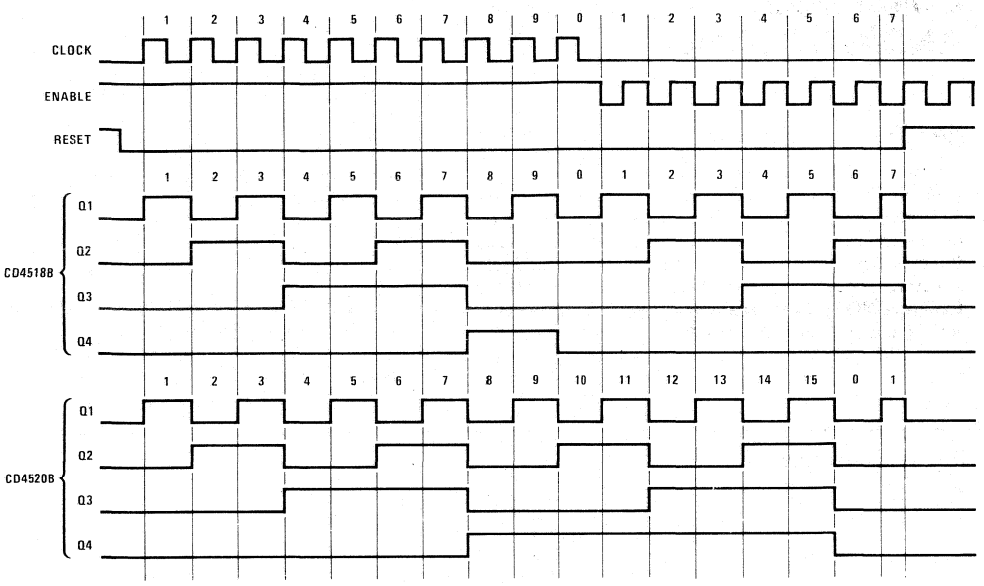
Decade Counter (CD4518B) 1/2 Device Shown



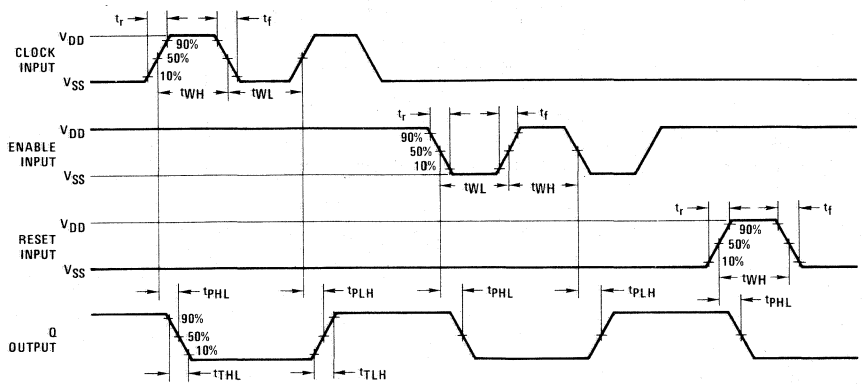
Binary Counter (CD4520B) 1/2 Device Shown



timing diagram



switching time waveforms



National Semiconductor

CD4519BM/CD4519BC 4-Bit AND/OR Selector

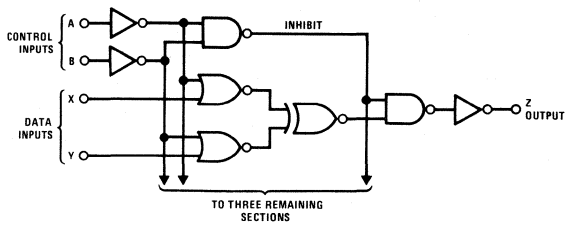
general description

The CD4519B is a monolithic complementary MOS (CMOS) integrated circuit constructed with N and P-channel enhancement mode transistors. Depending on the condition of the control inputs, this part provides three functions in one package: a 4-bit AND/OR selector, a quad 2-channel Data Selector, or a Quad Exclusive-NOR Gate. The device outputs have equal source and sink current capabilities and conform to the standard B series output drive and supply voltage ratings.

features

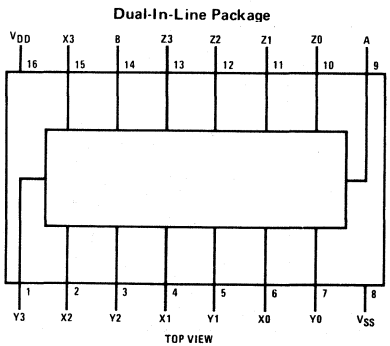
- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- 5V–10V–15V parametric ratings
- Symmetrical output characteristics
- Maximum input leakage 1μA at 15V over full temperature range
- Second source of Motorola MC14519

logic diagram



connection diagram

Dual-In-Line Package



TOP VIEW

truth table

CONTROL INPUTS		OUTPUT
A	B	Z_n
0	0	0
0	1	Y_n
1	0	X_n
1	1	$X_n \odot Y_n$

Note: $X_n \odot Y_n = \overline{X_n \oplus Y_n} = X_nY_n + \overline{X}_n\overline{Y}_n$

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4519BM	−55°C to +125°C
CD4519BC	−40°C to +85°C

dc electrical characteristics CD4519BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1		0.005	1		30	μA
		V_{DD} = 10V		2		0.006	2		60	μA
		V_{DD} = 15V		4		0.007	4		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

dc electrical characteristics CD4519BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		4			4		30	μA
		V_{DD} = 10V		8			8		60	μA
		V_{DD} = 15V		16			16		120	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V

dc electrical characteristics (con't) CD4519BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6	4.0		4.0	V
V_{IH}	High Level Input Voltage	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	3		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	6		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	9		11.0		V
I_{OL}	Low Level Output Current	$\|I_O\| < 1\mu A$								
		V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200K Ω, t_r = t_f = 20ns, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PHL}, t_{PLH}	Propagation Delay High-to-Low Level	*(Figure 1)*				
	or Low-to-High Level	V_{DD} = 5V		180	360	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		60	120	ns
t_{THL}, t_{TLH}	Transition Time	*(Figure 1)*				
		V_{DD} = 5V		90	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
C_{IN}	Average Input Capacitance	Any Input (Note 3)		5	7.5	pF
C_{pd}	Power Dissipation Capacity	Any Gate (Note 4)		25		pF

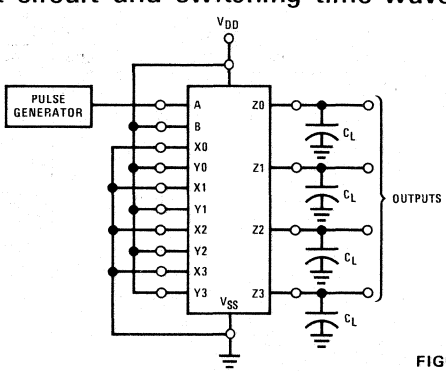
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{pd} determines the no load ac power consumption of any CMOS device. For complete explanation, see 54C/74C Family characteristics application note AN-90.

ac test circuit and switching time waveforms



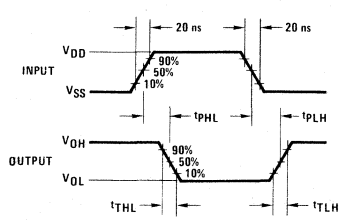
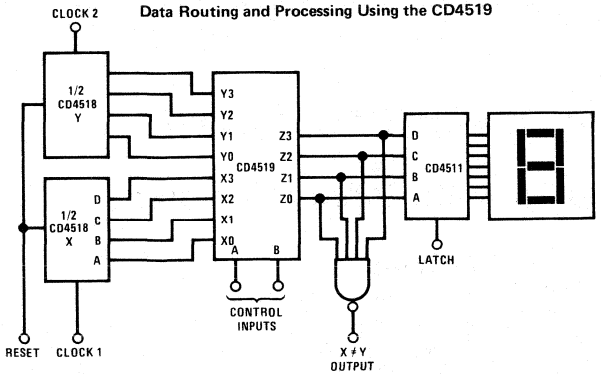


FIGURE 1

typical application

Data Routing and Processing Using the CD4519



CONTROL INPUTS		FUNCTION
A	B	
0	0	Display Zero
0	1	Display Counter Y
1	0	Display Counter X
1	1	Compare Counters

National Semiconductor

CD4522BM/CD4522BC Programmable Divide-By-N 4-Bit BCD Counter
CD4526BM/CD4526BC Programmable Divide-By-N 4-Bit Binary Counter

General Description

The CD4522BM/CD4522BC, CD4526BM/CD4526C are CMOS programmable cascadable down counters with a decoded "0" state output for divide-by-N applications. In single stage applications, the "0" output is applied to the Preset Enable input. For multi-stage applications, the "0" output is used in conjunction with the CF (Cascade Feedback) input to perform the divide-by-N function. The "0" output is normally at logical "0" level; it will go to a logical "1" state only when the counter is at its terminal count (0000) and if CF is at logical "1" level. Thus, CF acts as an active low inhibit for the "0" output. This feature allows cascade divide-by-N operations with no additional gate required (see Applications section). The Master Reset function provides synchronous initiation of divide-by-N cycles. The Clock Inhibit input allows disabling of the pulse counting function.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Features

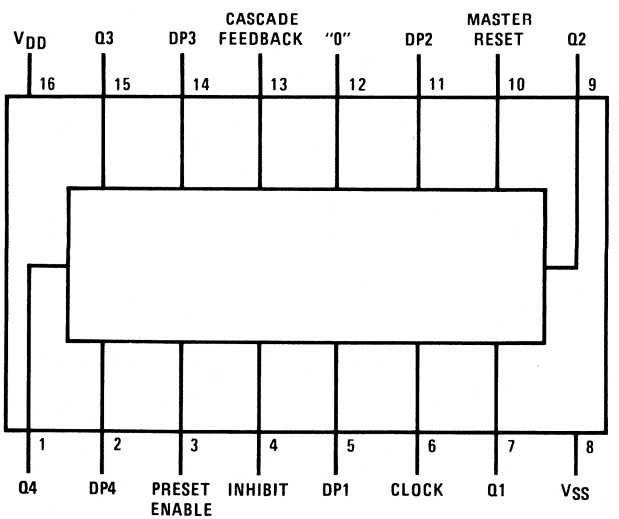
- Wide supply voltage range — 3V to 18V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Quiescent current = 5 nA/package typ @ V_{DD} = 5V
- Internally synchronous for high internal and external speed
- Logic edge-clocked design—incremented on positive transition of Clock or negative transition of Clock Inhibit
- Medium speed 7.7 MHz typ @ V_{DD} = 10V
- Asynchronous Preset Enable

Applications

- Programmable down counter
- Programmable frequency divider
- Frequency synthesizers
- Phase-locked loops

Connection Diagram

Dual-In-Line Package



TOP VIEW

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4522BM, CD4526BM	−55°C to +125°C
CD4522BC, CD4526BC	−40°C to +85°C

DC Electrical Characteristics CD4522BM, CD4526BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.005	5		150	μA
		V_{DD} = 10V		10		0.010	10		300	μA
		V_{DD} = 15V		20		0.015	20		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4522BC, CD4526BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
		V_{DD} = 10V		40		0.010	40		300	μA
		V_{DD} = 15V		80		0.015	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V

DC Electrical Characteristics (Continued) CD4522BC, CD4526BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{THL} or t_{TLH}	Output Transition Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to Q Outputs	V_{DD} = 5V		350	825	ns
		V_{DD} = 10V		130	345	ns
		V_{DD} = 15V		90	240	ns
t_{PHL} & t_{PLH}	Propagation Delay Time From Clock to "0" Output	V_{DD} = 5V		200	500	ns
		V_{DD} = 10V		80	250	ns
		V_{DD} = 15V		60	190	ns
PW_C	Minimum Clock Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
f_{CL}	Maximum Clock Pulse Frequency	V_{DD} = 5V	1.5	2.9		MHz
		V_{DD} = 10V	3.0	7.7		MHz
		V_{DD} = 15V	4.0	11		MHz
t_{rCL} & t_{fCL}	Maximum Clock or Inhibit Rise and Fall Time	V_{DD} = 5V	15			μs
		V_{DD} = 10V	15			μs
		V_{DD} = 15V	15			μs
t_{HOLD}	Hold Time	V_{DD} = 5V		40	125	ns
		V_{DD} = 10V		25	50	ns
		V_{DD} = 15V		20	40	ns
PW_{PE}	Minimum Preset Enable Pulse Width	V_{DD} = 5V		120	280	ns
		V_{DD} = 10V		50	120	ns
		V_{DD} = 15V		35	85	ns
PW_{MR}	Minimum Master Reset Pulse Width	V_{DD} = 5V		160	350	ns
		V_{DD} = 10V		75	180	ns
		V_{DD} = 15V		50	120	ns
C_{IN}	Input Capacitance	(Note 3)		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	Per Package (Note 4)		100		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

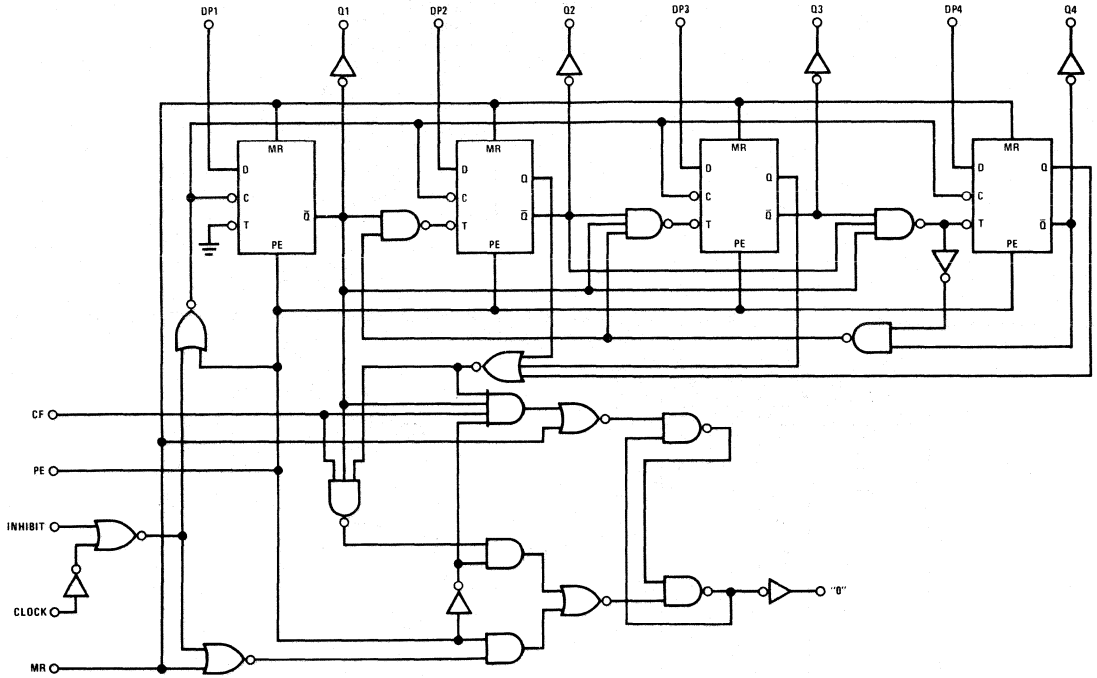
Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Capacitance is guaranteed by periodic testing.

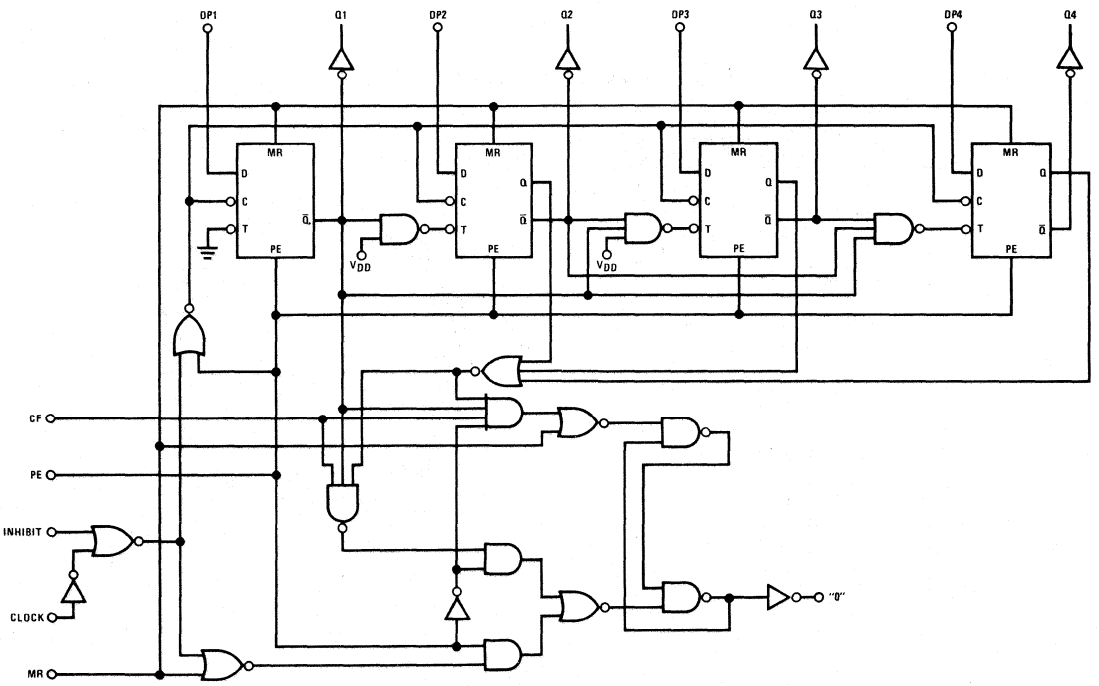
Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation, see 54C/74C Family Characteristics application note, AN-90.

Logic Diagrams

CD4522BM/CD4522BC



CD4526BM/CD4526BC



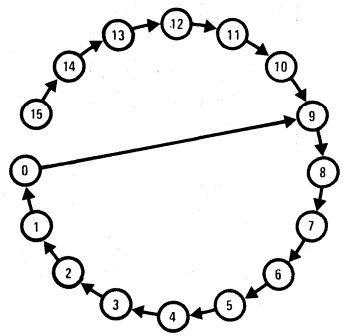
Truth Tables and Count Sequences

Both Types

CLOCK	INHIBIT	PRESET ENABLE	MASTER RESET	ACTION
0	0	0	0	No count
⌐	0	0	0	Count 1
X	1	0	0	No count
1	¬	0	0	Count 1
X	X	1	0	Preset
X	X	X	1	Reset

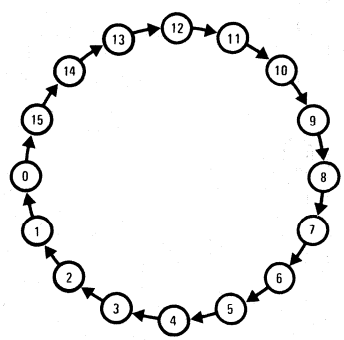
CD4522BM/CD4522BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



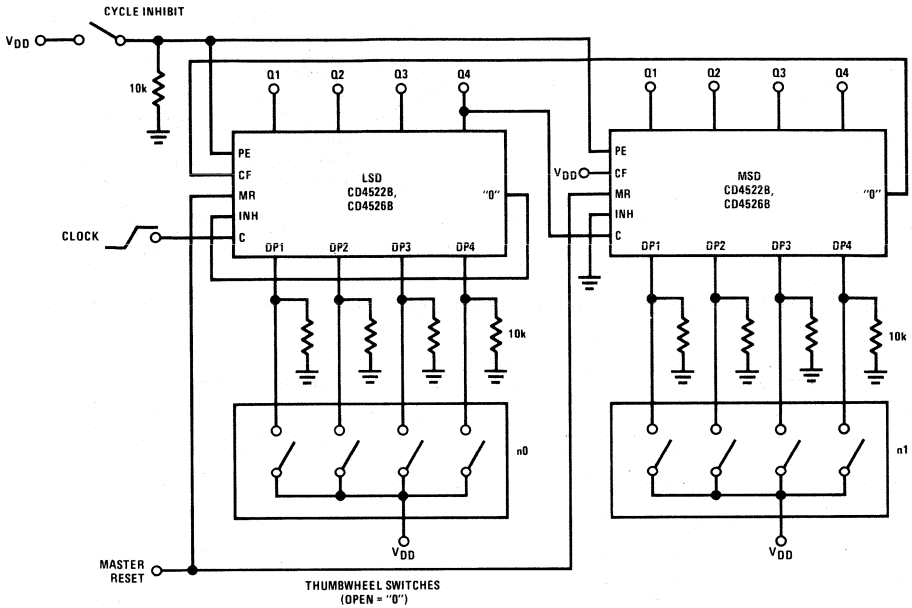
CD4526BM/CD4526BC

COUNT	OUTPUT			
	Q4	Q3	Q2	Q1
15	1	1	1	1
14	1	1	1	0
13	1	1	0	1
12	1	1	0	0
11	1	0	1	1
10	1	0	1	0
9	1	0	0	1
8	1	0	0	0
7	0	1	1	1
6	0	1	1	0
5	0	1	0	1
4	0	1	0	0
3	0	0	1	1
2	0	0	1	0
1	0	0	0	1
0	0	0	0	0



Typical Applications

2-Stage Programmable Down Counter

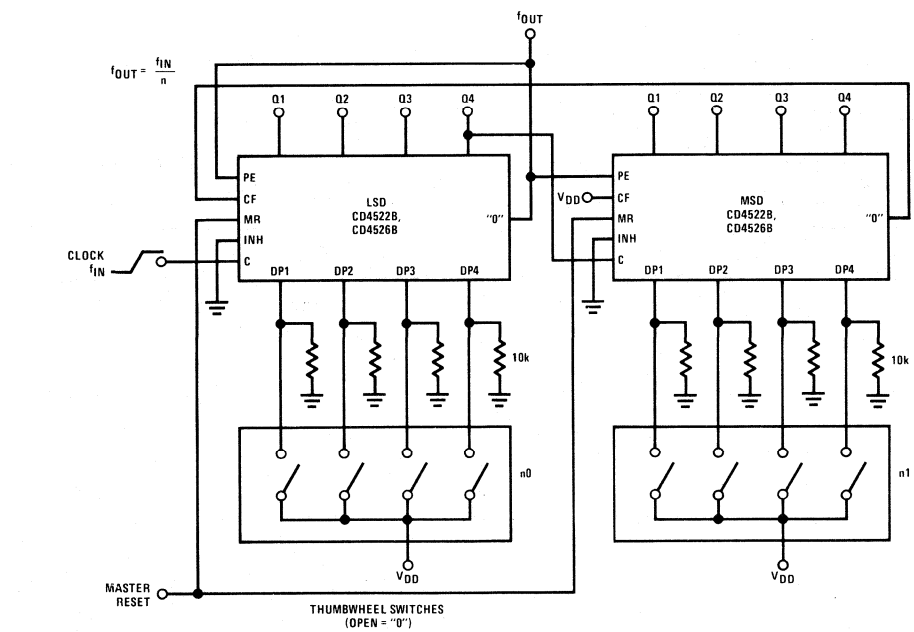


COUNTING CYCLE

LSD	MSD
n0	
n0−1	
.	
.	n1
.	
1	
0	
9 (15)	
8 (14)	
.	
.	n1−1
.	
1	
0	
.	
.	
.	
9 (15)	
8 (14)	
.	
.	0
.	
1	
0	

↓ STOP

2-Stage Programmable Frequency Divider



COUNTING CYCLE

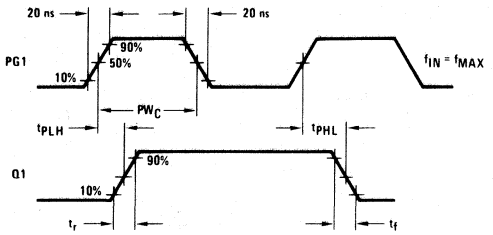
LSD	MSD
n0	
n0−1	
.	
.	n1
.	
1	
0	
9 (15)	
8 (14)	
.	
.	n1−1
.	
1	
0	
.	
.	
.	
9 (15)	
8 (14)	
.	
.	0
.	
1	
0	

↓ REPEAT CYCLE

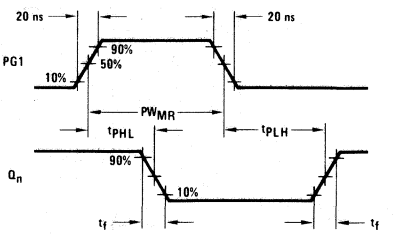
Note. When cascading more than 2 packages, tie "0" output of the nth package to CF input of the (n−1)th package for all n = 2, 3.

Switching Time Waveforms

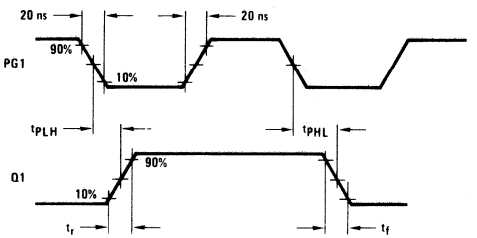
Test No. 1



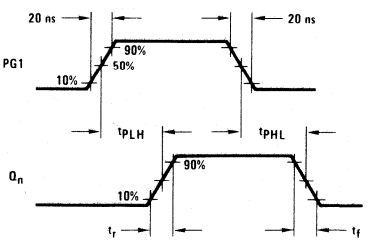
Test No. 4



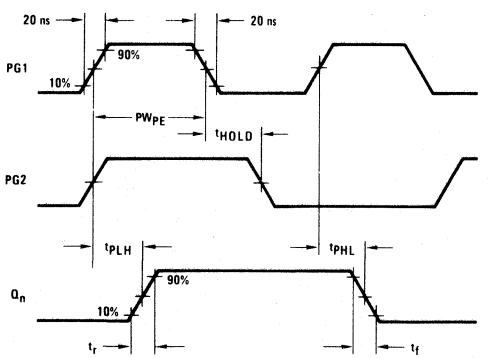
Test No. 2



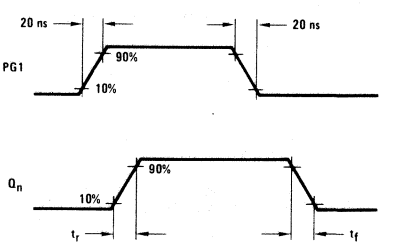
Tests No. 5 and 7



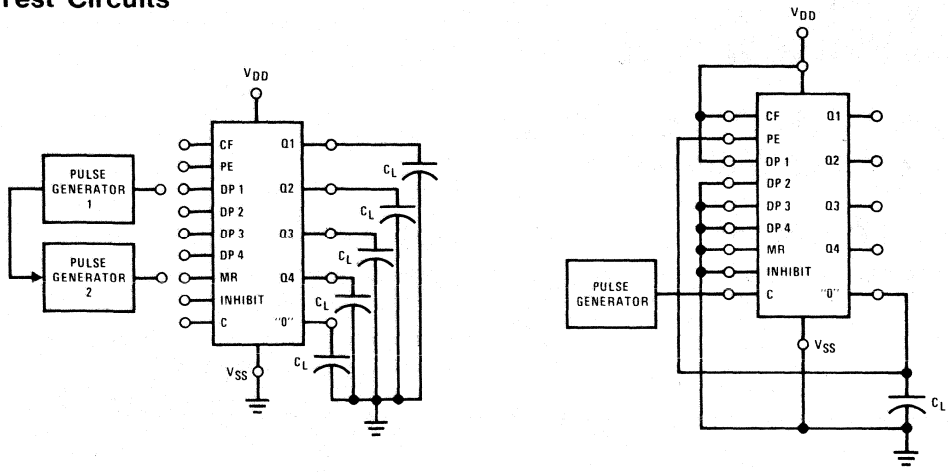
Test No. 3



Test No. 6



AC Test Circuits



a) Tests No. 1–6

b) Test No. 7

FIGURE 1. Test Circuit

Test Conditions

TABLE I

CHARACTERISTIC	TEST NO.	CLOCK	INHIBIT	PE	MR	DP_n	CF	OUTPUT
t_r, t_f, t_{PLH}, t_{PHL}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	2	V_{DD}	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
	5	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	V_{SS}	Q_n
PW_{MR}	4	V_{SS}	V_{SS}	V_{DD}	PG1	V_{DD}	V_{SS}	Q_n
PW_{PE}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
PW_C	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
f_{MAX}	1	PG1	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	Q1
t_{HOLD}	3	V_{SS}	V_{SS}	PG1	V_{SS}	PG2	V_{SS}	Q_n
t_r, t_f	6	V_{SS}	V_{SS}	V_{SS}	V_{DD}	V_{SS}	PG1	"0"
t_{PLH}, t_{PHL}	7	PG	V_{SS}	*Fig. 1b*	V_{SS}	*Fig. 1b*	V_{DD}	"0"

National Semiconductor

CD4528BM/CD4528BC Dual Monostable Multivibrator

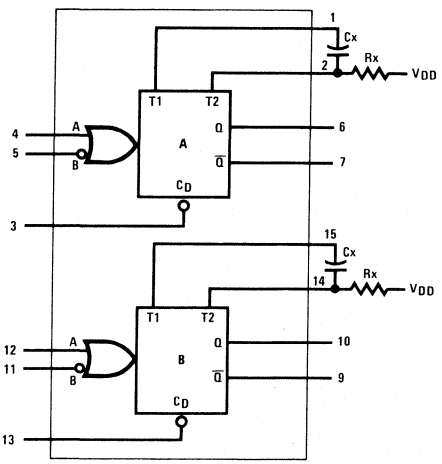
General Description

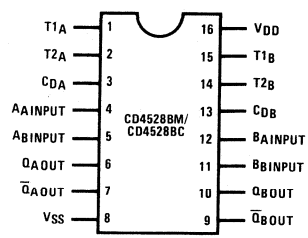
The CD4528B is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or falling edge of an input pulse, resulting in an output pulse over a wide range of widths. Pulse duration and accuracy are determined by external timing components Rx and Cx.

Features

- Wide supply voltage range — 3V to 18V
- Separate reset available
- Quiescent current = 5.0 nA/package typical at 5VDC
- Diode protection on all inputs
- Triggerable from leading or trailing edge pulse
- Capable of driving two low-power TTL loads or one low-power Schottky TTL load over the rated temperature range

Connection Diagrams





Truth Table

Inputs			Outputs	
Clear	A	B	Q	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↓	⎍	⎎
H	↑	H	⎍	⎎

H = High Level
L = Low Level
↑ = Transition from Low to High
↓ = Transition from High to Low
⎍ = One High Level Pulse
⎎ = One Low Level Pulse
X = Irrelevant

Absolute Maximum Ratings (Notes 1 and 2)

V_{DD}, DC Supply Voltage −0.5 VDC to +18 VDC
V_{IN}, Input Voltage, All Inputs −0.5 VDC to V_{DD} +0.5 V_{DC}
T_S, Storage Temperature Range −65°C to +150°C
P_D, Package Dissipation 500 mW
T_L, Lead Temperature (soldering, 10 seconds) 300°C

Recommended Operating Conditions (Note 2)

V_{DD}, DC Supply Voltage 3 V to 15 V
V_{IN}, Input Voltage 0 V to V_{DD} V_{DC}
T_A, Operating Temperature Range
CD4528BM −55°C to +125°C
CD4528BC −40°C to +85°C

DC Electrical Characteristics CD4528BM (Note 2)

Parameter	Conditions	−55°C		+25°C			+125°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		5	0.005		5		150	μA
	V_{DD} = 10V		10	0.010		10		300	μA
	V_{DD} = 15V		20	0.015		20		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
	V_{DD} = 10V		0.05			0.05		0.05	V
	V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.25		−0.2	−0.36		−0.14		mA
	V_{DD} = 10V, V_O = 9.5V	−0.62		−0.5	−0.9		−0.35		mA
	V_{DD} = 15V, V_O = 13.5V	−1.8		−1.5	−3.5		−1.1		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4528BC (Note 2)

Parameter	Conditions	-40°C		+25°C			+85°C		Units
		Min	Max	Min	Typ	Max	Min	Max	
I_{DD} Quiescent Device Current	V_{DD} = 5V		20		0.005	20		150	μA
	V_{DD} = 10V		40		0.010	40		300	μA
	V_{DD} = 15V		80		0.015	80		600	μA
V_{OL} Low Level Output Voltage	V_{DD} = 5V		0.05			0.05		0.05	V
	V_{DD} = 10V		0.05			0.05		0.05	V
	V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH} High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5.0		4.95		V
	V_{DD} = 10V	9.95		9.95	10.0		9.95		V
	V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL} Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
	V_{DD} = 10V, V_O = 1.0V or 9.0V		3.0		4.50	3.0		3.0	V
	V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH} High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
	V_{DD} = 10V, V_O = 1.0V or 9.0V	7.0		7.0	5.50		7.0		V
	V_{DD} = 15V, V_O = 0.5V or 4.5V	11.0		11.0	8.25		11.0		V
I_{OL} Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
	V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
	V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH} High Level Output Current	V_{DD} = 5V, V_O = 4.6V	-0.2		-0.16	-0.36		-0.12		mA
	V_{DD} = 10V, V_O = 9.5V	-0.5		-0.4	-0.9		-0.3		mA
	V_{DD} = 15V, V_O = 13.5V	-1.4		-1.2	-3.5		-1.0		mA
I_{IN} Input Current	V_{DD} = 15V, V_{IN} = 0V		-0.3		-10^{-5}	-0.3		-1.0	μA
	V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

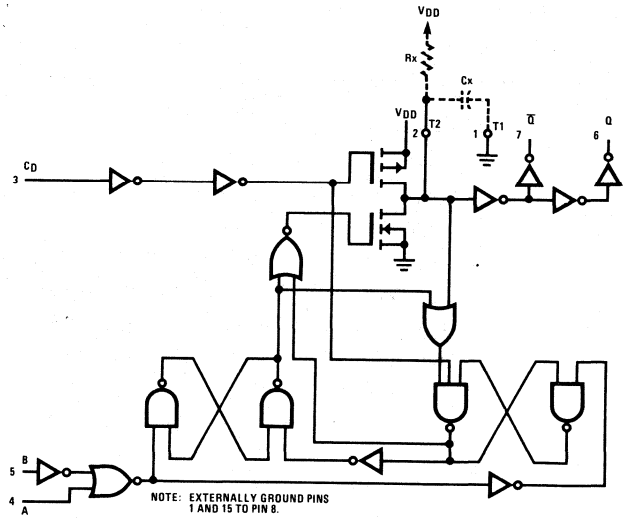
Note 2: V_{SS} = 0V unless otherwise specified.

AC Electrical Characteristics CD4528BM

$T_A = 25°C$, $C_L = 50\,pF$, $R_L = 200\,k\Omega$, Input $t_r = t_f = 20\,ns$, unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Output Rise Time	$t_r = (3.0\,ns/pF)C_L + 30\,ns$, $V_{DD} = 5.0V$		180	400	ns
	$t_r = (1.5\,ns/pF)C_L + 15\,ns$, $V_{DD} = 10.0V$		90	200	ns
	$t_r = (1.1\,ns/pF)C_L + 10\,ns$, $V_{DD} = 15.0V$		65	160	ns
Output Fall Time	$t_f = (1.5\,ns/pF)C_L + 25\,ns$, $V_{DD} = 5.0V$		100	200	ns
	$t_f = (0.75\,ns/pF)C_L + 12.5\,ns$, $V_{DD} = 10.0V$		50	100	ns
	$t_f = (0.55\,ns/pF)C_L + 9.5\,ns$, $V_{DD} = 15.0V$		35	80	ns
Turn-Off, Turn-On Delay A or B to Q or $\overline{Q}$ Cx = 15 pF, Rx = 5.0 kΩ	$t_{PLH}, t_{PHL} = (1.7\,ns/pF)C_L + 240\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = (0.66\,ns/pF)C_L + 8\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 65\,ns$, $V_{DD} = 15.0V$		65	150	ns
Turn-Off, Turn-On Delay A or B to Q or $\overline{Q}$ Cx = 100 pF, Rx = 10 kΩ	$t_{PLH}, t_{PHL} = 1.7\,ns/pF)C_L + 620\,ns$, $V_{DD} = 5.0V$		230	500	ns
	$t_{PLH}, t_{PHL} = 0.66\,ns/pF)C_L + 257\,ns$, $V_{DD} = 10.0V$		100	250	ns
	$t_{PLH}, t_{PHL} = (0.5\,ns/pF)C_L + 185\,ns$, $V_{DD} = 15.0V$		65	150	ns
Minimum Input Pulse Width A or B Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		60	150	ns
	$V_{DD} = 10.0V$		20	50	ns
	$V_{DD} = 15.0V$		20	50	ns
Output Pulse Width Q or $\overline{Q}$ For Cx < 0.01 μF (see graph for appropriate V_{DD} level) Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		550		ns
	$V_{DD} = 10.0V$		350		ns
	$V_{DD} = 15.0V$		300		ns
For Cx > 0.01 μF use $PW_{out} = 0.2RxCx\ \ln[V_{DD} - V_{SS}]$ Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$	15	29	45	μs
	$V_{DD} = 10.0V$	10	37	90	μs
	$V_{DD} = 15.0V$	15	42	95	μs
Pulse Width Match Between Circuits in the Same Package Cx = 10,000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		6	25	%
	$V_{DD} = 10.0V$		8	35	%
	$V_{DD} = 15.0V$		8	35	%
Reset Propagation Delay, t_{PLH}, t_{PHL} Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		325	600	ns
	$V_{DD} = 10.0V$		90	225	ns
	$V_{DD} = 15.0V$		60	170	ns
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		600		ns
	$V_{DD} = 10.0V$		290		ns
	$V_{DD} = 15.0V$		200		ns
Minimum Retrigger Time Cx = 15 pF, Rx = 5.0 kΩ	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		
Cx = 1000 pF, Rx = 10 kΩ	$V_{DD} = 5.0V$		0		
	$V_{DD} = 10.0V$		0		
	$V_{DD} = 15.0V$		0		

Logic Diagram (½ of Device Shown)



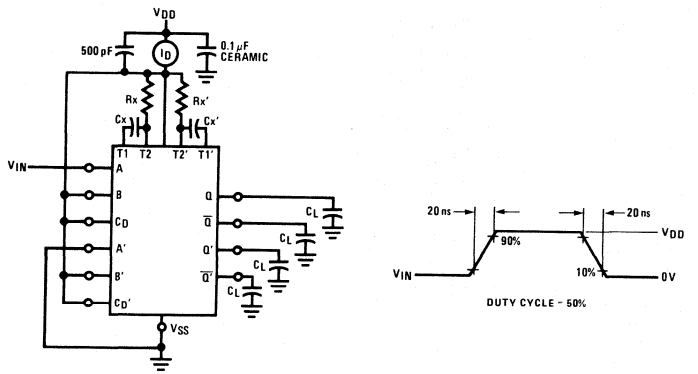
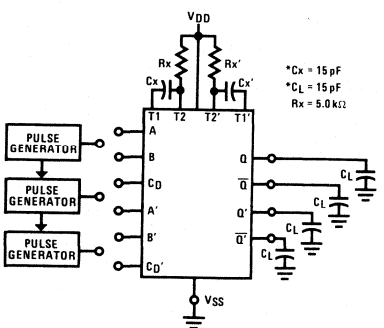


Figure 1. Power Dissipation Test Circuit and Waveforms



Input Connections

Characteristics	C_D	A	B
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_r, t_f, PW_{out}, PW_{in}	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, PW_{in}	PG3	PG1	PG2

*INCLUDES CAPACITANCE OF PROBES, WIRING, AND FIXTURE PARASITIC.

NOTE: AC TEST WAVEFORMS FOR PG1, PG2, AND PG3 ON NEXT PAGE.

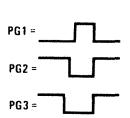


Figure 2. AC Test Circuit

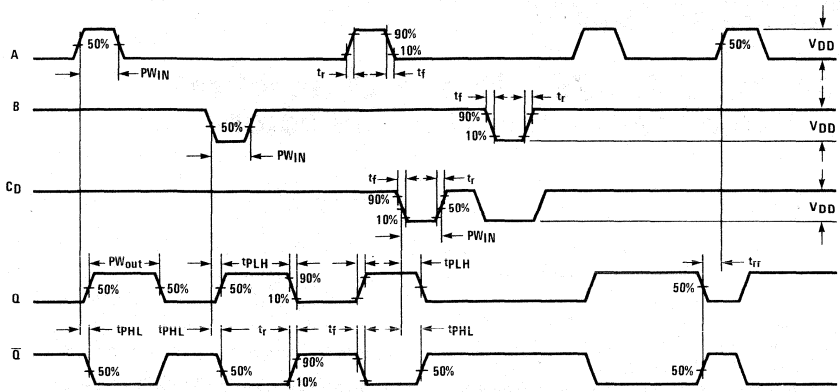


Figure 3. AC Test Waveforms

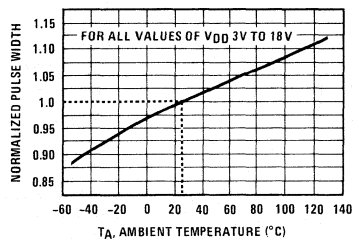


Figure 4. Normalized Pulse Width vs Temperature

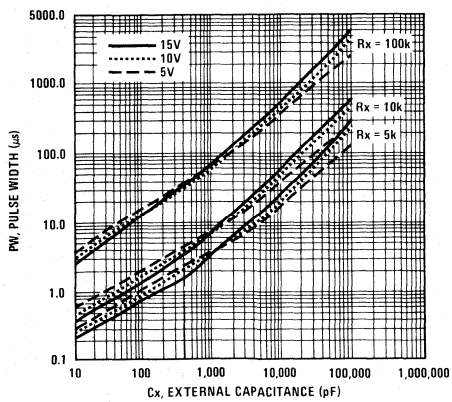


Figure 5. Pulse Width vs Cx

National Semiconductor

CD4529BM/CD4529BC Dual 4-Channel or Single 8-Channel Analog Data Selector

General Description

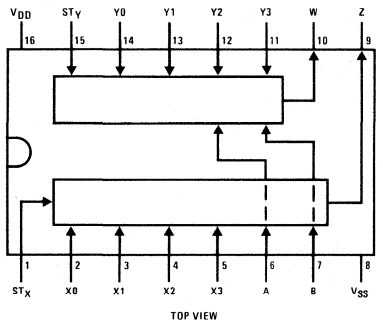
The CD4529B is a dual 4-channel or a single 8-channel analog data selector, implemented with complementary MOS (CMOS) circuits constructed with N and P-channel enhancement mode transistors. Dual 4-channel or 8-channel mode operation is selected by proper input coding, with outputs Z and W tied together for the single 8-bit mode. The device is suitable for digital as well as analog applications, including various 1-of-4 and 1-of-8 data selector functions. Since the device is analog and bidirectional, it can also be used for dual binary to 1-of-4 or single binary to 1-of-8 decoder applications.

Features

- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} typ
- Low quiescent power dissipation 0.005 μW/package typical @ 5 V_{DC}
- 10 MHz frequency operation (typical)
- Data paths are bidirectional
- Linear ON resistance (120Ω typical @ 15V)
- TRI-STATE® outputs (high impedance disable strobe)
- Plug-in replacement for MC14529B

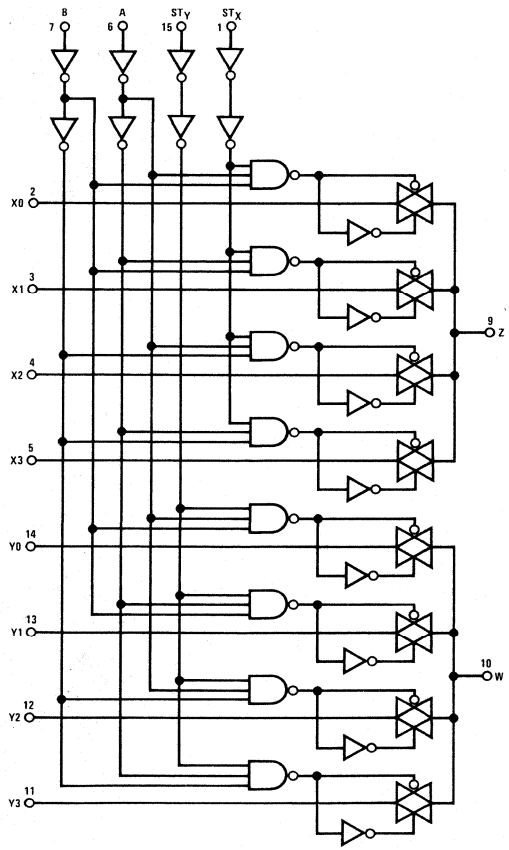
Connection Diagram

Dual-In-Line Package



TOP VIEW

Logic Diagram



Truth Table

ST_X	ST_Y	B	A	Z	W	
1	1	0	0	X0	Y0	Dual 4-Channel Mode 2 Outputs
1	1	0	1	X1	Y1	
1	1	1	0	X2	Y2	
1	1	1	1	X3	Y3	
1	0	0	0	X0		Single 8-Channel Mode 1 Output (Z and W tied together)
1	0	0	1	X1		
1	0	1	0	X2		
1	0	1	1	X3		
0	1	0	0	Y0		
0	1	0	1	Y1		
0	1	1	0	Y2		
0	1	1	1	Y3		
0	0	X	X	High Impedance (TRI-STATE®)		

X = Don't care

Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5V to +18V
V_{IN} Input Voltage	−0.5V to V_{DD} + 0.5V
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3V to 15V
V_{IN} Input Voltage	0 to V_{DD}
T_A Operating Temperature Range	
CD4529BM	−55°C to +125°C
CD4529BC	−40°C to +85°C

DC Electrical Characteristics CD4529BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		1.0		0.001	1.0		60	μA
		V_{DD} = 10V		1.0		0.002	1.0		60	μA
		V_{DD} = 15V		2.0		0.003	2.0		120	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5.0		4.95		V
		V_{DD} = 10V	9.95		9.95	10.0		9.95		V
		V_{DD} = 15V	14.95		14.95	15.0		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		400		165	480		640	Ω
		V_{IN} = −5V		400		100	480		640	Ω
		V_{IN} = ±0.25V		400		155	480		640	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		240		135	270		400	Ω
		V_{IN} = −7.5V		240		75	270		400	Ω
		V_{IN} = ±0.25V		240		100	270		400	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		400		165	480		640	Ω
		V_{IN} = 0.25V		400		100	480		640	Ω
		V_{IN} = 5.6V		400		160	480		640	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		400	Ω
		V_{IN} = 0.25V		250		75	270		400	Ω
		V_{IN} = 9.3V		250		110	270		400	Ω
I_{OFF}	Input to Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V, V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −5V, V_{DD} = 5V, V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±1250	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±2500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V, V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±2500	nA

DC Electrical Characteristics CD4529BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5.0		0.001	5.0		70	μA
		V_{DD} = 10V		5.0		0.002	5.0		70	μA
		V_{DD} = 15V		10.0		0.003	10.0		140	μA
V_{OL}	Low Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1$ μA								
		V_{DD} = 5V		0.05			0.05		0.05	V
		V_{DD} = 10V		0.05			0.05		0.05	V
		V_{DD} = 15V		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{IL} = 0V, V_{IH} = V_{DD}, $\|I_O\| < 1$ μA								
		V_{DD} = 5V	4.95		4.95	5.00		4.95		V
		V_{DD} = 10V	9.95		9.95	10.00		9.95		V
		V_{DD} = 15V	14.95		14.95	15.00		14.95		V
V_{IL}	Low Level Input Voltage (Note 3)	V_{DD} = 5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V		3.0		4.50	3.0		3.0	V
		V_{DD} = 15V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage (Note 3)	V_{DD} = 5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V	7.0		7.0	5.50		7.0		V
		V_{DD} = 15V	11.0		11.0	8.25		11.0		V
I_{IN}	Input Current	V_{DD} = 15V								
		V_{IN} = 0V		−0.3		-10^{-5}	−0.3		−1.0	μA
		V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA
R_{ON}	ON Resistance	V_{DD} = 5V, V_{SS} = −5V								
		V_{IN} = 5V		410		165	480		560	Ω
		V_{IN} = −5V		410		100	480		560	Ω
		V_{IN} = ±0.25V		410		155	480		560	Ω
		V_{DD} = 7.5V, V_{SS} = −7.5V								
		V_{IN} = 7.5V		250		135	270		350	Ω
		V_{IN} = −7.5V		250		75	270		350	Ω
		V_{IN} = ±0.25V		250		100	270		350	Ω
		V_{DD} = 10V, V_{SS} = 0V								
		V_{IN} = 10V		410		165	480		560	Ω
		V_{IN} = 0.25V		410		100	480		560	Ω
		V_{IN} = 5.6V		410		160	480		560	Ω
		V_{DD} = 15V, V_{SS} = 0V								
		V_{IN} = 15V		250		135	270		350	Ω
		V_{IN} = 0.25V		250		75	270		350	Ω
		V_{IN} = 9.3V		250		110	270		350	Ω
I_{OFF}	Input-Output Leakage Current	V_{SS} = −5V, V_{DD} = 5V								
		V_{IN} = 5V, V_{OUT} = −5V		±125		±0.001	±125		±500	nA
		V_{IN} = −5V, V_{OUT} = 5V		±125		±0.001	±125		±500	nA
		V_{SS} = −7.5V, V_{DD} = 7.5V								
		V_{IN} = 7.5V, V_{OUT} = −7.5V		±250		±0.0015	±250		±1000	nA
		V_{IN} = −7.5V, V_{OUT} = 7.5V		±250		±0.0015	±250		±1000	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Switch OFF is defined as $|I_O| \leq 10$ μA, switch ON as defined by R_{ON} specification.

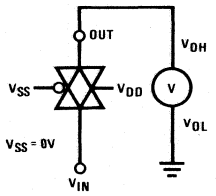
AC Electrical Characteristics CD4529BM/CD4529BC

$T_A = 25°C$, $R_L = 1\ k\Omega$, $t_r = t_f = 20$ ns, unless otherwise specified.

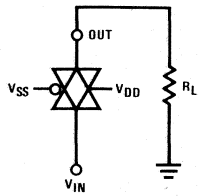
	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	V_{IN} to V_{OUT} Propagation Delay	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		20	40	ns
		$V_{DD} = 10V$		10	20	ns
		$V_{DD} = 15V$		8	15	ns
t_{PLH}, t_{PHL}	Control to Output Propagation Delay	$V_{IN} = V_{DD}$ or V_{SS}, $C_L = 50$ pF, $V_{IN} \leq 10V$				
		$V_{DD} = 5V$		200	400	ns
		$V_{DD} = 10V$		80	160	ns
		$V_{DD} = 15V$		50	120	ns
f_{MAX}	Maximum Control Input Pulse Frequency	$V_{SS} = 0V$, $C_L = 50$ pF				
		$V_{DD} = 5V$		5		MHz
		$V_{DD} = 10V$		10		MHz
		$V_{DD} = 15V$		12		MHz
	Crosstalk, Control to Output	$R_{OUT} = 10\ k\Omega$, $C_L = 50$ pF, $V_{SS} = 0$				
		$V_{DD} = 5V$		5.0		mV
		$V_{DD} = 10V$		5.0		mV
		$V_{DD} = 15V$		5.0		mV
	Noise Voltage	$f = 100$ Hz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		24		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		25		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		30		$nV/\sqrt{cycle}$
		$f = 100$ kHz, $V_{SS} = 0V$				
		$V_{DD} = 5V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 10V$		12		$nV/\sqrt{cycle}$
		$V_{DD} = 15V$		15		$nV/\sqrt{cycle}$
	Sine Wave (Distortion)	$V_{IN} = 1.77$Vrms Centered at 0V, $R_L = 10\ k\Omega$, $f = 1$ kHz, $V_{SS} = -5V$, $V_{DD} = 5V$		0.36		%
I_{LOSS}	Insertion Loss, $I_{LOSS} = 20\ Log_{10} \frac{V_{OUT}}{V_{IN}}$	$V_{IN} = 1.77$Vrms Centered at 0V, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$		2.0		dB
		$R_L = 10\ k\Omega$		0.8		dB
		$R_L = 100\ k\Omega$		0.25		dB
		$R_L = 1\ M\Omega$		0.01		dB
BW	Bandwidth, −3 dB	$V_{IN} = 1.77$Vrms Centered at 0 Vdc, $V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	35			MHz
		$R_L = 10\ k\Omega$	28			MHz
		$R_L = 100\ k\Omega$	27			MHz
		$R_L = 1\ M\Omega$	26			MHz
	Feedthrough and Crosstalk, $20\ Log_{10} \frac{V_{OUT}}{V_{IN}} = -50$ dB	$V_{SS} = -5V$, $V_{DD} = 5V$				
		$R_L = 1\ k\Omega$	850			kHz
		$R_L = 10\ k\Omega$	100			kHz
		$R_L = 100\ k\Omega$	12			kHz
		$R_L = 1\ M\Omega$	1.5			kHz

Test Circuits and Switching Time Waveforms

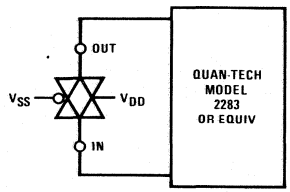
Output Voltage



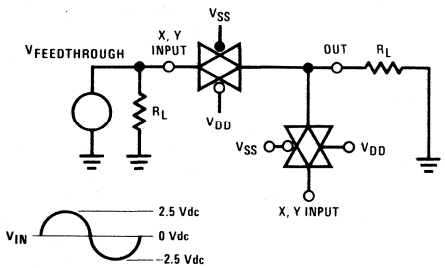
R_{ON} Characteristics



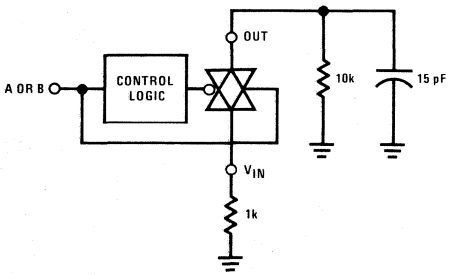
Noise Voltage



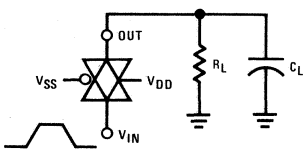
Frequency Response

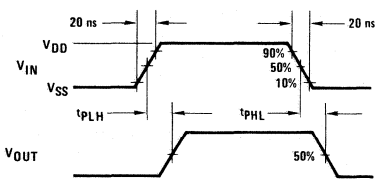


Crosstalk

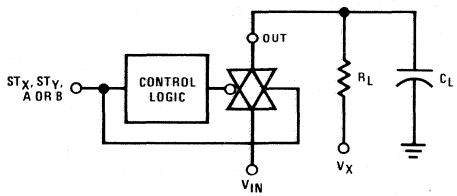


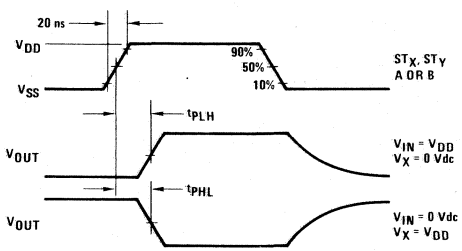
Propagation Delay





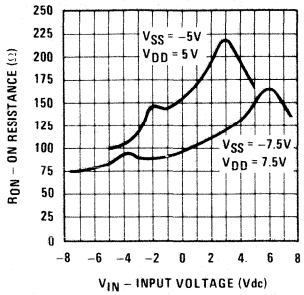
Turn-ON Delay Time



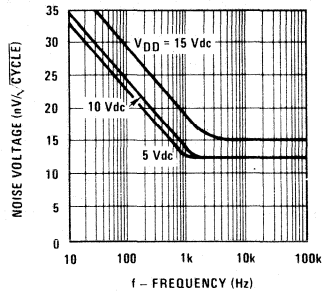


Typical Performance Characteristics

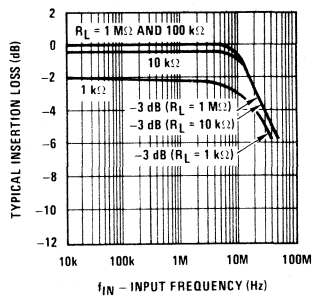
Typical R_{ON} vs V_{IN}



Typical Noise Characteristics



Typical Insertion Loss/ Bandwidth Characteristics



National Semiconductor

preliminary data

CD4538BM/CD4538BC Dual Monostable Multivibrator

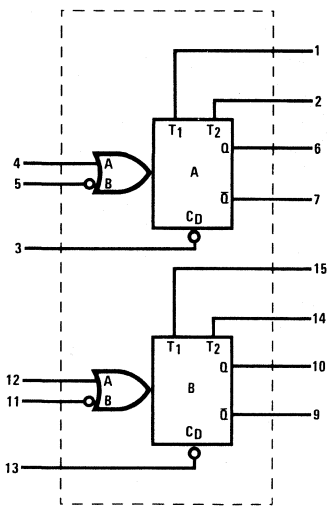
general description

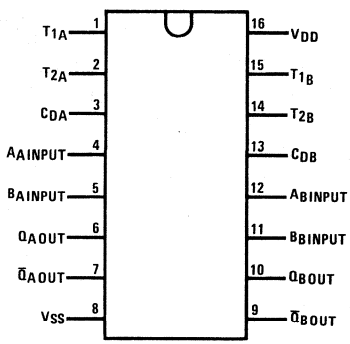
The CD4538 is a dual monostable multivibrator. Each device is retriggerable and resettable. Triggering can occur from either the rising or the falling edge of an input pulse, resulting in an accurate output pulse over a wide range of pulse widths. Pulse duration and accuracy are determined by external timing components R_X and C_X. Precise control of output pulse width has been added using linear CMOS techniques.

features

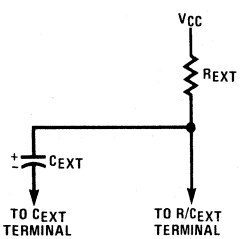
- Wide supply range — 3V to 18V
- ±0.5% typical pulse width variation from part to part
- ±0.5% typical pulse width variation over temperature range
- New formula: PW_{OUT} = RC (PW in seconds, R in ohms, C in Farads)
- Pulse width range — 1.0 μs to ∞
- Symmetrical output sink and source capability
- Separate latched reset inputs
- Quiescent current (standby) < 2 nA typical

logic and connection diagrams





timing components



truth table

Inputs			Outputs	
Clear	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

H = High level
L = Low level
↑ = Transition from low to high
↓ = Transition from high to low
⎍ = One high level pulse
⎎ = One low level pulse
X = Irrelevant

National Semiconductor

CD4543BM/CD4543BC BCD-to-7-Segment Latch/Decoder/Driver For Liquid Crystals

General Description

The CD4543BM/CD4543BC is a monolithic CMOS BCD-to-7-segment latch/decoder/driver for use with liquid crystal and other types of displays. The circuit provides the functions of a 4-bit storage latch and an 8421 BCD-to-7-segment decoder and driver. The device has the capability to invert the logic levels of the output combination. The phase (Ph), blanking (BI) and latch disable (LD) inputs are used to reverse the truth table phase, blank the display, and store a BCD code, respectively. For liquid crystal (LC) readouts, a square wave is applied to the Ph input of the circuit and the electrically common backplane of the display, the outputs of the circuit are connected directly to the segments of the LC readout. For other types of readouts. such as light-emitting diode (LED), incandescent, gas discharge, and fluorescent readouts, connection diagrams are given on this data sheet.

All inputs are protected against static discharge by diode clamps to V_{DD} and V_{SS}.

Applications

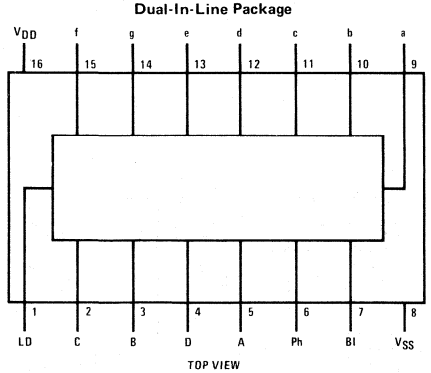
- Instrument (e.g., counter, DVM, etc.) display driver
- Computer/calculator display driver
- Cockput display driver
- Various clock, watch and timer uses

Features

- Wide supply voltage range — 3V to 18V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Low power dissipation — 50 nA/package typ at V_{DD} = 5V
- Latch storage
- Blanking input
- Blank for all illegal inputs
- Direct drive LCD, LED and VF displays
- Pin-for-pin replacement for CD4056B (with pin 7 tied to V_{SS})
- Pin-for-pin replacement for Motorola MC14543B

Connection Diagram and Truth Table

Dual-In-Line Package

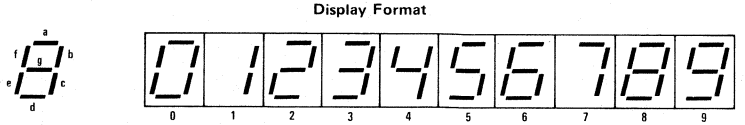


TOP VIEW

INPUTS							OUTPUTS							
LD	BI	Ph*	D	C	B	A	a	b	c	d	e	f	g	DISPLAY
X	1	0	X	X	X	X	0	0	0	0	0	0	0	Blank
1	0	0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	0	0	1	1	1	1	1	1	0	0	1	3
1	0	0	0	1	0	0	0	1	1	0	0	1	1	4
1	0	0	0	1	0	1	1	0	1	1	0	1	1	5
1	0	0	0	1	1	0	1	0	1	1	1	1	1	6
1	0	0	0	1	1	1	1	1	1	0	0	0	0	7
1	0	0	1	0	0	0	1	1	1	1	1	1	1	8
1	0	0	1	0	0	1	1	1	1	1	0	1	1	9
1	0	0	1	0	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	0	1	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	0	1	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	0	0	0	0	0	0	0	0	Blank
1	0	0	1	1	1	1	0	0	0	0	0	0	0	Blank
0	0	0	X	X	X	X	**							**
†	†	1	†				Inverse of Output Combinations Above							Display as Above

X = Don't care
† = Above combinations
* = For liquid crystal readouts, apply a square wave to Ph.
For common cathode LED readouts, select Ph = 0.
For common anode LED readouts, select Ph = 1.
** = Depends upon the BCD code previously applied when LD = 1.

Display Format



Absolute Maximum Ratings

(Notes 1 and 2)

V_{DD} DC Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

Recommended Operating Conditions

(Note 2)

V_{DD} DC Supply Voltage	3 V_{DC} to 15 V_{DC}
V_{IN} Input Voltage	0 to $V_{DD}V_{DC}$
T_A Operating Temperature Range	
CD4543BM	−55°C to +125°C
CD4543BC	−40°C to +85°C

DC Electrical Characteristics CD4543BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5			5		150	μA
		V_{DD} = 10V		10			10		300	μA
		V_{DD} = 15V		20			20		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4			2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.1		-10^{-5}	−0.1		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.1		10^{-5}	0.1		1.0	μA

DC Electrical Characteristics CD4543BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20			20		150	μA
		V_{DD} = 10V		40			40		300	μA
		V_{DD} = 15V		80			80		600	μA
V_{OL}	Low Level Output Voltage	V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5			1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0			3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5			3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0			7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0			11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44			0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1			0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0			2.4		mA

DC Electrical Characteristics CD4543BC (Note 2) (Continued)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44			−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1			−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0			−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.3		-10^{-5}	0.3		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.3		10^{-5}	0.3		1.0	μA

AC Electrical Characteristics T_A = 25°C, C_L = 50 pF, V_{SS} = 0, unless otherwise specified.

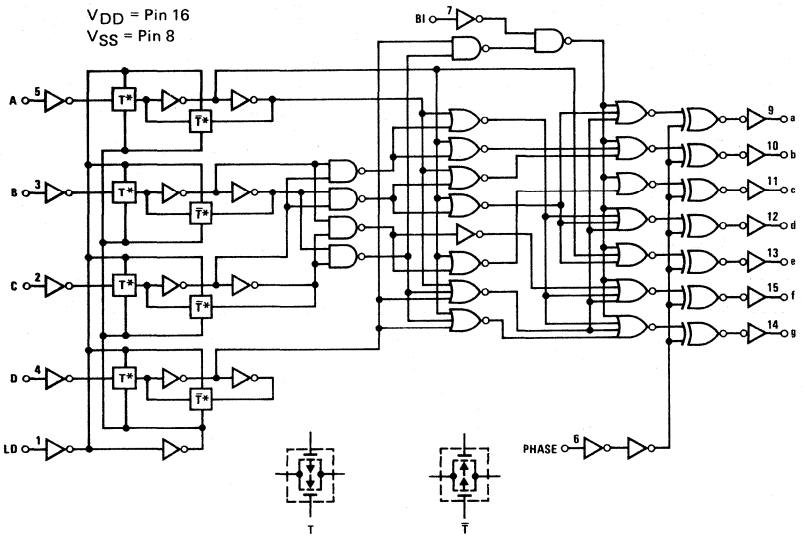
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Output Rise Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_f	Output Fall Time	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{PLH}	Turn-ON Propagation Delay Time	V_{DD} = 5V		450	1100	ns
		V_{DD} = 10V		170	440	ns
		V_{DD} = 15V		110	330	ns
t_{PHL}	Turn-OFF Propagation Delay Time	V_{DD} = 5V		500	1100	ns
		V_{DD} = 10V		180	440	ns
		V_{DD} = 15V		120	330	ns
$t_{SET\text{-}UP}$	Set-Up Time	V_{DD} = 5V		−5	80	ns
		V_{DD} = 10V		−2	30	ns
		V_{DD} = 15V		0	20	ns
t_{HOLD}	Hold Time	V_{DD} = 5V		30	120	ns
		V_{DD} = 10V		20	45	ns
		V_{DD} = 15V		15	30	ns
PW_{LD}	Latch Disable Pulse Width	V_{DD} = 5V		50	250	ns
		V_{DD} = 10V		30	100	ns
		V_{DD} = 15V		20	80	ns
C_{IN}	Input Capacitance	Per Input		5	7.5	pF
C_{PD}	Power Dissipation Capacitance	See C_{PD} Measurement Waveforms, (Note 3)		300		pF

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The tables of "Recommended Operating Conditions" and "Electrical Characteristics" provide conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: C_{PD} determines the no load AC power consumption of a CMOS device. For a complete explanation, see "MM54C/74C Family Characteristics" application note AN-90.

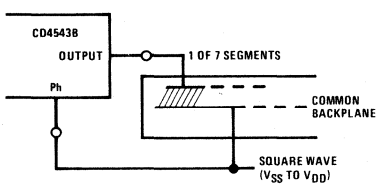
Logic Diagram



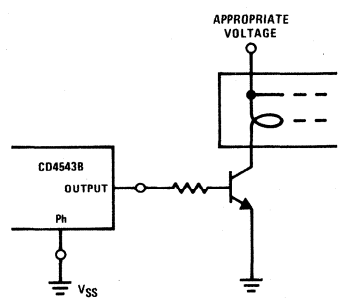
*Transmission gates

Typical Applications

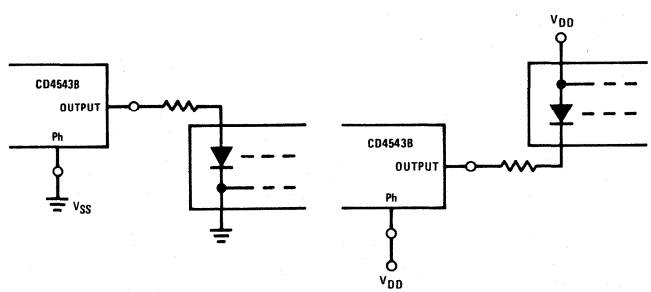
Liquid Crystal (LC) Readout



Incandescent Readout



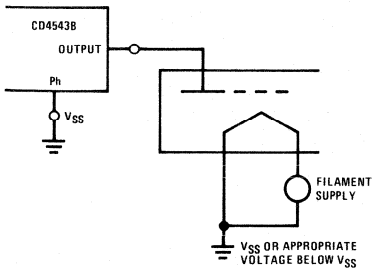
Light Emitting Diode (LED) Readout



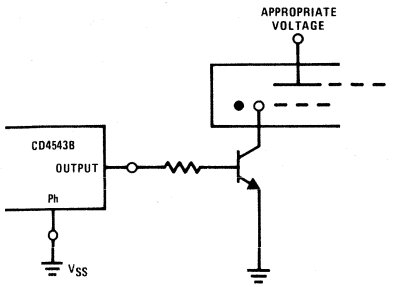
Note. Bipolar transistors may be added for gain (for $V_{DD} \leq 10V$ or $I_{OUT} \geq 10$ mA)

Typical Applications (Continued)

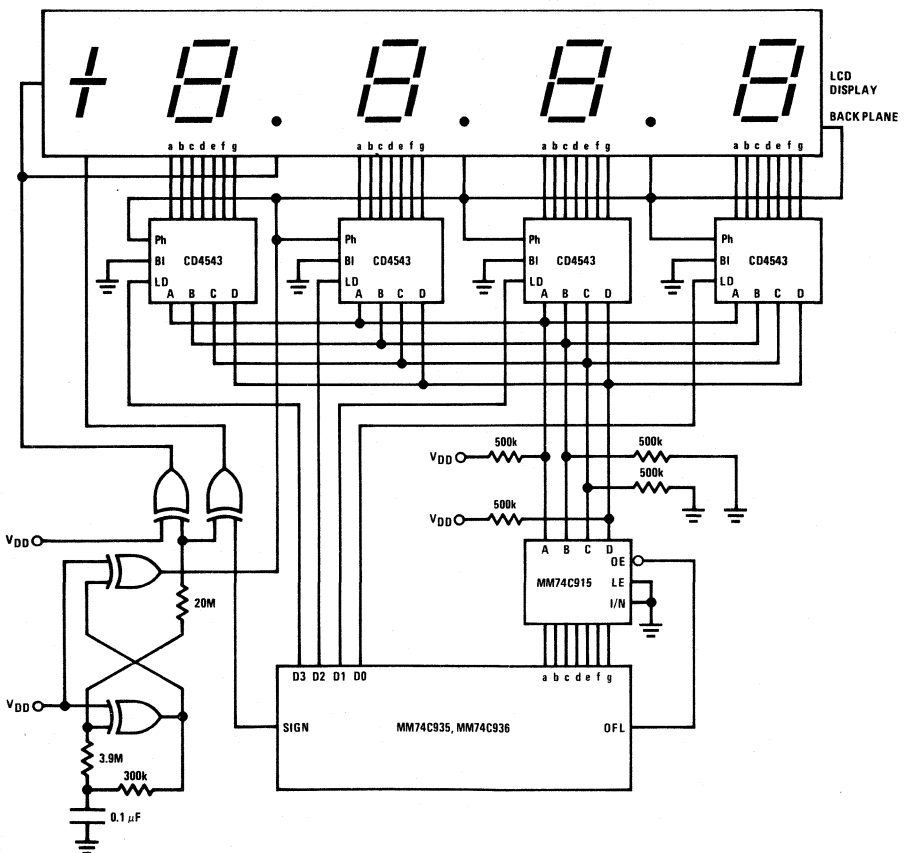
Fluorescent Readout



Gas Discharge Readout



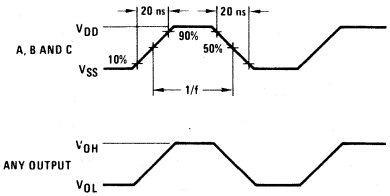
3 1/2-Digit DVM with LCD Display



Display 9.999 when overflowed. All digits can also be blanked at overflow by tying OFL to BI on the CD4543's

Switching Time Waveforms

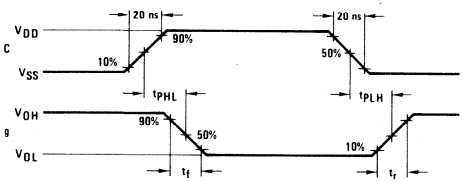
C_{PD} Measurement Waveforms



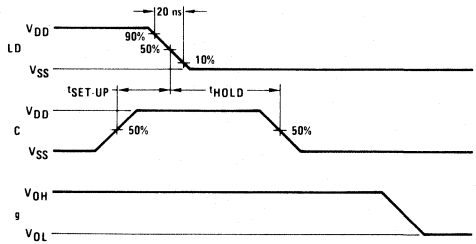
Inputs BI and Ph low, and inputs D and LD high. f in respect to a system clock.
All outputs connected to respective C_L loads.

Dynamic Signal Waveforms

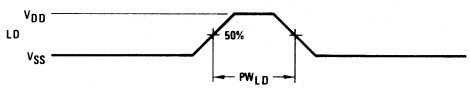
(a) Inputs D, Ph and BI low, and inputs A, B and LD high



(b) Inputs D, Ph and BI low, and inputs A and B high



(c) Data DCBA strobe into latches



National Semiconductor

CD4723BM/CD4723BC Dual 4-Bit Addressable Latch CD4724BM/CD4724BC, CD4099BM/CD4099BC 8-Bit Addressable Latches

general description

The CD4723B is a dual 4-bit addressable latch with common control inputs, including two address inputs (A0, A1), an active low enable input ($\overline{E}$) and an active high clear input (CL). Each latch has a data input (D) and four outputs (Q0–Q3). The CD4724B and CD4099B are 8-bit addressable latches with three address inputs (A0–A2), an active low enable input ($\overline{E}$), active high clear input (CL), a data input (D) and eight outputs (Q0–Q7).

Data is entered into a particular bit in the latch when that bit is addressed by the address inputs and the enable ($\overline{E}$) is low. Data entry in inhibited when enable ($\overline{E}$) is high.

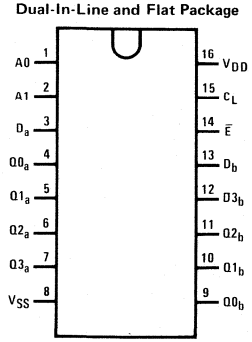
When clear (CL) and enable ($\overline{E}$) are high, all outputs are low. When clear (CL) is high, enable ($\overline{E}$) is low, the channel demultiplexing occurs. The bit that is addressed has an active output which follows the data input while all unaddressed bits are held low. When operating in the addressable latch mode ($\overline{E}$ = CL = low), changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode ($\overline{E}$ = high, CL = low).

features

- Wide supply voltage range — 3V to 15V
- High noise immunity — 0.45 V_{DD} typ
- Low power TTL compatibility — fan out of 2 driving 74L or 1 driving 74LS
- Serial to parallel capability
- Storage register capability
- Random (addressable) data entry
- Active high demultiplexing capability
- Common active high clear

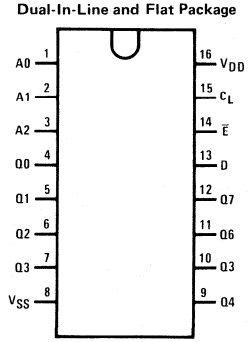
connection diagrams

CD4723B
Dual-In-Line and Flat Package



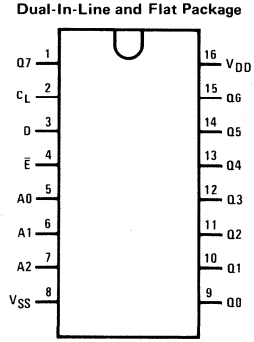
TOP VIEW

CD4724B
Dual-In-Line and Flat Package



TOP VIEW

CD4099B
Dual-In-Line and Flat Package



TOP VIEW

truth table

MODE SELECTION				
$\overline{E}$	CL	ADDRESSED LATCH	UNADDRESSED LATCH	MODE
L	L	Follows Data	Holds Previous Data	Addressable Latch
H	L	Holds Previous Data	Holds Previous Data	Memory
L	H	Follows Data	Reset to "0"	Demultiplexer
H	H	Reset to "0"	Reset to "0"	Clear

absolute maximum ratings

(Notes 1 and 2)

V_{DD} dc Supply Voltage	−0.5 to +18 V_{DC}
V_{IN} Input Voltage	−0.5 to V_{DD} +0.5 V_{DC}
T_S Storage Temperature Range	−65°C to +150°C
P_D Package Dissipation	500 mW
T_L Lead Temperature (Soldering, 10 seconds)	300°C

recommended operating conditions

(Note 2)

V_{DD} dc Supply Voltage	3 to 15 V_{DC}
V_{IN} Input Voltage	0 to V_{DD} V_{DC}
T_A Operating Temperature Range	
CD4723BM, CD4724BM, CD4099BM	−55°C to +125°C
CD4723BC, CD4724BC, CD4099BC	−40°C to +85°C

dc electrical characteristics CD4723BM, CD4724BM, CD4099BM (Note 2)

PARAMETER		CONDITIONS	−55°C		25°C			125°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		5		0.02	5		100	μA
		V_{DD} = 10V		10		0.02	10		200	μA
		V_{DD} = 15V		20		0.02	20		400	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.64		0.51	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.6		1.3	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	4.2		3.4	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.64		−0.51	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.6		−1.3	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−4.2		−3.4	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.10		-10^{-5}	−0.10		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.10		10^{-5}	0.10		1.0	μA

dc electrical characteristics CD4723BC, CD4724BC, CD4099BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{DD}	Quiescent Device Current	V_{DD} = 5V		20		0.02	20		150	μA
		V_{DD} = 10V		40		0.02	40		300	μA
		V_{DD} = 15V		80		0.02	80		600	μA
V_{OL}	Low Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V		0.05		0	0.05		0.05	V
		V_{DD} = 10V		0.05		0	0.05		0.05	V
		V_{DD} = 15V		0.05		0	0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| < 1\ \mu A$								
		V_{DD} = 5V	4.95		4.95	5		4.95		V
		V_{DD} = 10V	9.95		9.95	10		9.95		V
		V_{DD} = 15V	14.95		14.95	15		14.95		V
V_{IL}	Low Level Input Voltage	V_{DD} = 5V, V_O = 0.5 or 4.5V		1.5		2.25	1.5		1.5	V
		V_{DD} = 10V, V_O = 1V or 9V		3.0		4.5	3.0		3.0	V
		V_{DD} = 15V, V_O = 1.5V or 13.5V		4.0		6.75	4.0		4.0	V
V_{IH}	High Level Input Voltage	V_{DD} = 5V, V_O = 0.5V or 4.5V	3.5		3.5	2.75		3.5		V
		V_{DD} = 10V, V_O = 1V or 9V	7.0		7.0	5.5		7.0		V
		V_{DD} = 15V, V_O = 1.5V or 13.5V	11.0		11.0	8.25		11.0		V

dc electrical characteristics (Continued) CD4723BC, CD4724BC, CD4099BC (Note 2)

PARAMETER		CONDITIONS	−40°C		25°C			85°C		UNITS
			MIN	MAX	MIN	TYP	MAX	MIN	MAX	
I_{OL}	Low Level Output Current	V_{DD} = 5V, V_O = 0.4V	0.52		0.44	0.88		0.36		mA
		V_{DD} = 10V, V_O = 0.5V	1.3		1.1	2.25		0.9		mA
		V_{DD} = 15V, V_O = 1.5V	3.6		3.0	8.8		2.4		mA
I_{OH}	High Level Output Current	V_{DD} = 5V, V_O = 4.6V	−0.52		−0.44	−0.88		−0.36		mA
		V_{DD} = 10V, V_O = 9.5V	−1.3		−1.1	−2.25		−0.9		mA
		V_{DD} = 15V, V_O = 13.5V	−3.6		−3.0	−8.8		−2.4		mA
I_{IN}	Input Current	V_{DD} = 15V, V_{IN} = 0V		−0.30		-10^{-5}	−0.30		−1.0	μA
		V_{DD} = 15V, V_{IN} = 15V		0.30		10^{-5}	0.30		1.0	μA

ac electrical characteristics T_A = 25°C, C_L = 50 pF, R_L = 200k, Input $t_r = t_f$ = 20 ns, unless otherwise specified

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
t_{PLH}, t_{PHL}	Propagation Delay Data to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		75	150	ns
		V_{DD} = 15V		50	100	ns
t_{PLH}, t_{PHL}	Propagation Delay Enable to Output	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		60	120	ns
t_{PHL}	Propagation Delay Clear to Output	V_{DD} = 5V		175	350	ns
		V_{DD} = 10V		80	160	ns
		V_{DD} = 15V		65	130	ns
t_{PLH}, t_{PHL}	Propagation Delay Address to Output	V_{DD} = 5V		225	450	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		75	150	ns
t_{THL}, t_{TLH}	Transition Time (Any Output)	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH}, t_{WL}	Minimum Data Pulse Width	V_{DD} = 5V		100	200	ns
		V_{DD} = 10V		50	100	ns
		V_{DD} = 15V		40	80	ns
t_{WH}, t_{WL}	Minimum Address Pulse Width	V_{DD} = 5V		200	400	ns
		V_{DD} = 10V		100	200	ns
		V_{DD} = 15V		65	125	ns
t_{WH}	Minimum Clear Pulse Width	V_{DD} = 5V		75	150	ns
		V_{DD} = 10V		40	75	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time Data to $\overline{E}$	V_{DD} = 5V		40	80	ns
		V_{DD} = 10V		20	40	ns
		V_{DD} = 15V		15	30	ns
t_H	Minimum Hold Time Data to $\overline{E}$	V_{DD} = 5V		60	120	ns
		V_{DD} = 10V		30	60	ns
		V_{DD} = 15V		25	50	ns
t_{SU}	Minimum Set-Up Time Address to $\overline{E}$	V_{DD} = 5V		−15	50	ns
		V_{DD} = 10V		0	30	ns
		V_{DD} = 15V		0	20	ns
t_H	Minimum Hold Time Address to $\overline{E}$	V_{DD} = 5V		−50	15	ns
		V_{DD} = 10V		−20	10	ns
		V_{DD} = 15V		−15	5	ns
C_{PD}	Power Dissipation Capacitance	Per Package (Note 3)		100		pF
C_{IN}	Input Capacitance	Any Input		5	7.5	pF

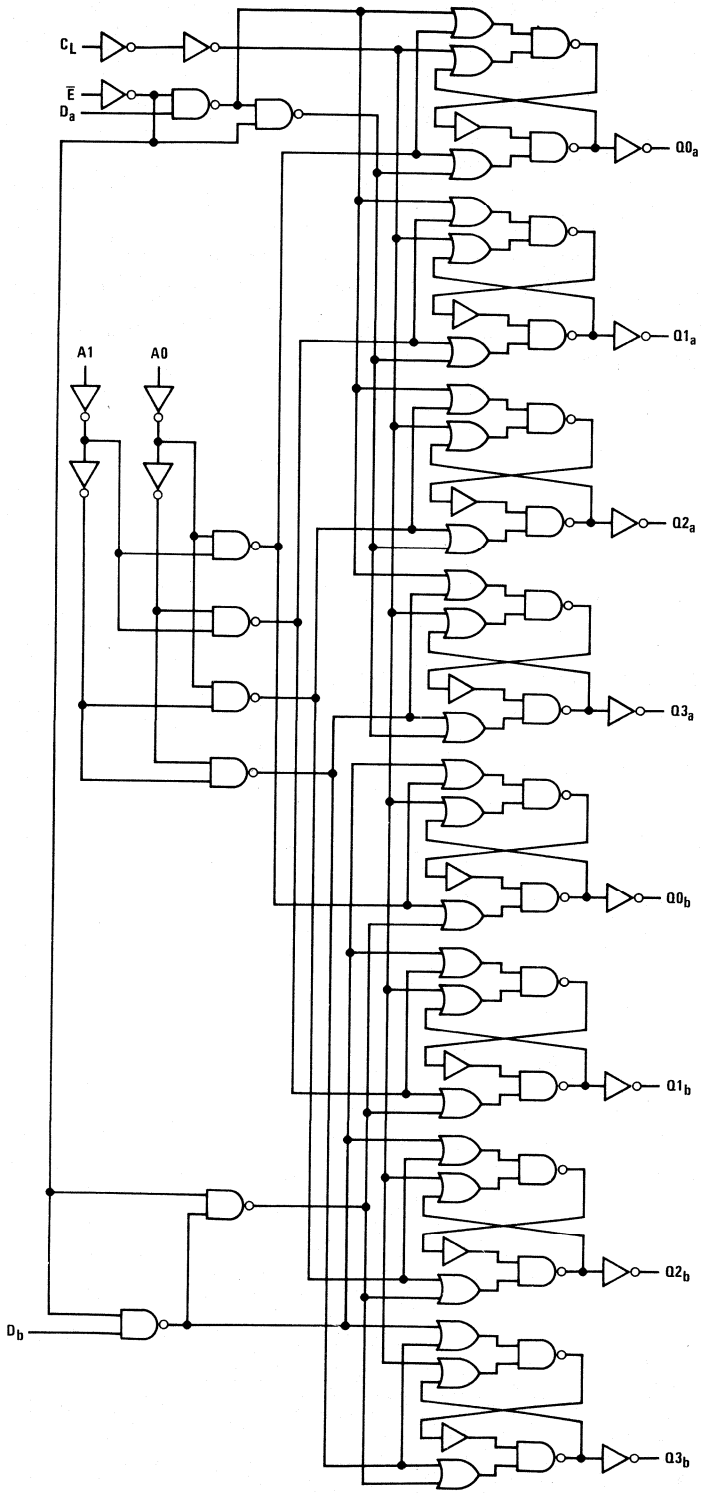
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed; they are not meant to imply that the devices should be operated at these limits. The table of "Recommended Operating Conditions" and "Electrical Characteristics" provides conditions for actual device operation.

Note 2: V_{SS} = 0V unless otherwise specified.

Note 3: Dynamic power dissipation (P_D) is given by: $P_D = (C_{PD} + C_L) V_{CC}^2 f + P_Q$; where C_L = load capacitance; f = frequency of operation; for further details, see application note AN-90, "54C/74C Family Characteristics".

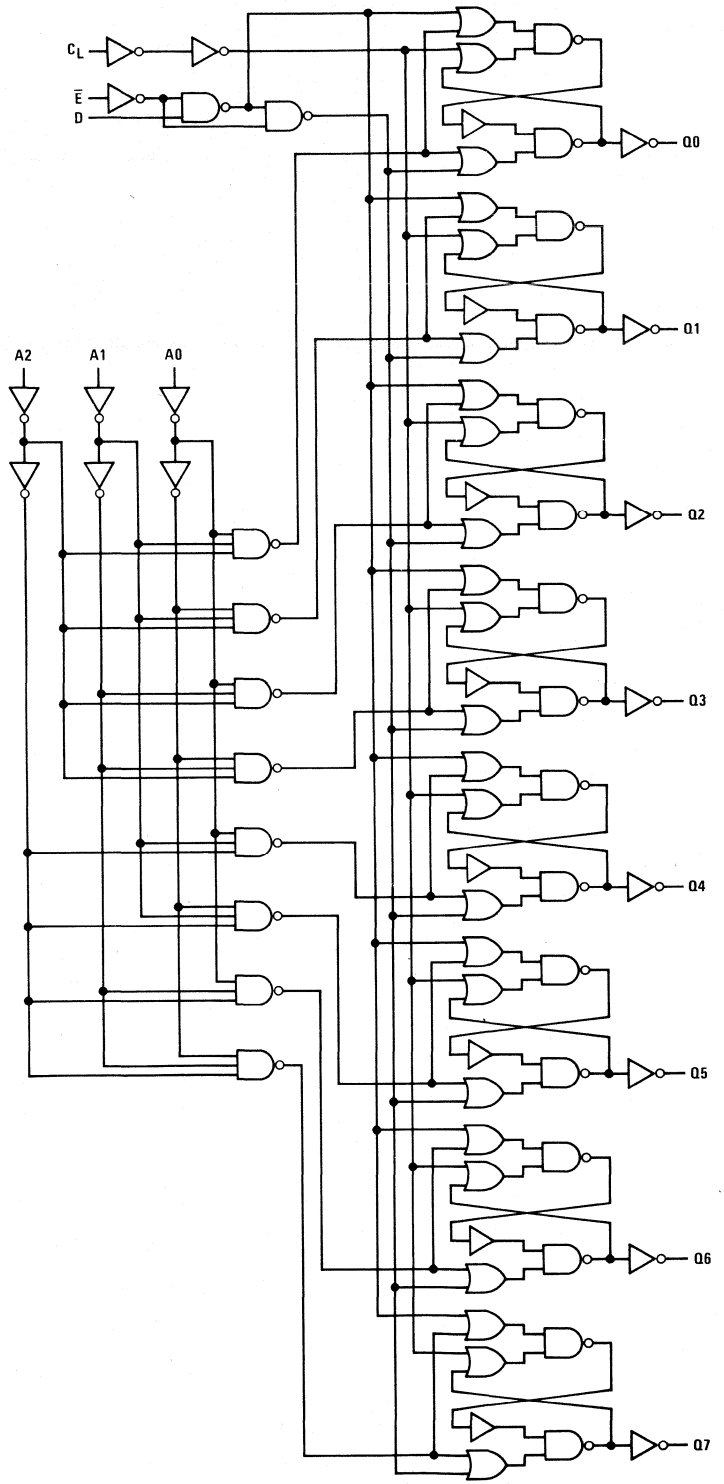
logic diagrams

CD4723B

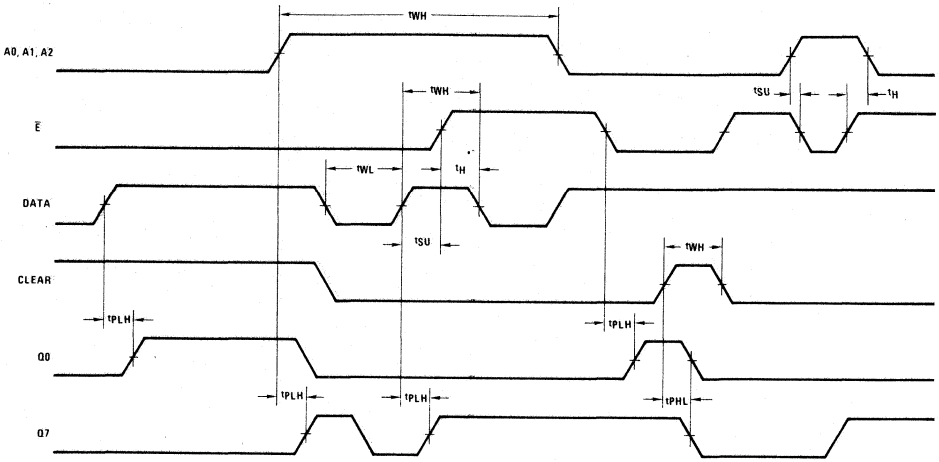


logic diagrams (Continued)

CD4724B, CD4099B



switching time waveforms



Compatible Bipolar Interface Circuits

National Semiconductor

DS1630/DS3630 Hex CMOS Compatible Buffer

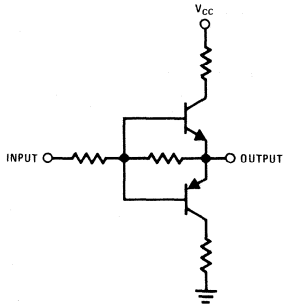
general description

The DS1630/DS3630 is a high current buffer intended for use with CMOS circuits interfacing with peripherals requiring high drive currents. The DS1630/DS3630 features low quiescent power consumption (typically 50μW) as well as high-speed driving of capacitive loads such as large MOS memories. The design of the DS1630/DS3630 is such that V_{CC} current spikes commonly found in standard CMOS circuits cannot occur, thereby, reducing the total transient and average power when operating at high frequencies.

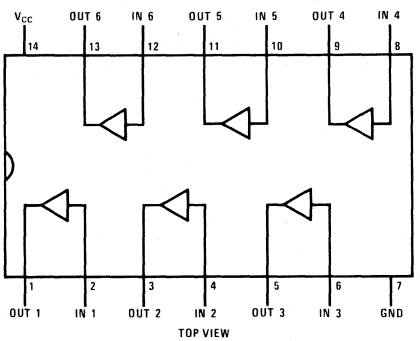
features

- High-speed capacitive driver
- Wide supply voltage range
- Input/output CMOS compatibility
- No internal transient V_{CC} current spikes
- 50μW typical standby power
- Fan out of 10 standard TTL loads

equivalent schematic and connection diagrams

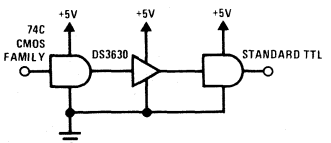


Dual-In-Line Package

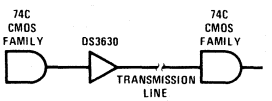


Order Number DS1630J, DS3630J or DS3630N

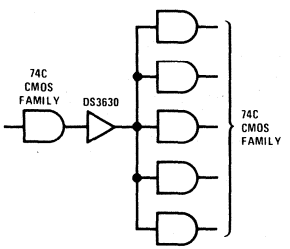
typical applications



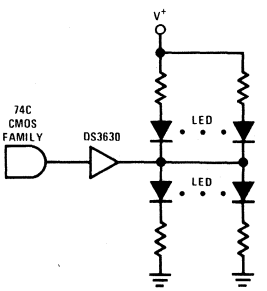
CMOS to TTL Interface



CMOS To Transmission Line Interface



CMOS To CMOS Interface



LED Driver

*Specifications may change.

absolute maximum ratings (Note 1)

Supply Voltage	16V
Input Voltage	16V
Output Voltage	16V
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	3	15	V
Temperature (T_A)			
DS1630	−55	+125	°C
DS3630	0	+70	°C

dc electrical characteristics (Notes 2 and 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{INH} Logical "1" Input Current	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630		90	200	μA
		DS3630		90	200	μA
	$V_{IN} = V_{CC} - 2.0V$, $I_{OUT} = 16$ mA	DS1630		0.5	3.2	mA
		DS3630		0.5	1.5	mA
I_{INL} Logical "0" Input Current	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		−0.15	−1	mA
		DS3630		$V_{CC}-150$	−800	μA
V_{OH} Logical "1" Output Voltage	$V_{IN} = V_{CC}$, $I_{OUT} = -400\mu A$	DS1630	$V_{CC}-1$	$V_{CC}-0.75$		V
		DS3630	$V_{CC}-0.9$	$V_{CC}-0.75$		V
	$V_{IN} = V_{CC} - 0.4V$, $I_{OUT} = 16$ mA	DS1630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
		DS3630	$V_{CC}-2.5$	$V_{CC}-2.0$		V
V_{OL} Logical "0" Output Voltage	$V_{IN} = 0V$, $I_{OUT} = 400\mu A$	DS1630		0.75	1	V
		DS3630		0.75	0.9	V
	$V_{IN} = 0V$, $I_{OUT} = 16$ mA	DS1630		0.95	1.3	V
		DS3630		0.95	1.3	V
	$V_{IN} = 0.4V$, $I_{OUT} = 16$ mA	DS1630		1.2	1.6	V
		DS3630		1.2	1.5	V

ac electrical characteristics $V_{CC} = 5.0V$, $T_A = 25°C$ unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
t_{pd0} Propagation Delay to a Logical "0"	$C_L = 50$ pF		30	45	ns
	$C_L = 250$ pF		40	60	ns
	$C_L = 500$ pF		50	75	ns
t_{pd1} Propagation Delay to a Logical "1"	$C_L = 50$ pF		15	25	ns
	$C_L = 250$ pF		35	50	ns
	$C_L = 500$ pF		50	75	ns

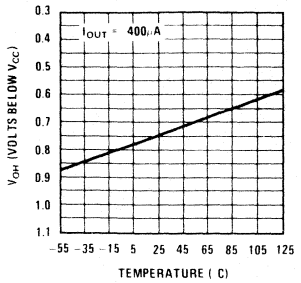
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1630 and across the 0°C to +70°C range for the DS3630. All typicals are given for $V_{CC} = 5.0V$ and $T_A = 25°C$.

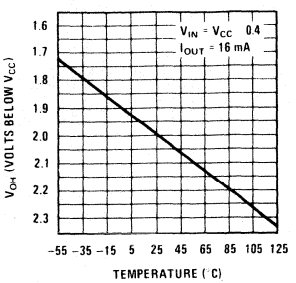
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

typical performance characteristics

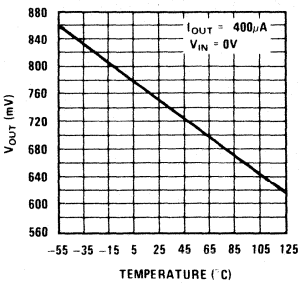
V_{OH} vs Temperature, $V_{IN} = V_{CC}$



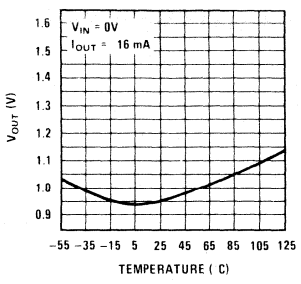
V_{OH} Active vs Temperature



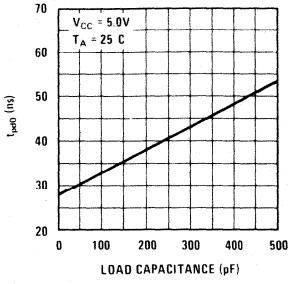
V_{OL} vs Temperature



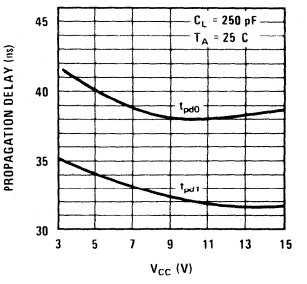
V_{OL} vs Temperature



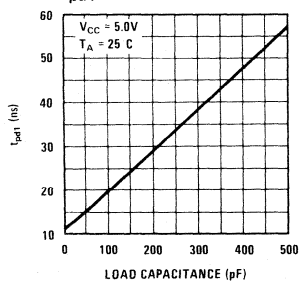
t_{pdo} vs Load Capacitance



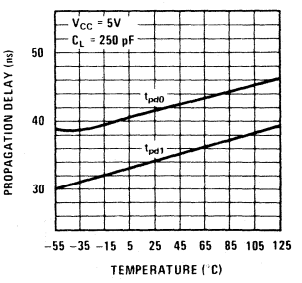
Propagation Delay vs V_{CC}



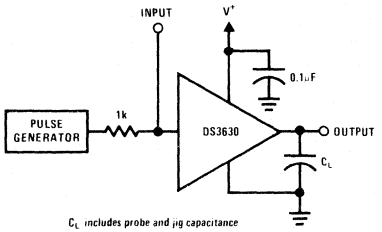
t_{pd1} vs Load Capacitance



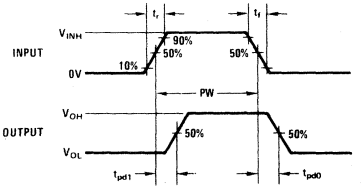
Propagation Delay vs Temperature



ac test circuit and switching time waveforms



C_L includes probe and jig capacitance



Pulse Generator characteristics: PRR = 1.0 MHz, PW = 500 ns, $t_r = t_f < 10$ ns, V_{IN} = 0 to V_{CC}

National Semiconductor

DS1631/DS3631, DS1632/DS3632, DS1633/DS3633, DS1634/DS3634 CMOS Dual Peripheral Drivers

general description

The DS1631 series of dual peripheral drivers was designed to be a universal set of interface components for CMOS circuits.

Each circuit has CMOS compatible inputs with thresholds that track as a function of V_{CC} (approximately 1/2 V_{CC}). The inputs are PNPs providing the high impedance necessary for interfacing with CMOS.

Outputs have high voltage capability, minimum breakdown voltage is 56V at 250μA.

The outputs are Darlington connected transistors. This allows high current operation (300 mA max) at low internal V_{CC} current levels since base drive for the output transistor is obtained from the load in proportion to the required loading conditions. This is essential in order to minimize loading on the CMOS logic supply.

Typical V_{CC} = 5V power is 28 mW with both outputs ON. V_{CC} operating range is 4.5V to 15V.

The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance OFF state with the same breakdown levels as when V_{CC} was applied.

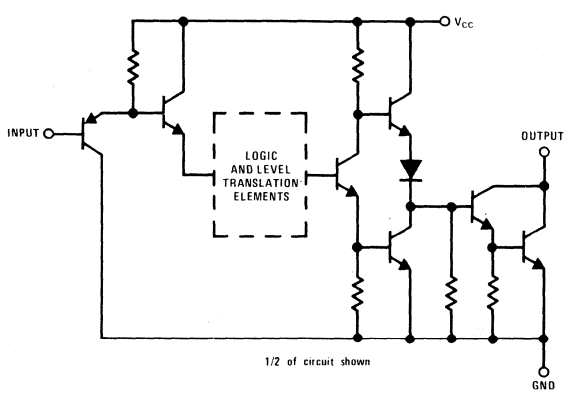
Pin-outs are the same as the respective logic functions found in the following popular series of circuits: DS75451, DS75461, DS3611. This feature allows direct conversion of present systems to the DM74C CMOS family and DS1631 series circuits with great power savings.

The DS1631 series is also TTL/DTL compatible at V_{CC} = 5V.

features

- CMOS compatible inputs
- TTL/DTL compatible inputs
- High impedance inputs — PNP's
- High output voltage breakdown — 56V min
- High output current capability — 300 mA max
- Same pin-outs and logic functions as DS75451, DS75461 and DS3611 series circuits
- Low V_{CC} power dissipation (28 mW both outputs "ON" at 5V)

schematic diagram (Equivalent Circuit)



SEE CONNECTION DIAGRAMS FOR ORDERING INFORMATION

absolute maximum ratings (Note 1)

Supply Voltage	16V
Voltage at Inputs	−0.3V to V_{CC} +0.3V
Output Voltage	56V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1631/DS1632/ DS1633/DS1634	4.5	15	V
DS3631/DS3632/ DS3633/DS3634	4.75	15	V
Temperature, T_A			
DS1631/DS1632/ DS1633/DS1634	−55	+125	°C
DS3631/DS3632/ DS3633/DS3634	0	+70	°C

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
All Circuits								
V_{IH}	Logical "1" Input Voltage	*(Figure 1)*	V_{CC} = 5V		3.5	2.5		V
			V_{CC} = 10V		8.0	5		V
			V_{CC} = 15V		12.5	7.5		V
V_{IL}	Logical "0" Input Voltage	*(Figure 1)*	V_{CC} = 5V			2.5	1.5	V
			V_{CC} = 10V			5.5	2.0	V
			V_{CC} = 15V			7.5	2.5	V
I_{IH}	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V, *(Figure 2)*				0.1		μA
I_{IL}	Logical "0" Input Current	V_{IN} = 0.4V, *(Figure 3)*	V_{CC} = 5V			−50		μA
			V_{CC} = 15V			−200		μA
V_{OH}	Output Breakdown Voltage	V_{CC} = 15V, I_{OH} = 250μA, *(Figure 1)*			56	65		V
V_{OL}	Output Low Voltage	V_{CC} = Min, *(Figure 1)*	I_{OL} = 100 mA			0.9		V
			I_{OL} = 300 mA			1.1		V
DS1631/DS3631								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7		mA
			V_{CC} = 15V	Both Drivers		14		mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
			V_{CC} = 15V, V_{IN} = 15V	Both Drivers		7.5		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1632/DS3632								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		8		mA
			V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		2.5		mA
			V_{CC} = 15V			9		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
DS1633/DS3633								
$I_{CC(0)}$	Supply Currents	V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output Low		7.5		mA
			V_{CC} = 15V			16		mA
$I_{CC(1)}$		*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output High		2		mA
			V_{CC} = 15V, V_{IN} = 15V			7.2		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				200		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

electrical characteristics (con't)

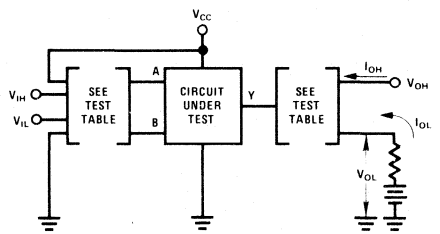
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
DS1634/DS3634								
$I_{CC(0)}$	Supply Currents	*(Figure 4)*	V_{CC} = 5V, V_{IN} = 5V	Output Low		7.5		mA
			V_{CC} = 15V, V_{IN} = 15V			18		mA
$I_{CC(1)}$		V_{IN} = 0V, *(Figure 4)*	V_{CC} = 5V	Output High		3		mA
			V_{CC} = 15V			11		mA
t_{pd1}	Propagation to "1"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns
t_{pd0}	Propagation to "0"	V_{CC} = 5.0V, T_A = 25°C, C_L = 15 pF, R_L = 50Ω, V_L = 10V, *(Figure 5)*				150		ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1631, DS1632, DS1633 and DS1634 and across the 0°C to +70°C range for the DS3631, DS3632, DS3633 and DS3634. All typical values are for T_A = 25°C.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

test circuits



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
LM3611	V_{IH}	V_{IH}	I_{OH}	V_{OH}
	V_{IL}	V_{CC}	I_{OL}	V_{OL}
LM3612	V_{IH}	V_{IH}	I_{OL}	V_{OL}
	V_{IL}	V_{CC}	I_{OH}	V_{OH}
LM3613	V_{IH}	GND	I_{OH}	V_{OH}
	V_{IL}	V_{IL}	I_{OL}	V_{OL}
LM3614	V_{IH}	GND	I_{OL}	V_{OL}
	V_{IL}	V_{IL}	I_{OH}	V_{OH}

Note: Each input is tested separately.

FIGURE 1. V_{IH}, V_{IL}, V_{OH}, V_{OL}

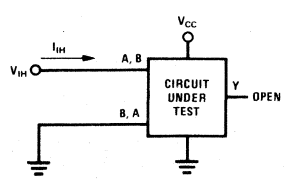
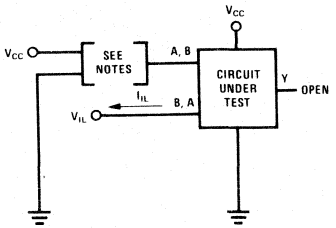


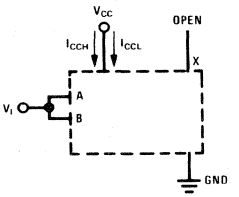
FIGURE 2. I_{IH}

test circuits (con't) and switching time waveforms



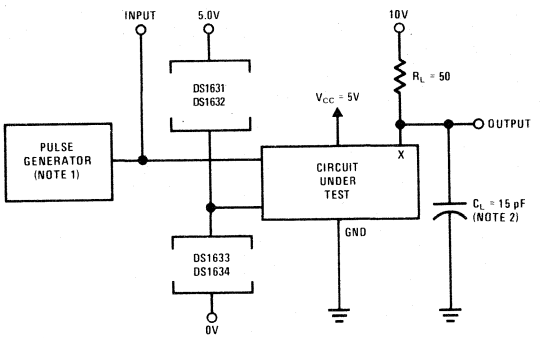
Note A: Each input is tested separately.
Note B: When testing DS1633 and DS1634 input not under test is grounded. For all other circuits it is at V_{CC}.

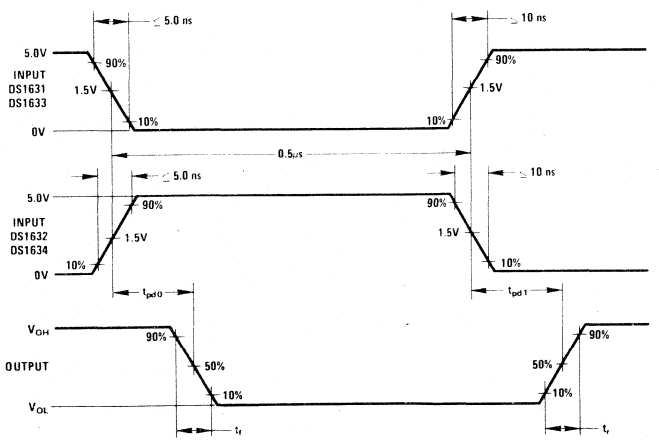
FIGURE 3. I_{IL}



Both gates are tested simultaneously.

FIGURE 4. I_{CC}



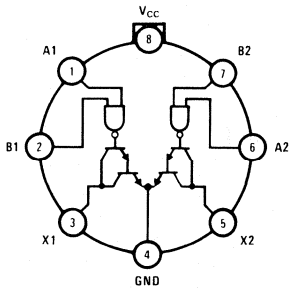


Note 1: The pulse generator has the following characteristics: PRR = 500 kHz, Z_{OUT} = 50Ω.
Note 2: C_L includes probe and jig capacitance.

FIGURE 5. Switching Times.

connection diagrams, truth tables and ordering information

DS1631
Metal Can Package

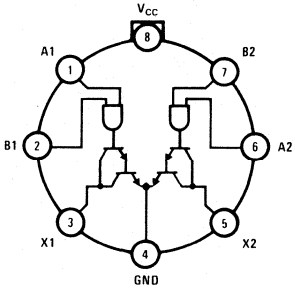


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1631H/DS3631H

DS1632
Metal Can Package

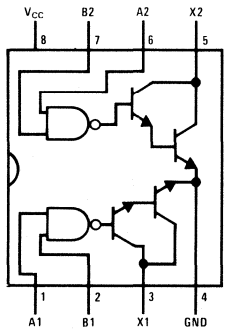


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1632H/DS3632H

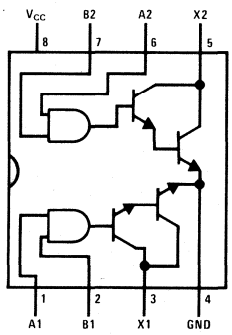
Dual-In-Line Package



TOP VIEW

Order Number 3631N

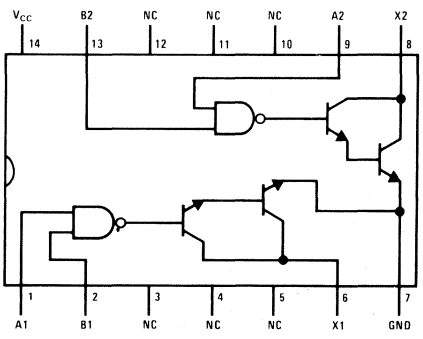
Dual-In-Line Package



TOP VIEW

Order Number DS3632N

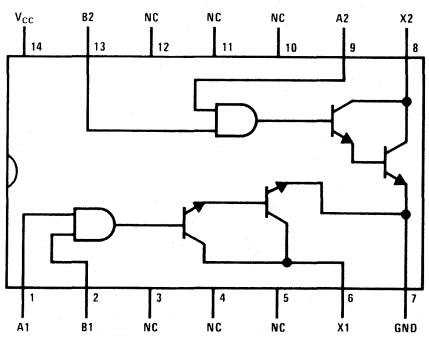
Dual-In-Line Package



TOP VIEW

Order Number DS1631J/DS3631J

Dual-In-Line Package



TOP VIEW

Order Number DS1632J/DS3632J

Positive logic: AB=X

A	B	OUTPUT X
0	0	0
1	0	0
0	1	0
1	1	1

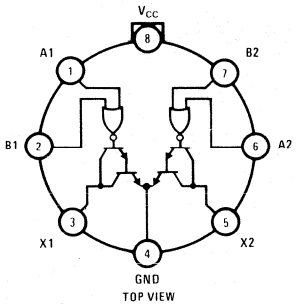
Positive logic: $\overline{AB}$=X

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

connection diagrams, truth tables and ordering information

DS1633

Metal Can Package

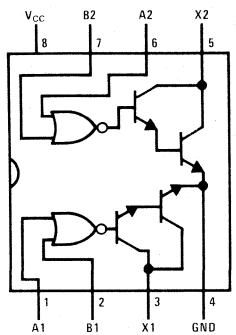


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1633H/DS3633H

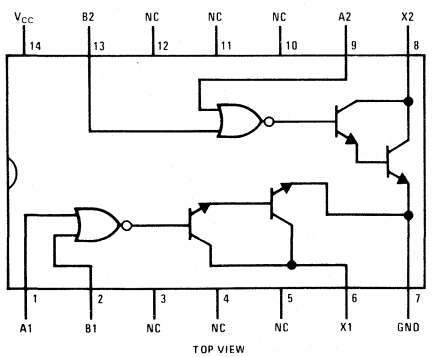
Dual-In-Line Package



TOP VIEW

Order Number DS3633N

Dual-In-Line Package



TOP VIEW

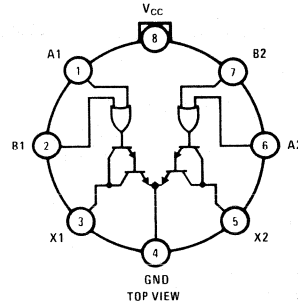
Order Number DS1633J/DS3633J

Positive logic: A + B = X

A	B	OUTPUT X
0	0	0
1	0	1
0	1	1
1	1	1

DS1634

Metal Can Package

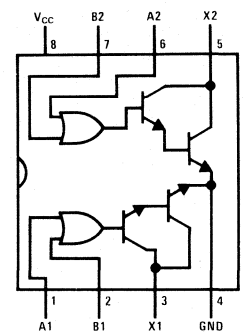


TOP VIEW

(Pin 4 is electrically connected to the case.)

Order Number DS1634H/DS3634H

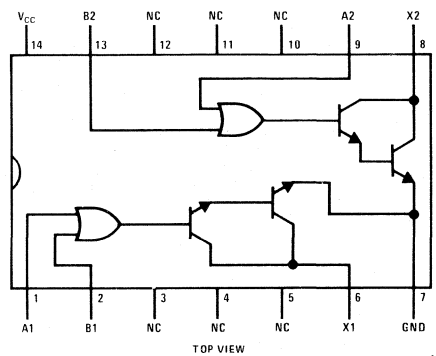
Dual-In-Line Package



TOP VIEW

Order Number DS3634N

Dual-In-Line Package



TOP VIEW

Order Number DS1634J/DS3634J

Positive logic: $\overline{A + B} = X$

A	B	OUTPUT X
0	0	1
1	0	0
0	1	0
1	1	0

National Semiconductor

DS1686/DS3686 Positive Voltage Relay Driver

general description

The DS1686/DS3686 is a high voltage/current positive voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of 54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at 5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

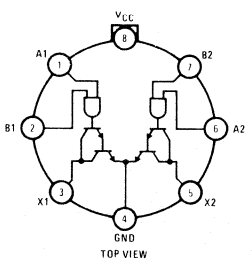
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

connection diagrams

Metal Can Package

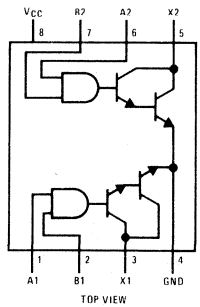


TOP VIEW

Pin 4 is in electrical contact with the case

Order Number DS1686H or DS3686H

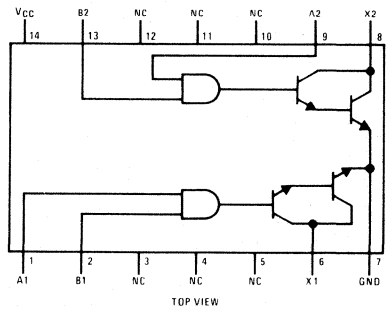
Dual-In-Line Package



TOP VIEW

Order Number DS3686N

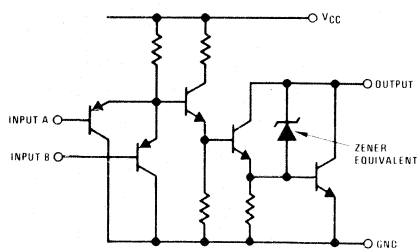
Dual-In-Line Package



TOP VIEW

Order Number DS1686J or DS3686J

schematic diagram



truth table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1686	4.5	5.5	V
DS3686	4.75	5.25	V
Temperature, T_A			
DS1686	−55	+125	°C
DS3686	0	+70	°C

electrical characteristics (Notes 2 and 3)

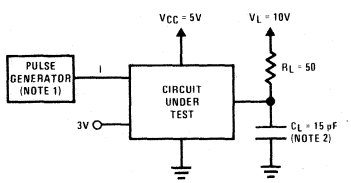
PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				0.01	40	μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−60	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = 5 mA			56	65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = 54V				0.5	250	μA
V_{OL}	Output "ON" Voltage	V_{CC} = Min, V_{IN} = 2V	I_{OUT} = 100μA	DS1686		0.85	1.1	V
				DS3686		0.85	1.0	V
			I_{OUT} = 300μA	DS1686		0.95	1.3	V
				DS3686		0.95	1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2.0	4.0	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18.0	28	mA
t_{pd0}	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				50		ns
t_{pd1}	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = 10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				1.0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1686 and across the 0°C to +70°C range for the DS3686. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

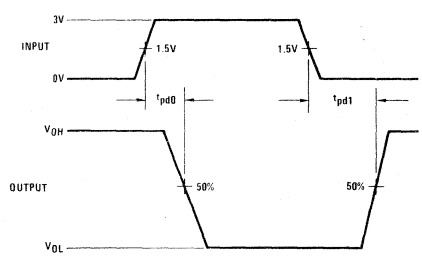
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \geq 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



National Semiconductor

DS1687/DS3687 Negative Voltage Relay Driver

general description

The DS1687/DS3687 is a high voltage/current negative voltage relay driver having many features not available in present relay drivers.

PNP inputs provide both TTL/DTL compatibility and high input impedance for low input loading.

Output leakage is specified over temperature at an output voltage of −54V. Minimum output breakdown (ac/latch breakdown) is specified over temperature at −5 mA. This clearly defines the actual breakdown of the device since the circuit has incorporated in it an internal reference which does not allow output breakdown latching found in existing relay drivers. Additionally, this internal reference circuit feature will eliminate the need in most cases of an external clamping (inductive transient voltage protection) diode. When the output is turned "OFF" by input logic conditions the resulting inductive voltage transient seen at the output is detected by an internal zener reference. The reference then momentarily activates the output transistor long enough so that the relay energy is discharged. This feature eliminates the need of external circuit protection components and insures output transistor protection.

The outputs are Darlington connected transistors, which allow high current operation at low internal V_{CC} current levels—base drive for the output transistor is obtained from the load in proportion to the required loading conditions. Typical V_{CC} power with both outputs "ON" is 90 mW.

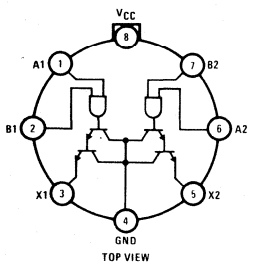
The circuit also features output transistor protection if the V_{CC} supply is lost by forcing the output into the high impedance "OFF" state with the same breakdown levels as when V_{CC} was applied.

features

- TTL/DTL/CMOS compatible inputs
- High impedance inputs (PNP's)
- High output voltage breakdown (−65V typ)
- High output current capability (300 mA max)
- Internal protection circuit eliminates need for output protection diode in most applications
- Output breakdown protection if V_{CC} supply is lost
- Low V_{CC} power dissipation (90 mW (typ) both outputs "ON")
- Voltage and current levels compatible for use in telephone relay applications

connection diagrams

Metal Can Package

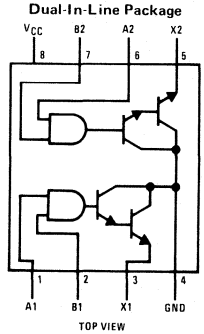


TOP VIEW

Pin 4 is in electrical contact with the case

Order Number DS1687H or DS3687H

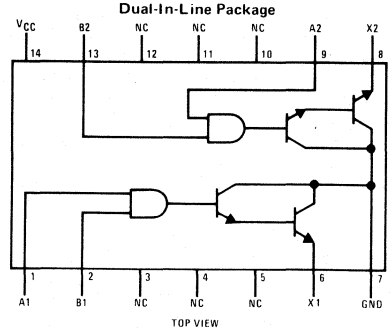
Dual-In-Line Package



TOP VIEW

Order Number DS3687N

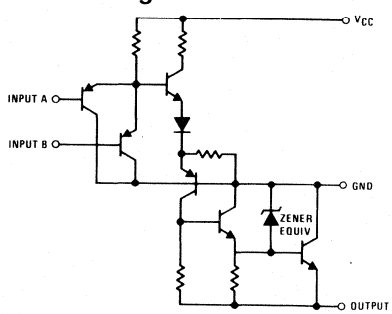
Dual-In-Line Package



TOP VIEW

Order Number DS1687J or DS3687J

schematic diagram



truth table

Positive logic: $\overline{AB} = X$

A	B	OUTPUT X
0	0	1
1	0	1
0	1	1
1	1	0

Logic "0" output "ON"
Logic "1" output "OFF"

absolute maximum ratings (Note 1)

Supply Voltage	7V
Input Voltage	15V
Output Voltage	56V
Storage Temperature Range	65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage, V_{CC}			
DS1687	4.5	5.5	V
DS3687	4.75	5.25	V
Temperature, T_A			
DS1687	−55	+125	°C
DS3687	0	+70	°C

electrical characteristics (Notes 2 and 3)

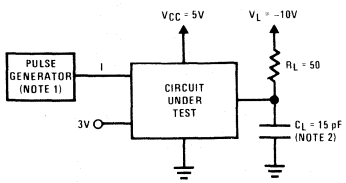
	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	Logical "1" Input Voltage				2.0			V
I_{IH}	Logical "1" Input Current	V_{CC} = Max, V_{IN} = 5.5V				0.01	40	μA
V_{IL}	Logical "0" Input Voltage						0.8	V
I_{IL}	Logical "0" Input Current	V_{CC} = Max, V_{IN} = 0.4V				−60	−250	μA
V_{CD}	Input Clamp Voltage	V_{CC} = 5V, I_{CLAMP} = −12 mA, T_A = 25°C				−1.0	−1.5	V
V_{OH}	Output Breakdown	V_{CC} = Max, V_{IN} = 0V, I_{OUT} = −5 mA			−56	−65		V
I_{OH}	Output Leakage	V_{CC} = Max, V_{IN} = 0V, V_{OUT} = −54V				−0.5	−250	μA
V_{OL}	Output "ON" Voltage	V_{CC} = Min, V_{IN} = 2V	I_{OUT} = 100 mA	DS1687		−0.85	−1.1	V
				DS3687		−0.85	−1.0	V
			I_{OUT} = 300 mA	DS1687		−0.95	−1.3	V
				DS3687		−0.95	−1.2	V
$I_{CC(1)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 0V, Outputs Open				2.0	4.0	mA
$I_{CC(0)}$	Supply Current (Both Drivers)	V_{CC} = Max, V_{IN} = 3V, Outputs Open				18.0	28	mA
$t_{pd(ON)}$	Propagation Delay to a Logical "0" (Output Turn "ON")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				50		ns
$t_{pd(OFF)}$	Propagation Delay to a Logical "1" (Output Turn "OFF")	C_L = 15 pF, V_L = −10V, R_L = 50Ω, T_A = 25°C, V_{CC} = 5.0V				1.0		μs

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS1687 and across the 0°C to +70°C range for the DS3687. All typicals are given for V_{CC} = 5.0V and T_A = 25°C.

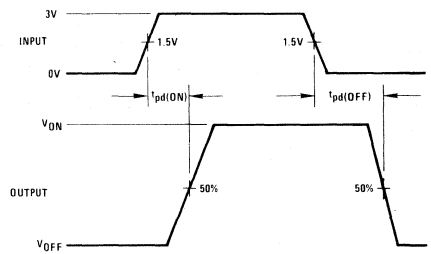
Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

ac test circuit and switching time waveforms



Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, 50% duty cycle, $Z_{OUT} \geq 50\Omega$, $t_r = t_f \leq 10$ ns.

Note 2: C_L includes probe and jig capacitance.



National Semiconductor

DS78C20/DS88C20 Dual CMOS Compatible Differential Line Receiver

general description

The DS78C20 and DS88C20 are high performance, dual differential, CMOS compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA and Federal Standards.

Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver, and the pinout is identical.

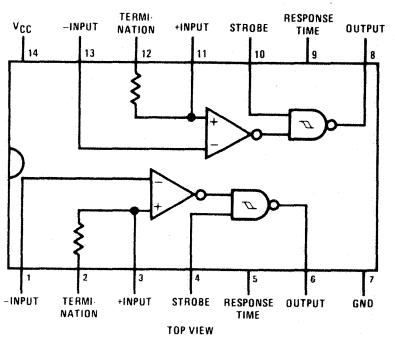
A response pin is provided for controlling sensitivity to input noise spikes with an external capacitor. Each receiver includes a 180Ω terminating resistor, which may be used optionally on twisted pair lines. The DS78C20 is specified over a −55°C to +125°C operating temperature range, and the DS88C20 over a 0°C to +70°C range.

features

- Full compatibility with EIA Standards RS-232-C, RS-422 and RS-423, and Federal Standards 1020 and 1030
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 1/2 V_{CC} strobe threshold for CMOS compatibility
- 5k input impedance
- 50 mV input hysteresis
- 200 mV input threshold
- Operation voltage range = 4.5V to 15V

connection diagram

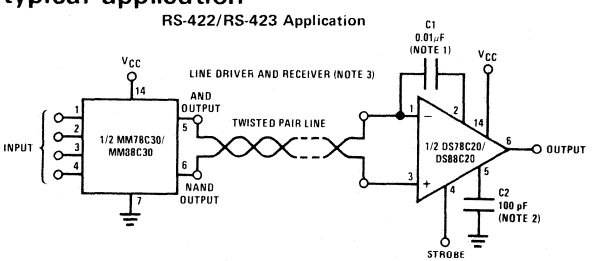
Dual-In-Line and Flat Package



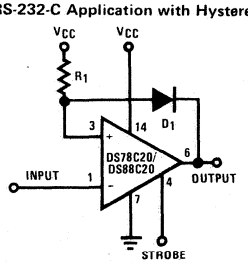
TOP VIEW

typical application

RS-422/RS-423 Application



RS-232-C Application with Hysteresis



Note 1: (Optional internal termination resistor).

a) Capacitor in series with internal line termination resistor; terminates the line and saves termination power. Exact value depends on line length.

b) Pin 1 connected to pin 2; terminates the line.

c) Pin 2 open; no internal line termination.

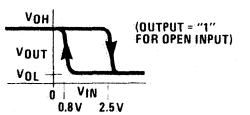
d) Transmission line may be terminated elsewhere or not at all.

Note 2: Optional to control response time.

Note 3: V_{CC} = 4.5V to 15V for the DS78C20. For further information on line drivers and line receivers, refer to application notes AN-22, AN-83 and AN-108.

For signals which require fail-safe or have slow rise and fall times, use R_1 and D_1 as shown above; otherwise the positive input (pin 3 or pin 11) may be connected to ground.

V_{CC}	$R_1 \pm 5\%$
5V	4.3kΩ
10V	15 kΩ
15V	24 kΩ



absolute maximum ratings (Note 1)

Supply Voltage	18V
Input Voltage	±25V
Strobe Voltage	18V
Output Sink Current	50 mA
Power Dissipation	600 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

operating conditions

	MIN	MAX	UNITS
Supply Voltage (V_{CC})	4.5	15	V
Temperature (T_A)			
DS78C20	−55	+125	°C
DS88C20	0	+70	°C
Common-Mode Voltage (V_{CM})	−15	+15	V
Differential Input Voltage (V_{DIFF})		≤6	V

electrical characteristics (Notes 2 and 3)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
V_{TH}	Differential Threshold Voltage	I_{OUT} = −200 μA, $V_{OUT} \geq V_{CC} - 1.2V$	−10V ≤ V_{CM} ≤ 10V		0.06	0.2	V
			−15V ≤ V_{CM} ≤ 15V		0.06	0.3	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq 0.5V$	−10V ≤ V_{CM} ≤ 10V		−0.08	−0.2	V
			−15V ≤ V_{CM} ≤ 15V		−0.08	−0.3	V
R_{IN}	Input Resistance	−15V ≤ V_{CM} ≤ 15V			5		kΩ
R_T	Line Termination Resistance	T_A = 25°C		100	180	300	Ω
I_{IND}	Data Input Current (Unterminated)	V_{CM} = 10V			2	3.1	mA
		V_{CM} = 0V			0	−0.5	mA
		V_{CM} = −10V			−2	−3.1	mA
V_{THB}	Input Balance	I_{OUT} = 200 μA, $V_{OUT} \geq V_{CC} - 1.2V$, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		0.1	0.4	V
		I_{OUT} = 1.6 mA, $V_{OUT} \leq 0.5V$, R_S = 500Ω, (Note 5)	−7V ≤ V_{CM} ≤ 7V		−0.1	−0.4	V
V_{OH}	Logical "1" Output Voltage	I_{OUT} = −200 μA, V_{DIFF} = 1V		V_{CC}−1.2	V_{CC}−0.75		V
V_{OL}	Logical "0" Output Voltage	I_{OUT} = 1.6 mA, V_{DIFF} = −1V			0.25	0.5	V
I_{CC}	Power Supply Current	15V ≤ V_{CM} ≤ −15V, V_{DIFF} = −0.5V (Both Receivers)	V_{CC} = 5.5V		8	15	mA
			V_{CC} = 15V		15	30	mA
$I_{IN(1)}$	Logical "1" Strobe Input Current	V_{STROBE} = 15V, V_{DIFF} = 3V			15	100	μA
$I_{IN(0)}$	Logical "0" Strobe Input Current	V_{STROBE} = 0V, V_{DIFF} = −3V			−0.5	−100	μA
V_{IH}	Logical "1" Strobe Input Voltage	I_{OUT} = 1.6 mA, $V_{OL} \leq 0.5V$	V_{CC} = 5V	3.5	2.5		V
			V_{CC} = 10V	8.0	5		V
			V_{CC} = 15V	12.5	7.5		V
V_{IL}	Logical "0" Strobe Input Voltage	I_{OUT} = −200 μA, $V_{OH} = V_{CC} - 1.2V$	V_{CC} = 5V		2.5	1.5	V
			V_{CC} = 10V		5.0	2.0	V
			V_{CC} = 15V		7.5	2.5	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0V, V_{CC} = 15V, V_{STROBE} = 0V, (Note 4)		−5	−20	−40	mA

switching characteristics V_{CC} = 5V, T_A = 25°C

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$t_{pd0(D)}$	Differential Input to "0" Output	C_L = 50 pF		60	100	ns
$t_{pd1(D)}$	Differential Input to "1" Output	C_L = 50 pF		100	150	ns
$t_{pd0(S)}$	Strobe Input to "0" Output	C_L = 50 pF		30	70	ns
$t_{pd1(S)}$	Strobe Input to "1" Output	C_L = 50 pF		100	150	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

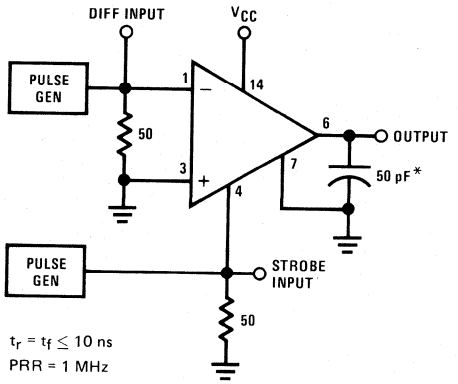
Note 2: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78C20 and across the 0°C to +70°C range for the DS88C20. All typical values are for T_A = 25°C, V_{CC} = 5V and V_{CM} = 0V.

Note 3: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

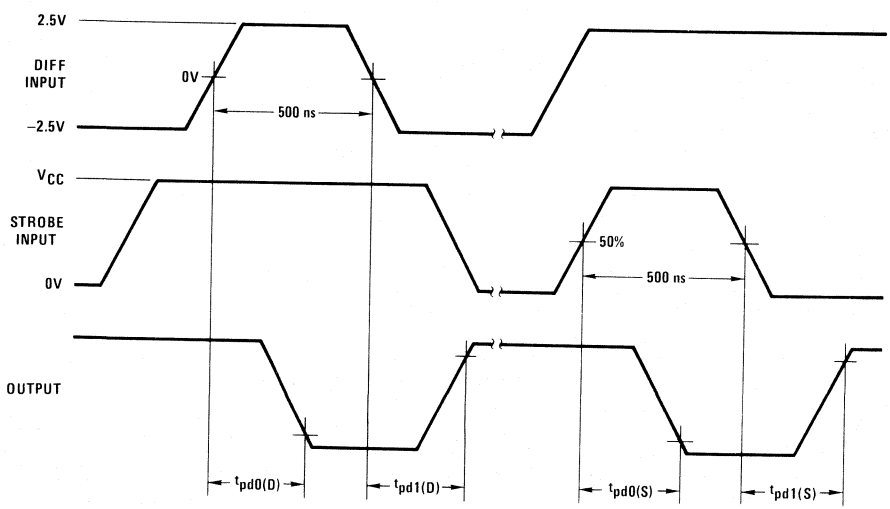
Note 4: Only one output at a time should be shorted.

Note 5: Refer to EIA-RS-422 for exact conditions.

ac test circuit and switching time waveforms



*Includes probe and jig capacitance



National Semiconductor

LM146/LM246/LM346 Programmable Quad Operational Amplifier

general description

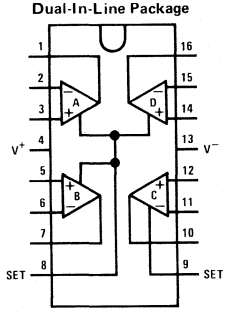
The LM146 series of quad op amps consist of four independent, high gain, internally compensated, low power, programmable amplifiers. Two external resistors (R_{SET}) allow the user to program the gain-bandwidth product, slew rate, supply current, input bias current, input offset current and input noise. For example, the user can trade-off supply current for bandwidth or optimize noise figure for a given source resistance. In a similar way, other amplifier characteristics can be tailored to the application. Except for the two programming pins at the end of the package, the LM146 pin-out is the same as the LM124 and LM148.

features (I_{SET} = 10 μA)

- Programmable electrical characteristics
- Battery-powered operation
- Low supply current — 350 μA per amplifier
- Gain-bandwidth product — 1 MHz
- Large dc voltage gain — 120 dB
- Low noise voltage — 25 nV/$\sqrt{\text{Hz}}$
- Wide power supply range — ±1.5V to ±22V
- Class AB output stage—no crossover distortion
- Ideal pin out for Biquad active filters
- Overload protection for inputs and outputs

connection diagram

Dual-In-Line Package



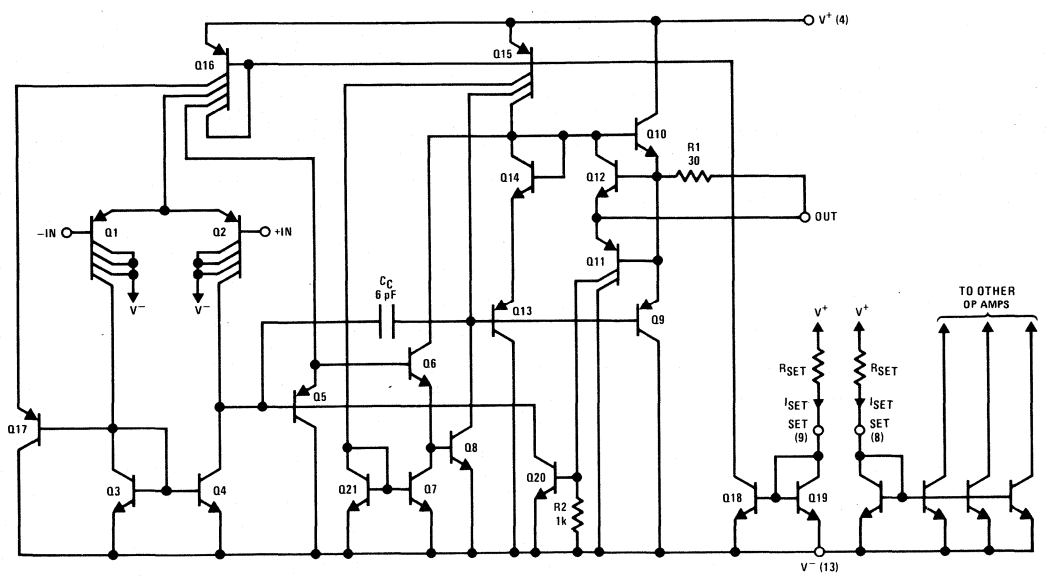
TOP VIEW

PROGRAMMING EQUATIONS

Total Supply Current = 1.4 mA (I_{SET}/10 μA)
Gain-Bandwidth Product = 1 MHz (I_{SET}/10 μA)
Slew Rate = 0.4V/μs (I_{SET}/10 μA)
Input Bias Current ≃ 50 nA (I_{SET}/10 μA)
I_{SET} = Current into pin 8, pin 9 (see schematic diagram)

$$I_{SET} = \frac{V^+ - V^- - 0.6V}{R_{SET}}$$

schematic diagram



absolute maximum ratings

	LM146	LM246	LM346
Supply Voltage	±22V	±18V	±18V
Differential Input Voltage (Note 1)	±30V	±30V	±30V
CM Input Voltage (Note 1)	±15V	±15V	±15V
Power Dissipation (Note 2)	900 mW	500 mW	500 mW
Output Short-Circuit Duration (Note 3)	Indefinite	Indefinite	Indefinite
Operating Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
Maximum Junction Temperature	150°C	110°C	100°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C
Thermal Resistance (θ_{jA}), (Note 2) P_D	900 mW	900 mW	900 mW
θ_{jA}	100°C/W	100°C/W	100°C/W

dc electrical characteristics (V_S = ±15V, T_A = 25°C, I_{SET} = 10 μA)

PARAMETER	CONDITIONS	LM146			LM246/LM346			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{CM} = 0V, $R_S \leq 50\ \Omega$		2	5		2	6	mV
Input Offset Current	V_{CM} = 0V		2	10		2	100	nA
Input Bias Current	V_{CM} = 0V		50	100		50	500	nA
Supply Current (4 Op Amps)			1.4	2.0		1.4	2.0	mA
Large Signal Voltage Gain	R_L = 10 kΩ, ΔV_{OUT} = ±10V	50	1000		25	1000		V/mV
Input CM Range		±13.5	±14		±13.5	±14		V
CM Rejection Ratio	$R_S \leq 50\ \Omega$	70	100		70	100		dB
Power Supply Rejection Ratio	$R_S \leq 50\ \Omega$	76	100		74	100		dB
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		±12	±14		V
Short-Circuit Current		10	20	30	10	20	30	mA
Gain-Bandwidth Product			1.0			1.0		MHz
Phase Margin	C_L = 100 pF		60			60		Deg
Slew Rate			0.4			0.4		V/μs
Input Noise Voltage	f = 1 kHz		25			25		$nV/\sqrt{Hz}$
Channel Separation	R_L = 10 kΩ, ΔV_{OUT} = 0V to ±14V		120			120		dB
Input Resistance			1.0			1.0		MΩ

Note 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 2: The maximum power dissipation for these devices must be derated at elevated temperatures and is dictated by T_{jMAX}, θ_{jA}, and the ambient temperature, T_A. The maximum available power dissipation at any temperature is $P_d = (T_{jMAX} - T_A)/\theta_{jA}$ or the 25°C P_{dMAX}, whichever is less.

Note 3: Any of the amplifier outputs can be shorted to ground indefinitely; however, more than one should not be simultaneously shorted as the maximum junction temperature will be exceeded.

National Semiconductor

LM195/LM295/LM395 Ultra Reliable Power Transistors

general description

The LM195/LM295/LM395 are fast, monolithic power transistors with complete overload protection. These devices, which act as high gain power transistors, have included on the chip, current limiting, power limiting, and thermal overload protection making them virtually impossible to destroy from any type of overload. In the standard TO-3 transistor power package, the LM195 will deliver load currents in excess of 1.0A and can switch 40V in 500 ns.

The inclusion of thermal limiting, a feature not easily available in discrete designs, provides virtually absolute protection against overload. Excessive power dissipation or inadequate heat sinking causes the thermal limiting circuitry to turn off the device preventing excessive heating.

features

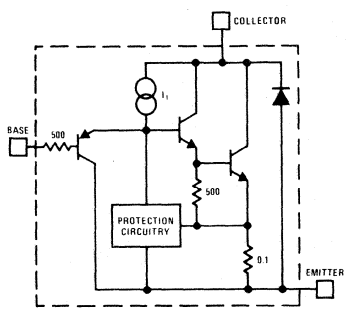
- Internal thermal limiting
- Greater than 1.0A output current
- 3.0μA typical base current
- 500 ns switching time
- 2.0V saturation
- Base can be driven up to 40V without damage
- Directly interfaces with CMOS or TTL

The LM195 offers a significant increase in reliability as well as simplifying power circuitry. In some applications, where protection is unusually difficult, such as switching regulators, lamp or solenoid drivers where normal power dissipation is low, the LM195 is especially advantageous.

The LM195 is easy to use and only a few precautions need be observed. Excessive collector to emitter voltage can destroy the LM195 as with any power transistor. When the device is used as an emitter follower with low source impedance, it is necessary to insert a 5.0k resistor in series with the base lead to prevent possible emitter follower oscillations. Although the device is usually stable as an emitter follower, the resistor eliminates the possibility of trouble without degrading performance. Finally, since it has good high frequency response, supply by passing is recommended.

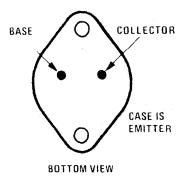
The LM195/LM295/LM395 are available in standard TO-3 power packages and solid Kovar TO-5. The LM195 is rated for operation from −55°C to +150°C, the LM295 from −25°C to +150°C and the LM395 from 0°C to +125°C.

simplified circuit and connection diagrams

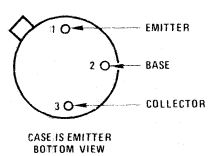


Simplified Circuit of the LM195

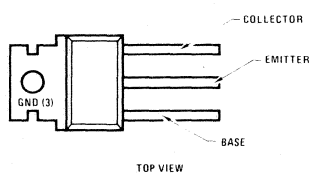
TO-3 Metal Can Package



TO-5 Metal Can Package



TO-220 Power Package



absolute maximum ratings

Collector to Emitter Voltage	
LM195, LM295	42V
LM395	36V
Collector to Base Voltage	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Forward)	
LM195, LM295	42V
LM395	36V
Base to Emitter Voltage (Reverse)	20V
Collector Current	Internally Limited
Power Dissipation	Internally Limited
Operating Temperature Range	
LM195	−55°C to +150°C
LM295	−25°C to +150°C
LM395	0°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics (Note 1)

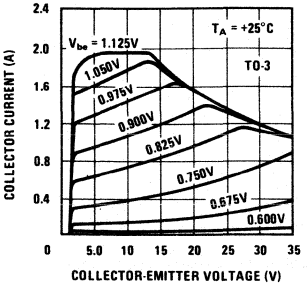
PARAMETER	CONDITIONS	LM195, LM295			LM395			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Collector-Emitter Operating Voltage	$I_Q \leq I_C \leq I_{MAX}$			42			36	V
Base to Emitter Breakdown Voltage	$0 < V_{CE} \leq V_{CEMAX}$	42			36	60		V
Collector Current								
TO-3	$V_{CE} \leq 15V$	1.2	2.0		1.0	2.0		A
TO-5	$V_{CE} \leq 7.0V$	1.2	2.0		1.0	2.0		A
TO-220	$V_{CE} \leq 15V$				1.0	2.0		A
Saturation Voltage	$I_C \leq 1.0A$		1.8	2.0		1.8	2.2	V
Base Current	$0 \leq I_C \leq I_{MAX}$ $0 \leq V_{CE} \leq V_{CEMAX}$		3.0	5.0		3.0	10	μA
Quiescent Current	$V_{be} = 0$ $0 \leq V_{CE} \leq V_{CEMAX}$		2.0	5.0		2.0	10	mA
Base to Emitter Voltage	$I_C = 1.0A$, $T_A = +25°C$		0.9			0.9		V
Switching Time	$V_{CE} = 36V$, $R_L = 36\Omega$, $T_A = +25°C$		500			500		ns
Thermal Resistance Junction to Case (Note 2)	TO-3 Package		2.3	3.0		2.3	3.0	°C/W
	TO-5 Package		12	15		12	15	°C/W

Note 1: Unless otherwise specified, these specifications apply for $-55°C \leq T_j \leq +150°C$ for the LM195, $-25°C \leq T_j \leq +150°C$ for the LM295 and $0°C \leq +125°C$ for the LM395.

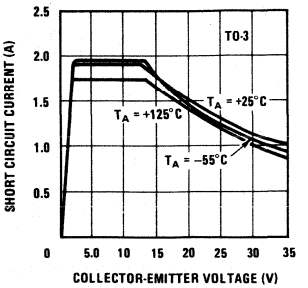
Note 2: Without a heat sink, the thermal resistance of the TO-5 package is about +150°C/W, while that of the TO-3 package is +35°C/W.

typical performance characteristics

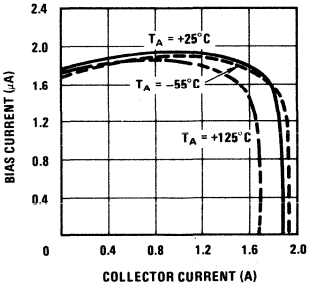
Collector Characteristics



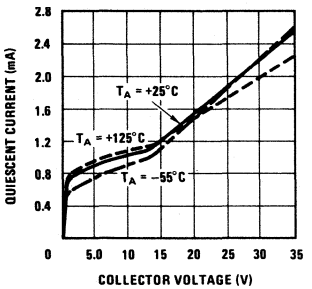
Short Circuit Current



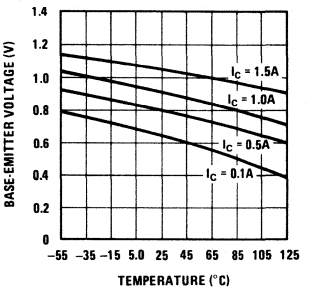
Bias Current



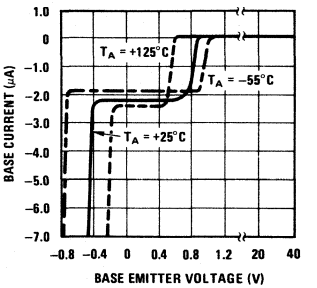
Quiescent Current



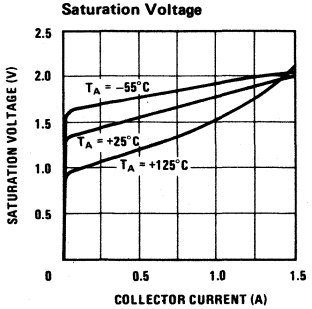
Base Emitter Voltage



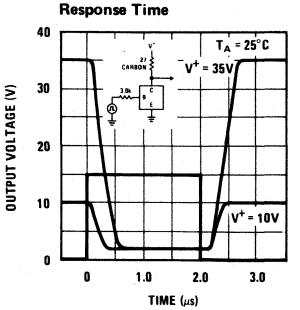
Base Current



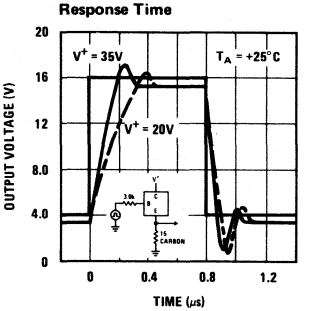
Saturation Voltage



Response Time

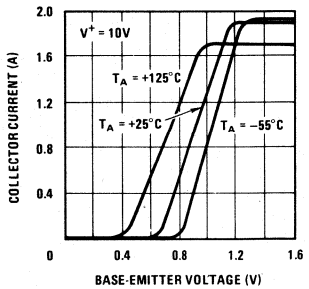


Response Time

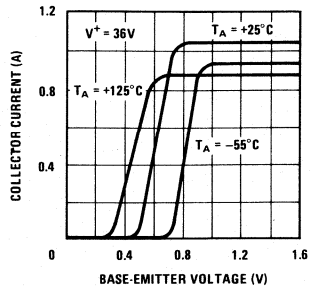


typical performance characteristics (con't)

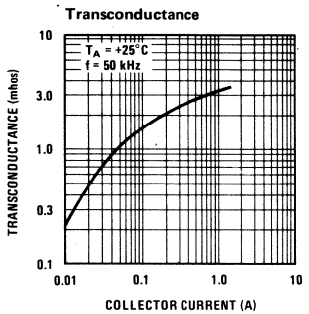
10V Transfer Function



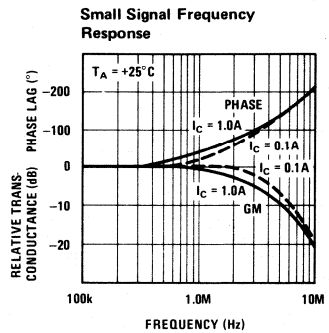
36V Transfer Function



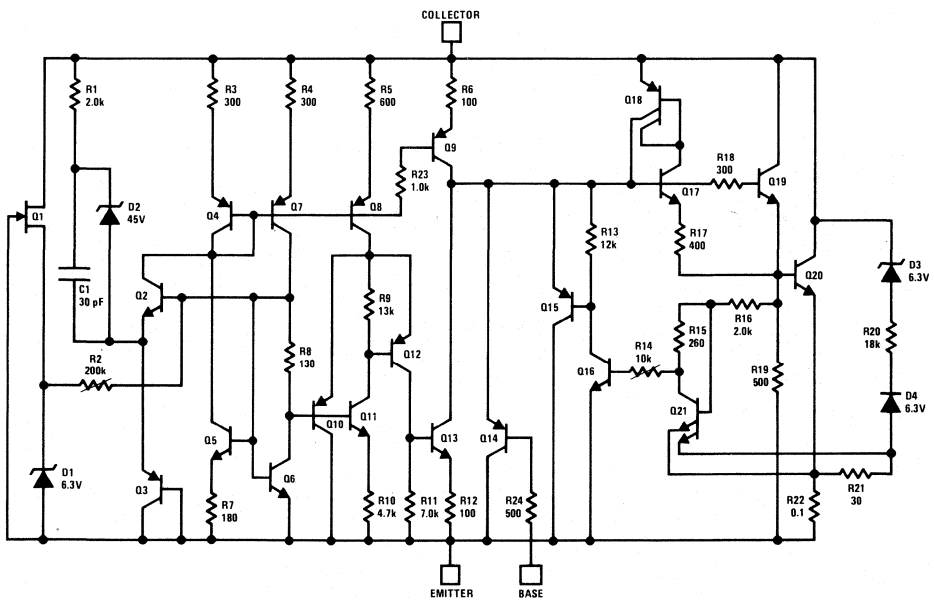
Transconductance



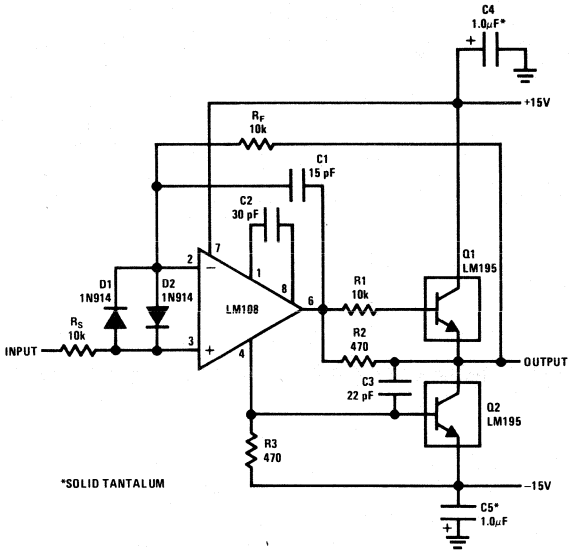
Small Signal Frequency Response



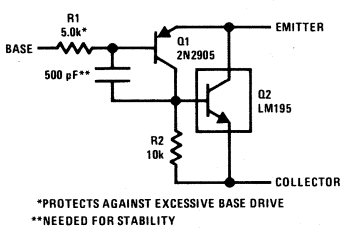
schematic diagram



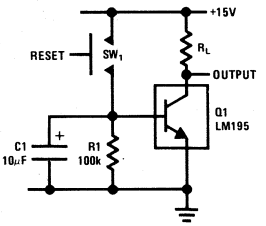
typical applications



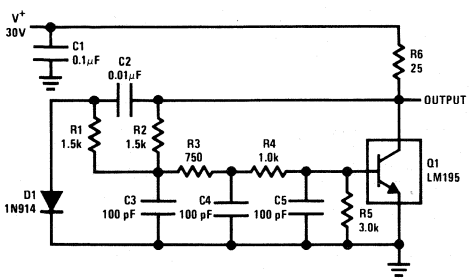
1.0 Amp Voltage Follower



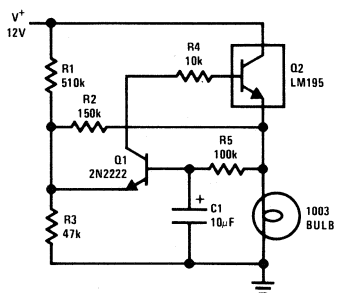
Power PNP



Time Delay

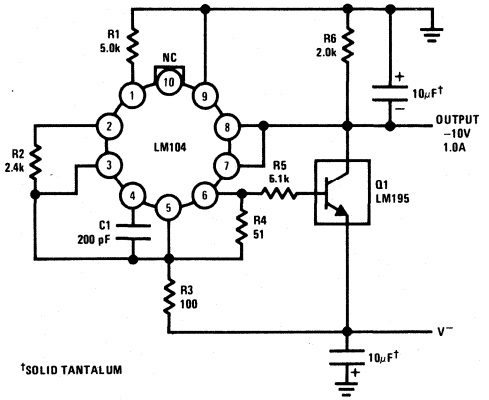


1.0 MHz Oscillator

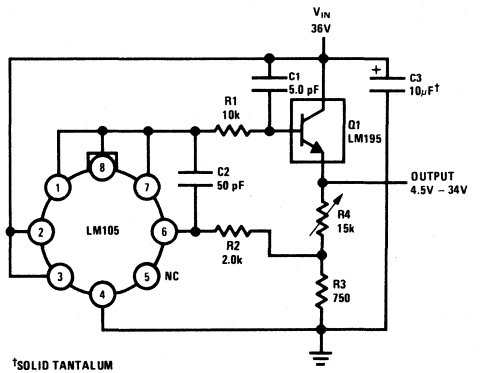


1.0 Amp Lamp Flasher

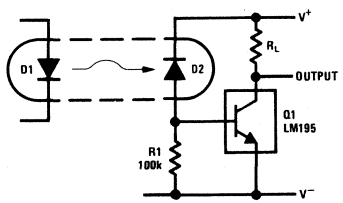
typical applications (con't)



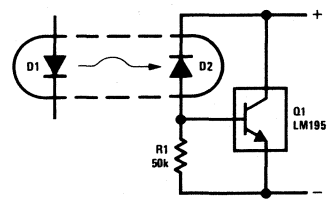
1.0 Amp Negative Regulator



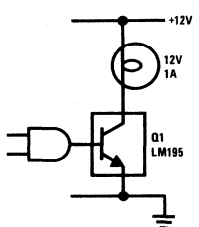
1.0 Amp Positive Voltage Regulator



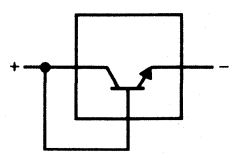
Fast Optically Isolated Switch



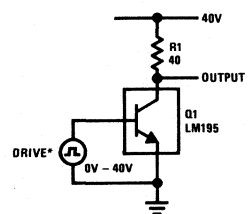
Optically Isolated Power Transistor



CMOS or TTL Lamp Interface



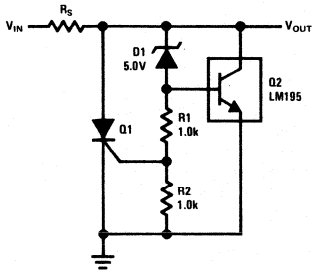
Two Terminal Current Limiter



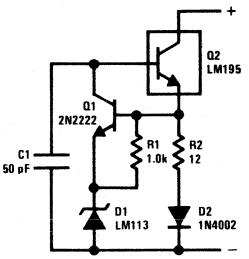
*DRIVE VOLTAGE 0V TO ≥ 1.0V ≤ 42V

40V Switch

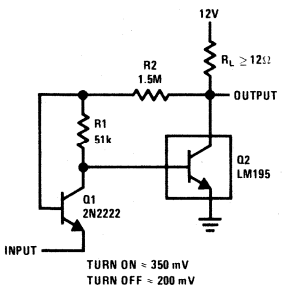
typical applications (con't)



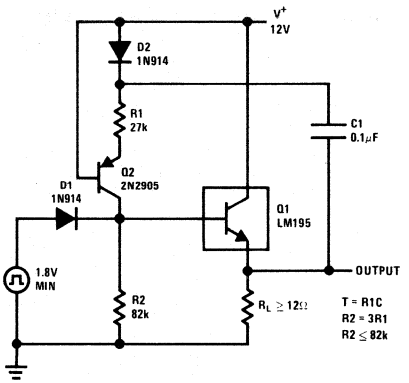
6.0V Shunt Regulator with Crowbar



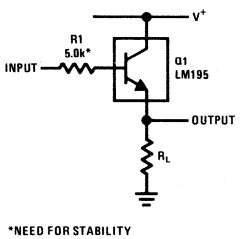
Two Terminal 100 mA Current Regulator



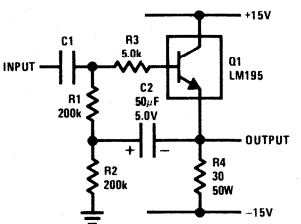
Low Level Power Switch



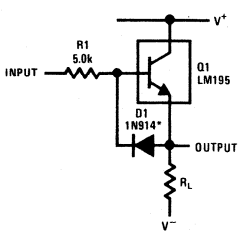
Power One-Shot



Emitter Follower

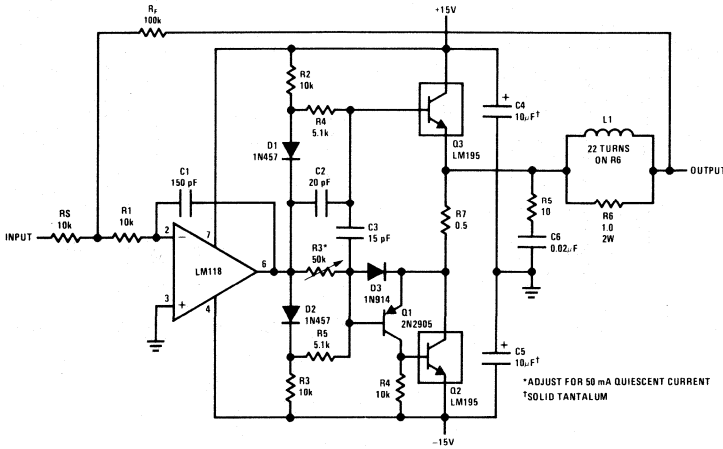


High Input Impedance AC Emitter Follower

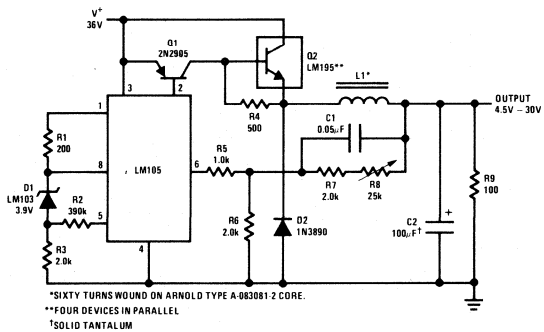


Fast Follower

typical applications (con't)



Power Op Amp



6.0 Amp Variable Output Switching Regulator

Consumer Products

National Semiconductor

MM5369 17-Stage Programmable Oscillator/Divider

general description

The MM5369 is a CMOS integrated circuit with 17 binary divider stages that can be used to generate a precise 60 Hz reference from commonly available high frequency quartz crystals. An internal pulse is generated by mask programming the combinations of stages 1 through 4, 16 and 17 to set or reset the individual stages. The programmable number the circuit will divide by can vary from 10000 to 98000. The MM5369 is advanced one count on the positive transition of each clock pulse. Two buffered outputs are available: the crystal frequency for tuning purposes and the 17th stage 60 Hz output. Mask options are available for use with commonly available, low cost, high frequency crystals. Therefore, this design can be "customized" by special order to design specific programmable divider limits whereby the maximum divide-by can be 98,000 and the minimum divide-by can be 10,000. The MM5369 is available in an 8-lead dual-in-line epoxy package.

features

- Crystal Oscillator
- Two buffered outputs
  - Output 1 cyrstal frequency
  - Output 2 full division
- High speed (4 MHz at V_{DD} = 10)
- Wide supply range 3–15V
- Low Power
- Fully static operation
- 8 lead dual-in-line package
- Low current

Standard MM5369N Only

- 3.58 MHz (color TV oscillator) input frequency
- 60 Hz output frequency

connection diagram

Dual-In-Line Package

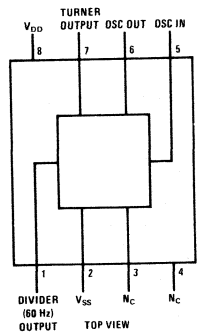


FIGURE 1.

Order Number MM5369N
See Package 17

block diagram

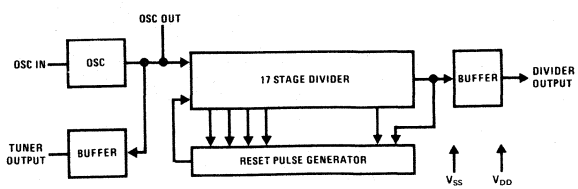


FIGURE 2.

absolute maximum ratings

Voltage at Any Pin	$-0.3V$ to V_{CC} $+0.3V$
Operating Temperature	$0^{\circ}C$ to $+70^{\circ}C$
Storage Temperature	$-65^{\circ}C$ to $+150^{\circ}C$
Package Dissipation	500 mW
Maximum V_{CC} Voltage	16V
Operating V_{CC} Range	3V to 15V
Lead Temperature (Soldering, 10 seconds)	$300^{\circ}C$

electrical characteristics

T_A within operating temperature range, V_{SS} = GND, $3V \leq V_{DD} \leq 15V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current Drain	V_{DD} = 15V			10	μA
Operating Current Drain	V_{DD} = 10V, f_{IN} = 4.19 MHz		1.2	2.5	mA
Frequency of Oscillation	V_{DD} = 10V	DC		4.5	MHz
	V_{DD} = 6V	DC		2	MHz
Output Current Levels	V_{DD} = 10V				
	V_{OUT} = 5V				
Logical "1" Source		500			μA
Logical "0" Sink		500			μA
Output Voltage Levels	V_{DD} = 10V				
	I_O = 10 μA				
Logical "1"		9.0			V
Logical "0"				1.0	V

functional description

A connection diagram for the MM5369 is shown in *Figure 1* and a block diagram is shown in *Figure 2*.

TIME BASE

A precision time base is provided by the interconnection of a 3,579,545 Hz quartz crystal and the RC network shown in *Figure 3* together with the CMOS inverter/amplifier provided between the OSC IN and the OSC OUT terminals. Resistor R1 is necessary to bias the inverter for class A amplifier operation. Capacitors C1 and C2 in series provide the parallel load capacitance required for precise tuning of the quartz crystal.

The network shown provides > 100 ppm tuning range when used with standard crystals trimmed for C_L = 12 pF. Tuning to better than ±2 ppm is easily obtainable.

DIVIDER

A pulse is generated when divider stages 1 through 4, 16 and 17 are in the correct state. By mask options, this pulse is used to set or reset individual stages of the counter, thus varying the modulus of the counter from 10000 to 98000. *Figure 4* shows the relationship between the duty cycle and the programmed modulus.

OUTPUTS

The Tuner Output is a buffered output at the crystal oscillator frequency. This output is provided so that the crystal frequency can be obtained without disturbing the crystal oscillator. The Divide Output is the input frequency divided by the mask programmed number. Both outputs are push-pull outputs. A typical application of the MM5369 is shown in *Figure 5*.

functional description (cont.)

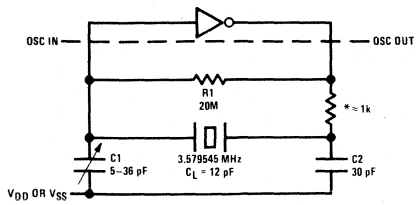


FIGURE 3. Crystal Oscillator Network

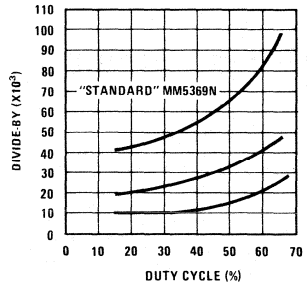


FIGURE 4. Plot of Divide-By Vs Duty Cycle

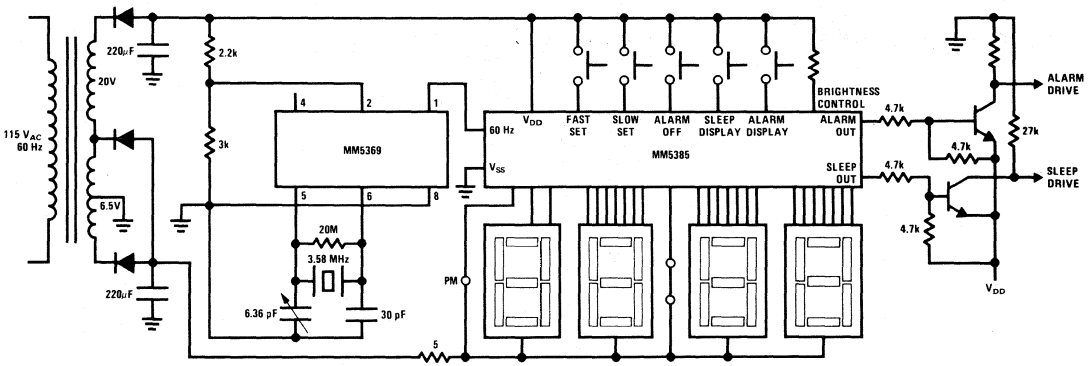


FIGURE 5. Clock Radio Circuit with Battery Back-Up

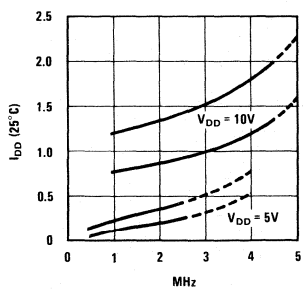


FIGURE 6. Typical Current Drain Vs Oscillator Frequency

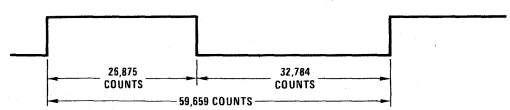


FIGURE 7. Output Waveform for Standard MM5369

*To be selected based on xtal used

National Semiconductor

MM5393 Push Button Telephone Dialer

general description

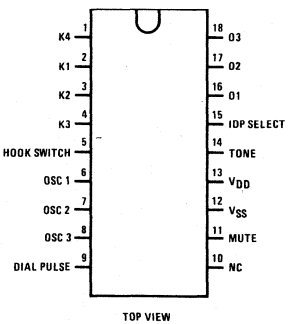
The MM5393 is a monolithic metal gate CMOS integrated circuit which provides all logic required to convert a push button input to a series of pulses suitable for simulating a telephone dial. Storage is provided for 21 digits, therefore, the information is retained after the call is completed and the number is available for redial. Entering a new number simply overrides the previous one. An interdigital pause can be externally selected as either 415 ms or 830 ms. A muting output is supplied to mute receiver noise during outpulsing, and a 600 Hz tone is activated every time a key is depressed.

features

- 21-digit storage
- Selectable interdigital pause
- Redial of last number
- 600 Hz tone
- Line powered operation

connection diagram

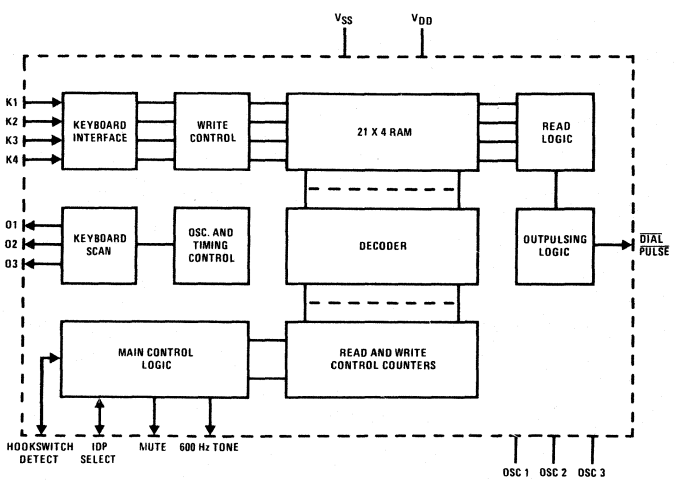
Dual-In-Line Package



TOP VIEW

Order Number MM5393N
See Package 20

block diagram



absolute maximum ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	−30°C to +65°C
Storage Temperature Range	−40°C to +70°C
$V_{DD} - V_{SS}$	6V max
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature range, V_{SS} − Gnd, $2V \leq V_{DD} \leq 5.5V$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Levels					
Logical "1"		V_{DD}−0.25		V_{DD}	V
Logical "0"		V_{SS}		V_{SS}+0.25	V
Output Current Levels					
Dial Pulse					
Logical "1"	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.5	150			μA
Logical "0"	V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5	150			μA
Mute					
Logical "1"	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.5	100			μA
Logical "0"	V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5	100			μA
Tone					
Logical "1"	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.5	10			μA
Logical "0"	V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5	10			μA
01, 02, 03					
Logical "1"	V_{DD} = 3V, V_{OUT} = V_{DD} − 0.5	20			μA
Logical "0"	V_{DD} = 3V, V_{OUT} = V_{SS} + 0.5	150			μA

functional description

The time base for the MM5393 is an RC controlled oscillator nominally tuned to 20 kHz. This is successively divided to provide timing signals for the various counters. The keyboard inputs, K1–K4, in conjunction with the scan counter outputs, 01–03, indicate the presence of a particular key depression. If only one key is detected for 5 ms, the decoded key will be loaded into the RAM. The push button inputs are accepted at an asynchronous rate, loaded into a first-in-first-out memory, and outpulsing of the correct number of pulses begins immediately after the first digit is entered. After the first digit has been completed, outpulsing will cease unless another key has been entered. This allows use in a PBX system to ensure receipt of a dial tone before entering the remainder of the number. If the call was not successful, it can be redialed at a later time by pressing the redial key (#). If an access code is required as in a PBX system, it can be entered, the dial tone can be established, then the redial key can be pushed. Only one key can be entered before pushing the redial key because after the second key entry, the memory is erased. A block diagram of the MM5393 is shown in *Figure 1*.

KEYPAD DATA INPUTS

Keypad closures cause the connection of 2 of 7 switch contacts arranged as a matrix (shown in *Figure 2*). Key closures are protected from contact bounce for 5 ms.

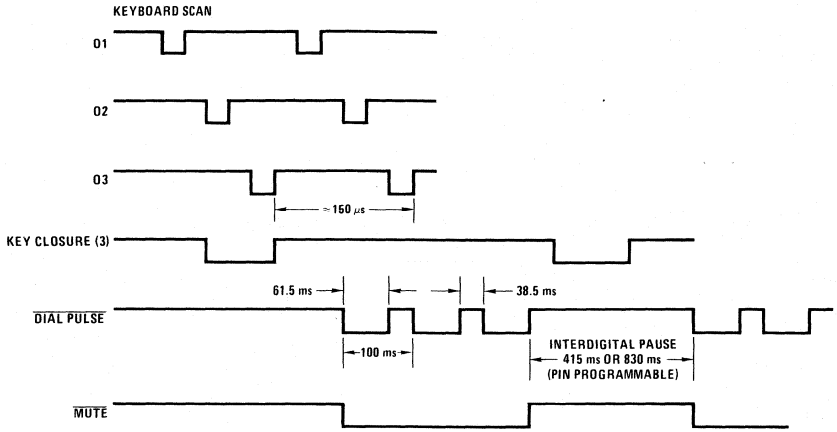
IMPULSING MARK-TO-SPACE RATIO

The mark-to-space ratio is 1.6:1 (61.5% to 38.5%).

IMPULSING OUTPUT

The number of pulses will correspond to the input digit. For example, key 5 will generate 5 pulses. The outpulsing rate is 10 Hz, and it can be varied by adjusting the frequency of the oscillator. Because it is intended to drive a transistor buffer, the outpulsing data is inverted. Digits are separated by an interdigital pause which is pin programmable for either 415 ms or 830 ms.

switching time waveforms



Note. All times are based on a 20 kHz oscillator.

FIGURE 1

keypad matrix

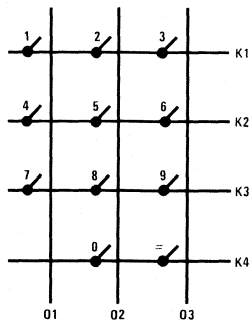


FIGURE 2

typical application

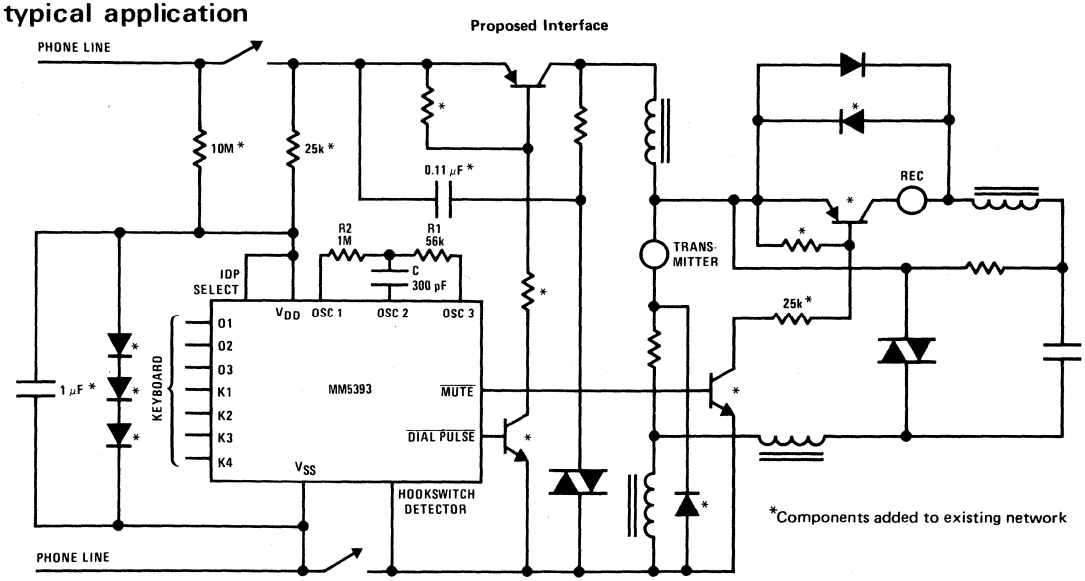


FIGURE 3

National Semiconductor

MM5395 TOUCH TONE® Generator

general description

The MM5395 is an integrated circuit that can provide all tone frequency pairs required for the TOUCH TONE® telephone dialing system. The output frequencies are generated by programmably dividing the frequency of the on-chip crystal-controlled oscillator; thus, accurate output frequencies can be obtained without tuning. The only external component needed for the oscillator is an inexpensive 3.579545 MHz crystal.

The device has four row and four column inputs. Inputs to the device can either be in a 2-out-of-8 code format from a keyboard, or by BCD signals to the row inputs.

The device is fabricated using our low voltage CMOS process so that it may be powered directly from the telephone line.

The MM5395 is designed to be used in a wide variety of tone signaling and data transmission applications.

features

- 3V to 5V supply
- On-chip 3.579545 MHz crystal-controlled oscillator
- Interface with standard telephone keypad
- Interface with single contact low-cost keypad option
- Multi-key lockout with single tone capability
- On-chip high band and low band tone generators and mixer
- High band pre-emphasis
- Low harmonic distortion
- Accurate tone frequencies
- Open emitter, emitter follower output
- Mute switch output
- Can be powered directly from the telephone line

functional description

The functional block diagram of MM5395 is shown in *Figure 1*. The device can be operated in Keypad Interface Mode or Signal Interface Mode (BCD into row input) depending on the logical level at "Control" input. In either mode, the MM5395 will digitally synthesize the high and/or low band sine waves when valid signals are applied to row or column inputs. The sum of the two sine waves is then provided at the "Tone Output." The base of the output NPN transistor is brought out ("FILTER") for easy filtering. Operational functional features are summarized in tables.

block diagram

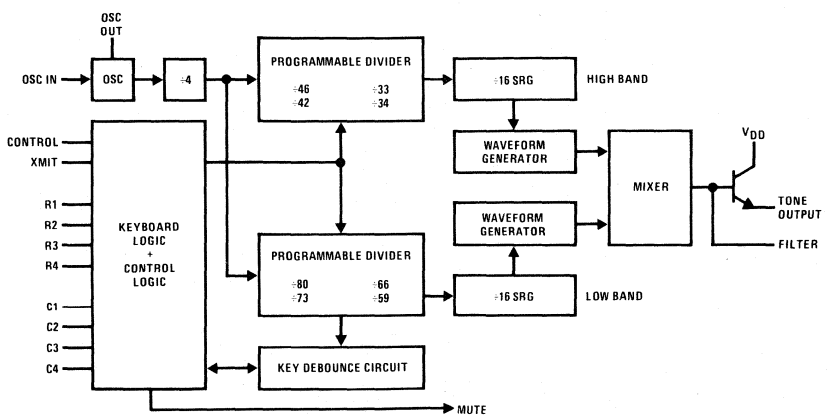


FIGURE 1

absolute maximum ratings

Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature Range	−40°C to +70°C
Storage Temperature Range	−65°C to +150°C
$V_{DD} - V_{SS}$	6V
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

T_A within operating temperature, $3V \leq V_{DD} - V_{SS} \leq 5V$, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pull-Up Resistor @ Column Inputs	$V_{IN} = V_{SS}$	100		400	kΩ
Input Pull-Down Resistor @ "Xmit"	$V_{IN} = V_{DD}$	100		400	kΩ
Internal Resistor @ Row Inputs					
To V_{DD} (Option A)	$V_{IN} = V_{SS}$	100		400	kΩ
To V_{SS} (Option B)	$V_{IN} = V_{DD}$	100		400	kΩ
Input Voltage Levels					
Logical "1"		V_{DD}−0.25		V_{DD}	V
Logical "0"		V_{SS}		V_{SS}+0.25	V
Output Voltage Swings @ "TONE OUTPUT"	$V_{DD} - V_{SS} = 3.0V$, $R_L > 500\Omega$				
Low Band Only			820		mVp-p
High Band Only			1000		mVp-p
Harmonic Distortion	$R_L \geq 500\Omega$, No External Filtering			−20	dB
Tone Frequency Deviation				1.0	%
Operating Frequency			3.579545		MHz
Key-Down Debounce Time			7	11.35	ms
Key-Up Debounce Time			4	7.15	ms
Power Dissipation	$V_{DD} - V_{SS} = 6V$, $R_L = 500\Omega$			30	mW
Output Current Level @ "MUTE"	$V_{DD} - V_{SS} = 3.0V$				
Logical "1"	$V_{OUT} = V_{DD} - 0.2V$	20			μA
Logical "0"	$V_{OUT} = V_{SS} + 0.5V$	2.0			mA

functional description (Continued)

TABLE I. Interface Mode Control

CONTROL	XMIT	INTERFACE MODE
0	Open	Keypad
1	0	Idle } BCD Signal
1	1	Send tones } e.g. MM5393

functional description (Continued)

TABLE II. Keypad Interface

(a). Functional Truth Table

ROW	COLUMN	LOW BAND	HIGH BAND
None	None	DC	DC
One	One	f_L	f_H
None	One	DC	f_H
One	None	f_L	DC
Two or more	None	DC	DC
Two or more	One	DC	f_H
None	Two or more	DC	DC
One	Two or more	f_L	DC

(b). Output Frequencies

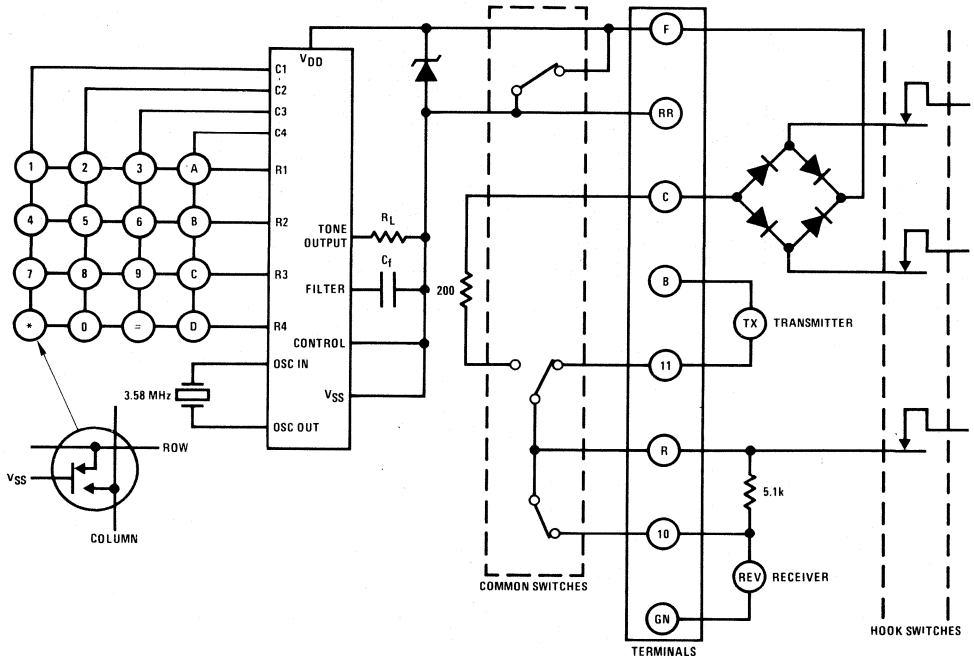
INPUTS	DESIRED FREQUENCIES		ACTUAL FREQUENCY	PERCENT DEVIATION
	f_L (Hz)	f_H (Hz)	(Hz)	
R1	697	–	699.1	0.306
R2	770	–	766.2	−0.497
R3	852	–	847.4	−0.536
R4	941	–	948.0	0.741
C1	–	1209	1215.9	0.569
C2	–	1336	1331.7	−0.324
C3	–	1477	1471.9	−0.35
C4	–	1633	1645.0	0.736

TABLE III. Functional Truth Table for Signal Interface

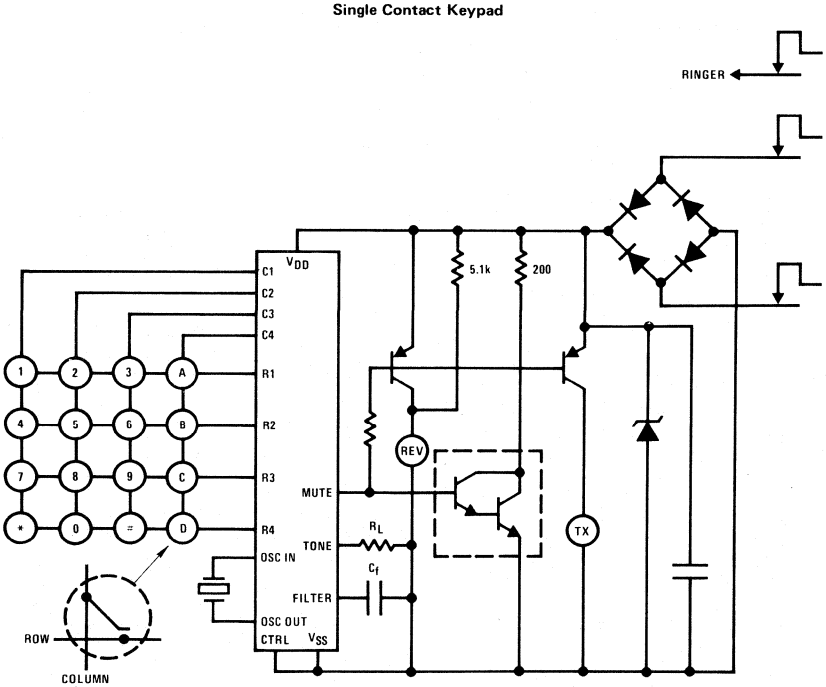
XMIT	C1	C2	R1	R2	R3	R4	FREQUENCIES GENERATED	
							f_L (Hz)	f_H (Hz)
0	X	X	X	X	X	X	DC	DC
1	Open	Open	0	0	0	0	941	1336
1	Open	Open	0	0	0	1	697	1209
1	Open	Open	0	0	1	0	697	1336
1	Open	Open	0	0	1	1	697	1477
1	Open	Open	0	1	0	0	770	1209
1	Open	Open	0	1	0	1	770	1336
1	Open	Open	0	1	1	0	770	1477
1	Open	Open	0	1	1	1	852	1209
1	Open	Open	1	0	0	0	852	1336
1	Open	Open	1	0	0	1	852	1477
1	0	Open	Valid BCD Inputs				f_L	DC
1	Open	0					DC	f_H
1	0	0					DC	DC

typical applications

Standard Telephone Keypad

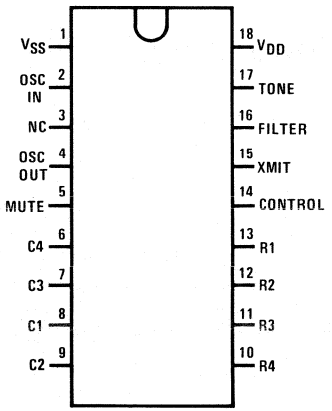


Single Contact Keypad



connection diagram

Dual-In-Line Package



TOP VIEW

Order Number MM5395N
See Package 20

National Semiconductor

MM53100, MM53105 Programmable TV Timers

general description

The MM53100 and MM53105 programmable TV timers are monolithic CMOS integrated circuits utilizing P and N-channel low threshold enhancement devices. These circuits contain all the logic to give a 4 or 6-digit, 24-hour display from a 50 or 60 Hz input, and control the "ON" time of the TV. The duration of the viewing period is 5, 10, 20 or 30 mins, selected by 2 input pins. Manual "ON" and "OFF" inputs are also provided. The MM53100 and MM53105 have ultra-low power dissipation in the stand-by mode and are ideally suited to crystal controlled battery-operated systems. The MM53100 is designed for an optimum interface in TVs with a positive common reference voltage (e.g., +18V). The MM53105 is designed for an optimum interface for TVs with a 0V reference voltage. Both are packaged in a 24-lead dual-in-line epoxy package.

features

- 50 or 60 Hz operation
- 24-hour display format
- Programmable TV on time
- Selectable view time
- Ultra-low power dissipation
- All counters resettable
- Low voltage operation
- Elimination of illegal time display at turn-on
- Daily repeat or non-repeating operating
- Fool-proof safety features
- Compatible with MM5840 or MM5841 display circuits

applications

- TV time display
- Remote TV "ON"/"OFF" switch
- Computer clock
- Time data–logging systems

block diagram

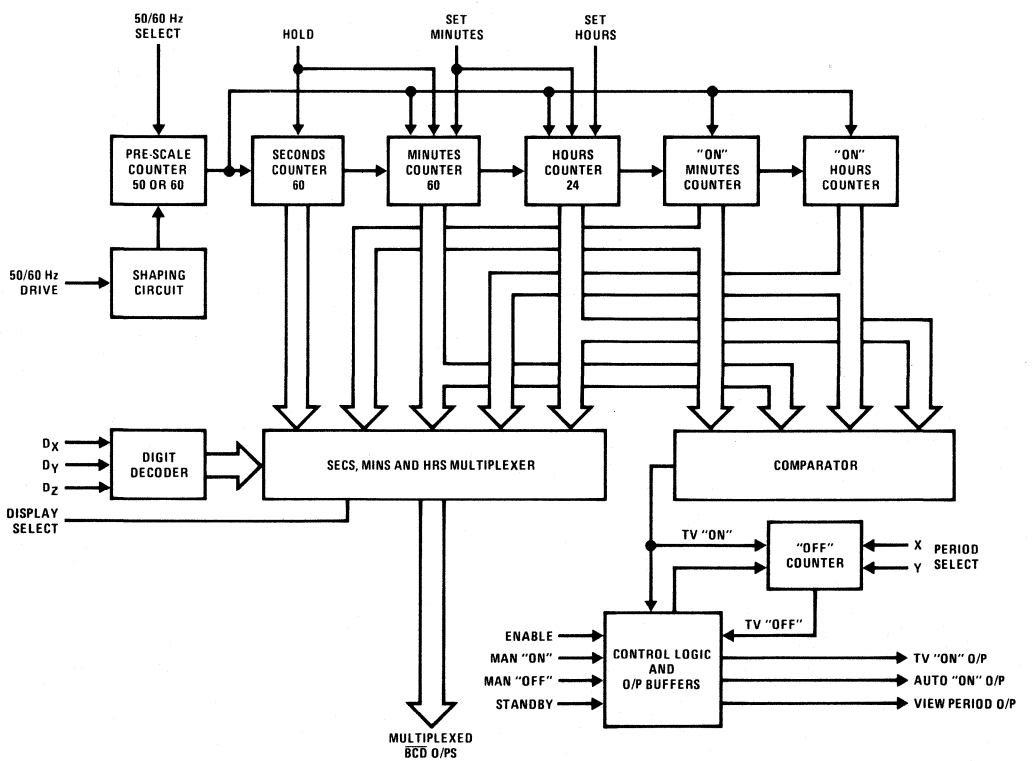


FIGURE 1. MM53100, MM53105 Block Diagram

absolute maximum ratings (MM53100) (V_{DD} common voltage reference)

Supply Voltage ($V_{DD} - V_{SS}$)	6V
Voltage at 50/60 Hz Select and Period Select Inputs	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Current Into or Out of Any Other Input	100 μA max

electrical characteristics (MM53100) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.8		5.0	V
Supply Current	$V_{DD} = 4.5V$		10	25	μA
Input Logic Levels					
50/60 Hz Input, Digit Select Inputs, Display Select, "ON", "OFF", Time Setting Control, Standby Control					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"	(Note 1)			$V_{SS}+0.5$	V
50/60 Hz Select, Period Select (X, Y)					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
Display Select Input Delay		0.5		2.0	μs
Output Logic Levels					
BCD Outputs	External Resistor, 15 kΩ to $V_{DD} - 12V$, $C_L = 15$ pF				
Logic "1"		$V_{DD}-0.8$			V
Logic "0"				$V_{DD}-11.2$	V

Note 1: If input voltages go more negative than V_{SS}, the input current must be limited to a maximum of 100 μA by the use of external series resistors. No resistors are required on the D_X, D_Y, D_Z inputs when interfacing with the MM5840.

absolute maximum ratings (MM53105) (V_{SS} common voltage reference)

Supply Voltage ($V_{DD} - V_{SS}$)	6V
Voltage at 50/60 Hz Select and Period Select Inputs	$V_{SS} + 6V$
Voltage at Any Other Pin	$V_{SS} + 13V$

electrical characteristics (MM53105) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage		2.8		5.0	V
Supply Current	$V_{DD} = 4.5V$		10	25	μA
Input Logic Levels					
50/60 Hz Input, Digit Select Inputs, "ON", "OFF", Display Select, Time Setting Controls, Standby Control					
Logic "1"		$V_{DD}-0.5$		13	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
50/60 Hz Select, Period Select (X, Y)					
Logic "1"		$V_{DD}-0.5$		V_{DD}	V
Logic "0"		V_{SS}		$V_{SS}+0.5$	V
Display Select Input Delay		0.5		2.0	μs

electrical characteristics (Continued) (MM53105) $T_A = 25°C$, $V_{DD} = 4.5V$, $V_{SS} = 0V$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Logic Levels					
BCD Outputs	External Resistor 15 kΩ to 12V, C_L = 15 pF				
Logic "1"		11.2			V
Logic "0"				0.8	V
TV "ON" Output, Auto "ON" Output, View Period Output					
Logic "1"	Loaded 2.7 kΩ to V_{SS}	0.5			mA
Logic "0"	Loaded 2.7 kΩ to V_{DD}	1.0			mA

Note 1: Input voltages to go more positive than V_{DD}.

functional description

A block diagram of the MM53100, MM53105 TV timers is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1*. *Figures 5a and 5b* illustrate the system configuration for a crystal controlled TV display system using both circuits.

Dual-In-Line Package, Top View

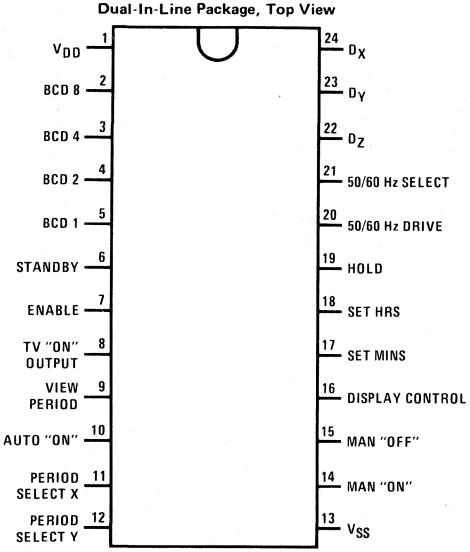


FIGURE 2.

Order Number MM53100N or MM53105N
See Package 22

50 or 60 Hz Drive: This input is applied to a Schmitt trigger shaping circuit which allows use of a filtered sinewave input. A simple RC filter should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the time-keeping function.

Alternatively, in a crystal controlled battery operated system, an oscillator and prescaler such as the MM53107 could be used as a time base.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 pps time base. The counter is programmed for 60 Hz operation by connecting this input to V_{DD}. An internal 1 MΩ pull-down resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Inputs to set hours and set minutes as well as hold input, are provided. Internal 1 MΩ pull-down resistors provide the normal timekeeping function. Switching any 1 of these inputs (1 at a time) to "1" results in the desired time setting function. Set Hours advances hours information at 1 hour/second and Set Minutes advances minutes information at 1 minute/second, without roll over into the hours counter. Set Minutes also resets the seconds counter to 0. The hold input stops the clock to the minutes counter and resets the seconds counter. Activating Set Minutes and Set Hours simultaneously resets the displayed counters to all 0's.

Display: This input controls the display and time-setting operation. It has an internal 1 MΩ pull-down resistor to V_{SS}. When taken to Logic "0" or in open circuit condition, the real time is displayed and the Set Hours and Set Minutes inputs operate the real time counters. When taken to logic "1", the "ON" time is displayed and the time-setting inputs operate on the "ON" counters.

Digital Select Inputs (D_X, D_Y, D_Z): These 3 inputs are used to determine which digit will be displayed. Table IA shows the code for each digit. Seconds will be displayed as "00" when the "ON" time is being displayed.

Enable: This input has an internal resistor to V_{SS}. When taken to logic "1", this input disables the programmed "ON" time for the TV output.

Period Select Inputs (X, Y): These inputs have pull-down resistors to V_{SS}. They determine the view period, i.e., 5, 10, 20 or 30 mins. Table IB shows the Period Select Code.

functional description (Continued)

Standby Control Input: This input has an internal resistor to V_{SS}. Its function is to sense when the line generated 12V supply is turned off and to then disable the outputs. In the TV, this input should be connected to the 12V supply.

Manual "ON" Input: This input has an internal resistor to V_{SS}. When taken to logic "1", this input turns the TV output to the "0" state. It is designed to have typically 0.75 second debounce time to prevent maloperation.

Manual "OFF" Input: This input has an internal resistor to V_{SS}. When taken to logic "1", this input turns the TV output to the "1" state. It is designed to have typically 0.75 second debounce time to prevent maloperation.

TV "ON" Output: *Figure 3* illustrates the CMOS inverter output circuit used.

In the manual mode of operation, the manual "ON" input sets this output to "0", the manual "OFF" input resets this output to "1". The manual "ON" input inhibits the auto "ON" output.

In the programmable mode, this output goes to "0" when the programmed "ON" time coincides with the real time (unless enable = 1). The output will then stay at "0" for the selected period of 5, 10, 20 or 30 minutes before returning to "1" state. During this period, a signal on the manual "ON" input will prevent the automatic switch-off.

Manual "OFF" input will always reset the output to a logic "1" state.

Auto "ON" TV Output: An additional output is provided to indicate that the TV is "ON" in the automatic mode of operation. This output goes to a logic "0" for the duration of the auto "ON" time. Manual "ON" switches this output back to a logic "1".

View Period Indicator: This output normally is a logic "1". When the TV switches on at the programmed time, this output transmits a 1 Hz waveform for the duration of the selected view period. Hence, it can be used to indicate that the TV is switched on for a limited period only by means of a flashing on-screen and/or off-screen display. The output will permanently return to "1" at the end of the viewing period or when a valid manual "ON" or "OFF" input signal is received during the view period.

BCD Outputs: *Figure 4* illustrates the open drain output circuits used, a) MM53100, b) MM53105.

With the use of the external respective pull-up and pull-down resistors, these outputs are designed to be compatible with the MM5840 and MM5841 TV display circuits.

Note. Case (a) for common V_{DD}, case (b) for common V_{SS} when used with the MM5840.

TABLE IA. Digit Select Code

DIGIT SELECT LINES	DIGIT DISPLAYED							
	S1	S10	*	M1	M10	*	H1	H10
D_X	1	0	0	1	1	0	0	1
D_Y	1	1	0	0	0	0	1	1
D_Z	0	0	0	0	1	1	1	1

TABLE IB. Period Select Code

PERIOD SELECT INPUTS		VIEW PERIOD PROGRAMMED
X	Y	
0	0	5 mins
0	1	10 mins
1	0	20 mins
1	1	30 mins

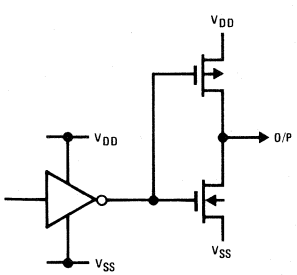


FIGURE 3. CMOS Output (TV "ON", Auto "ON", Indicator)

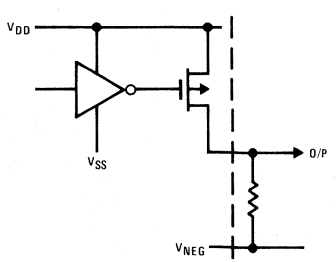


FIGURE 4a. BCD Outputs, MM53100

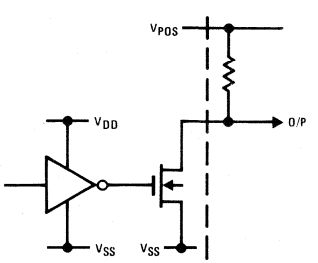


FIGURE 4b. BCD Outputs, MM53105

functional description (Continued)

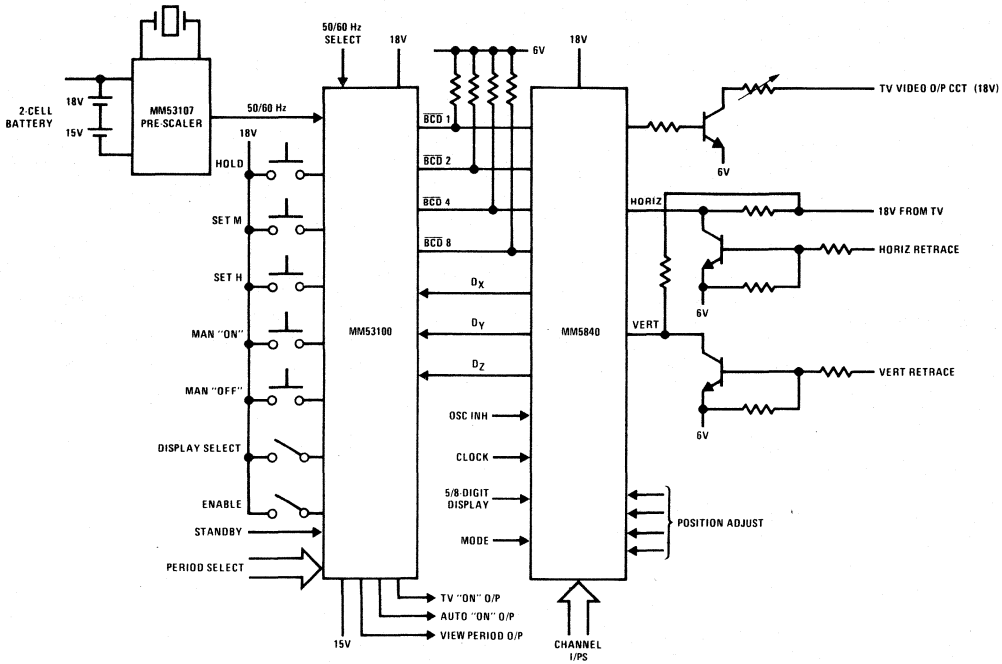


FIGURE 5a. Typical System Diagram, MM53100

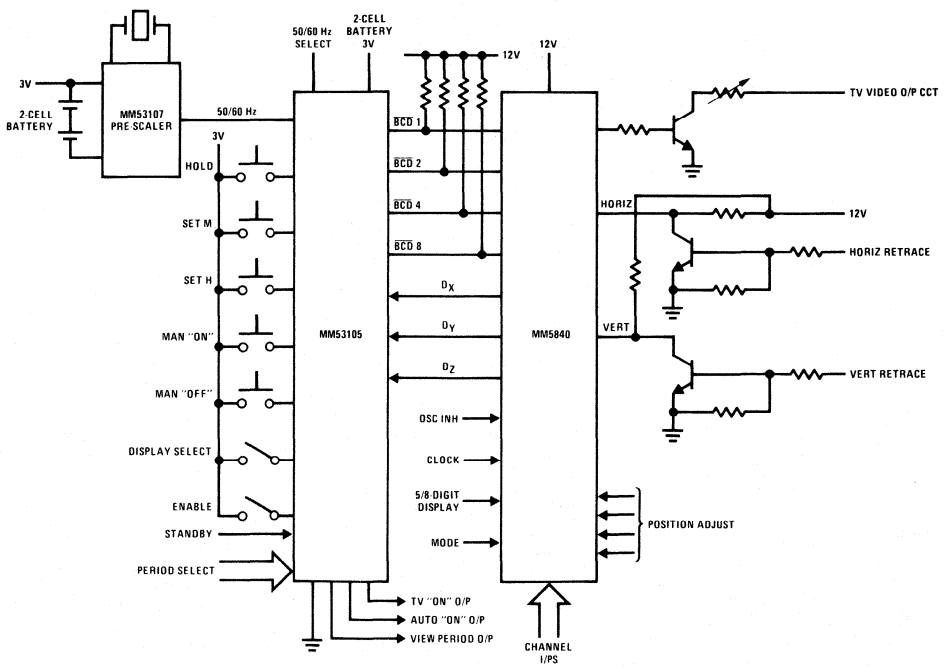


FIGURE 5b. Typical System Diagram, MM53105

National Semiconductor

MM53104 TV Game Clock Generator

general description

The MM53104 is a monolithic CMOS clock generator designed to generate the 2-phase non-overlapping clocks, ϕ_1 and ϕ_2, for the MM57100 TV game chip.

The MM53104 contains two independent oscillator circuits that can either be driven by an external input or be used as a Colpitts-type oscillator (e.g., crystal oscillator). The first oscillator (X1, X2) is designed to operate at 3.58 MHz and the output (X2) is fed internally to a divide-by-3 1/2 counter to generate the 1.0227 MHz ϕ_1 and ϕ_2 outputs required by the MM57100. The second oscillator (Y1, Y2) is a completely independent oscillator and is designed for a 4.5 MHz operation.

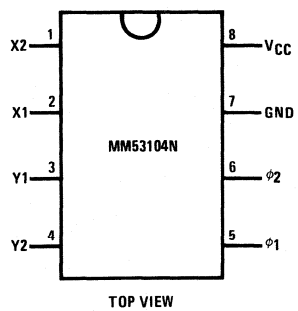
All pins are protected against static damages by diode clamps to both V_{CC} and ground.

features

- Directly drives MM57100
- Two on-chip oscillator circuits
- Low power consumption 250 mW typ @ 15V

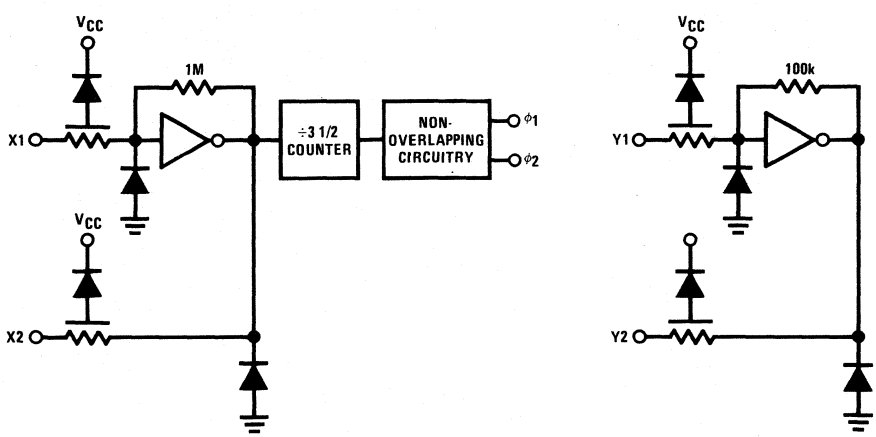
connection diagram

Dual-In-Line Package



TOP VIEW

logic diagrams



absolute maximum ratings (Note 1)

Voltage at Any Pin	−0.3V to V_{CC} +0.3V
V_{CC}	−0.3V to 16V
Recommended V_{CC}	15V ±5%
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation	500 mW
Lead Temperature (Soldering, 10 seconds)	300°C

dc electrical characteristics $14.25V \leq V_{CC} \leq 15.75V$

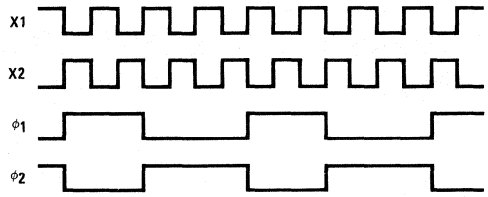
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC}	Quiescent Current	X1 = Y1 = V_{CC}			600	μA
	Operating Current	Y1 = GND		15		mA
V_{OH}	Output High Level, ϕ_1 or ϕ_2	V_{CC} = 15V	14.95			V
V_{OL}	Output Low Level, ϕ_1 or ϕ_2	V_{CC} = 15V			0.05	V
I_{OH}	Output Source Current, ϕ_1 or ϕ_2	V_{CC} = 15V, V_O = 13.5V	−7.0			mA
I_{OL}	Output Sink Current, ϕ_1 or ϕ_2	V_{CC} = 15V, V_O = 1.5V	11.0			mA

ac electrical characteristics V_{CC} = 15V, C_L = 15 pF, all limits apply across temperature.

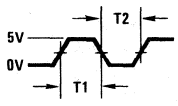
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
T_R	Rise Time of ϕ_1 or ϕ_2			15	30	ns
T_F	Fall Time of ϕ_1 or ϕ_2			15	30	ns
$T_{PW,\phi 1+}$	Positive Pulse Width of ϕ_1		410	455	510	ns
$T_{PW,\phi 1-}$	Negative Pulse Width of ϕ_1		470	520	570	ns
$T_{PW,\phi 2+}$	Positive Pulse Width of ϕ_2		510	570	600	ns
$T_{PW,\phi 2-}$	Negative Pulse Width of ϕ_2		380	410	470	ns
$T_{W,\phi 2-}$	Effective Negative Pulse Width of ϕ_2		405	440		ns
T_{dL1}	ϕ_1 Overlapping ϕ_2 Time			−13	5	ns
T_{dL2}	ϕ_2 Overlapping ϕ_1 Time			−2	10	ns
V_{OL1}	ϕ_1 Cross-Over ϕ_2 Voltage		V_{CC}−1.0	V_{CC}		V
V_{OL2}	ϕ_2 Cross-Over ϕ_1 Voltage		V_{CC}−2.0	V_{CC}−0.8		V

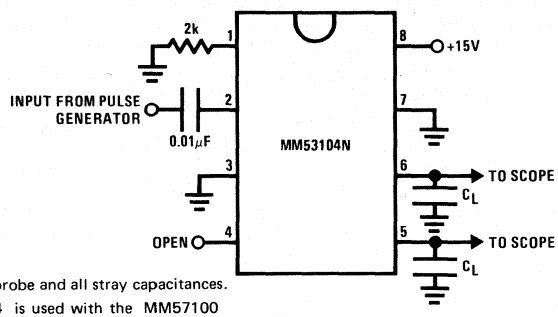
Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

timing diagram



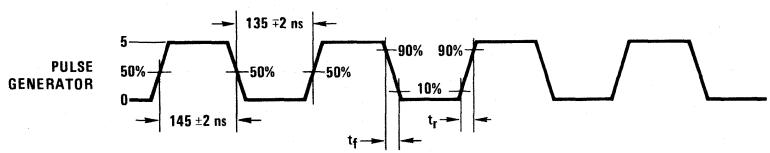
ac test circuit

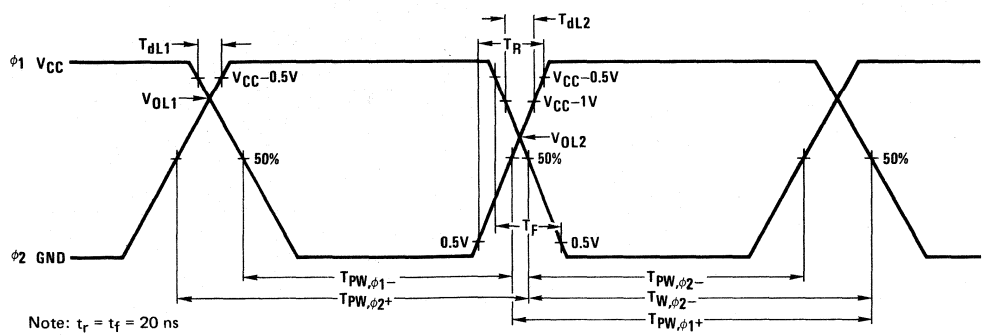




T1 = 145 ns
T2 = 135 ns
$t_r = t_f = 20$ ns
C_L = 15 pF including scope probe and all stray capacitances.
Note: When the MM53104 is used with the MM57100 and LM1889, the 4.5 MHz oscillator in the MM53104 is not needed and thus pin 3 should be grounded.

switching time waveforms





Note: $t_r = t_f = 20$ ns

National Semiconductor

MM55104, MM55106, MM55114, MM55116 PLL Frequency Synthesizer

general description

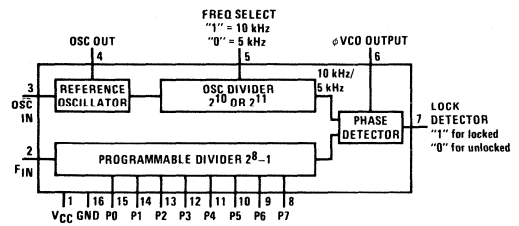
The MM55104 and MM55106 devices contain phase locked loop circuits useful for frequency synthesizer applications in C.B. transceivers. The devices operate off a single power supply and contain an oscillator, a 2^{10} or 2^{11} divider chain, a binary input programmable divider, and phase detector circuitry. The devices may be used in double I.F. or single I.F. systems. The MM55104, MM55114, MM55106 and MM55116, use a 10.24 MHz or 5.12 MHz quartz crystal to determine the reference frequency. The MM55106 and MM55116 have an output pin which provides a 5.12 MHz signal, which may be tripled for use as a reference oscillator frequency in two crystal systems. Also, the MM55106 provides an additional input to the programmable divider which allows $2^9 - 1$ division of the input frequency (F_{IN}). The inputs to the programmable divider are standard binary signals. Selection of a channel is accomplished by mechanical switches or by external electronic programming of the programmable divider.

The ϕVCO output provides a high level voltage (sources current) when the VCO frequency is lower than the lock frequency, and ϕVCO provides a low level voltage (sinks current) when the VCO frequency is higher than the lock frequency. The ϕVCO output goes to a high impedance (TRI-STATE®) condition under lock conditions, and the lock detector output LD goes to a high state under lock conditions.

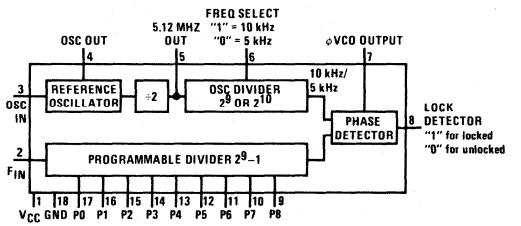
features

- Single power supply
- Low power CMOS technology
- Binary input channel select code
- 5 kHz or 10 kHz output from oscillator divide
- 5.12 MHz output (MM55106 and MM55116 only)
- On-chip oscillator
- Pull-down resistors on programmable divider inputs
- Low voltage operation—5V (MM55104, MM55106)
- High voltage operation—8V (MM55114, MM55116)

block diagrams



MM55104, MM55114



MM55106, MM55116

pin descriptions

P0–P8	Programmable divider inputs
F_{IN}	Frequency input from VCO (mixed down)
OSC IN	Oscillator amplifier input terminal
OSC OUT	Oscillator amplifier output terminal
LD	Lock detector
ϕVCO	Output of phase detector for control of the VCO
FS	Frequency division select 10 kHz or 5 kHz – "1" is 10 kHz; "0" is 5 kHz
5.12 MHz OUT	OSC Frequency divided by 2 output

truth table

Truth table for binary inputs to programmable divider.

N	P8	P7	P6	P5	P4	P3	P2	P1	P0
1	0	0	0	0	0	0	0	0	X
2	0	0	0	0	0	0	0	1	0
	.								
	.								
511	1	1	1	1	1	1	1	1	1

$F_{OUT} = F_{IN}/N$

1 = High voltage level, V_{OH}

0 = Low voltage level, V_{OL}

X = Don't care

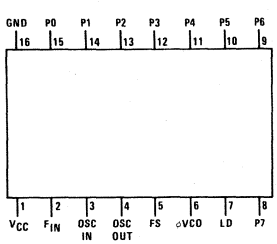
absolute maximum ratings

Voltage at Any Pin	V_{CC} + 0.3V to Gnd − 0.3V	V_{CC} Max	
Operating Temperature Range	−30°C to +75°C	MM55104, MM55106	7V
Storage Temperature Range	−40°C to +125°C	MM55114, MM55116	12V
		Lead Temperature (Soldering, 10 seconds)	300°C

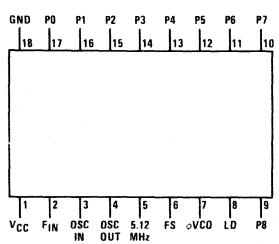
electrical characteristics $T_A = 25°C$

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})					
MM55104, MM55106		4.5	5.0	5.5	V
MM55114, MM55116		7.0	8.0	10.0	V
Supply Current (I_{CC})	Freq @ Osc In = 10 MHz, @ F_{IN} = 2.5 MHz, All Other I/O Pins Open, (Note 1)				
MM55104, MM55106	V_{CC} = 5V		3	10	mA
MM55114, MM55116	V_{CC} = 8V		8	16	mA
Logical "1" Input Voltage ($V_{IN(1)}$)					
P0–P8, FS, F_{IN}		(V_{CC}–0.4V)			V
Logical "0" Input Voltage ($V_{IN(0)}$)					
P0–P8, FS, F_{IN}				0.4	V
Logical "1" Output Voltage					
5.12 MHz Out, LD	I_O = 0.5 mA	(V_{CC}–0.5V)			V
ϕVCO	I_O = 0.4mA				
Osc Out	I_O = 0.25mA				
Logical "0" Output Voltage					
ϕVCO, 5.12 MHz Out, LD	I_O = −0.5mA			0.5	V
Osc Out	I_O = −0.25mA				
Logical "1" Input Current					
FS (Pull-Up)				1.0	μA
MM55104, MM55106 / MM55114, MM55116 P0–P8 (Pull-Down)	V_{CC} = 5V	5	20	50	μA
	V_{CC} = 8V	10	40	100	μA
Logical "0" Input Current					
P0–P8 (Pull-Down)				1.0	μA
MM55104, MM55106	V_{CC} = 5V	−10	−35	−100	μA
MM55114, MM55116 FS (Pull-Up)	V_{CC} = 8V	−30	−120	−300	μA
Toggle Frequency @ F_{IN}		3			MHz
Oscillator Frequency @ Osc In		10.24			MHz
TRI-STATE Leakage @ ϕVCO				1.0	μA

connection diagrams (Dual-In-Line Packages, Top View)



Order Number MM55104N or MM55114N
See Package 19



Order Number MM55106N or MM55116N
See Package 20

typical applications

INTRODUCTION TO FREQUENCY SYNTHESIS

The components of a frequency synthesizer are shown in *Figure 1*. The voltage controlled oscillator produces the desired output frequencies spaced f_V Hz apart according to the relation:

$$f_V = f_r N$$

The reference frequency, fr, must be equal to or less than the (channel) spacing between the frequencies being synthesized.

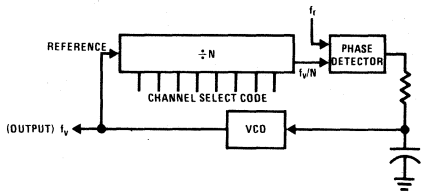


FIGURE 1. Basic Frequency Synthesizer

Although simple in concept, the circuit of *Figure 1* has certain difficulties. In CB, we are synthesizing the following frequencies:

Ch 1	26.965
Ch 2	26.975
.	.
.	.
.	.
Ch 23	27.225

Although the channel spacing is 10 kHz, a reference frequency of 5 kHz would be necessary due to the odd 5 kHz in the assigned channel. This in itself poses no problem; however, present technology limits the counting speed of programmable dividers to something less than 5 MHz, ruling out the approach shown in *Figure 1*.

Two solutions to this problem are shown in *Figure 2*.

Frequency prescaling shown in *Figure 2(a)* reduces the VCO frequency by M (a fixed number) to a frequency that can be divided by the programmable counter. The reference frequency f_r must also be reduced by M. In the case of CB, if M = 10, f_V = 26.965 MHz, the input to the programmable divider will be 2.6965 MHz, and the 5 kHz reference frequency will be reduced to 500 Hz. This poses problems in speed of response of the phase locked loop.

The second technique mixes the output frequency of the VCO with a stable fixed frequency to obtain a related reference frequency.

$$f_V = Nf_r + f_O$$

This technique has the advantage of allowing a 10 kHz reference frequency in the loop instead of 5 kHz.

Further complexity arises when one considers that the synthesizer must also generate a local oscillator signal as well as a transmitter input signal for the radio *(Figure 3)*. A system which provides these frequencies, as well as the proper offset to allow the programmable divider to operate within its limits is shown in the typical applications diagrams *(Figure 4)*. The only departure from the ideal situation shown in *Figure 3* is that the first IF frequency of 10.7 MHz must be changed to 10.695 MHz (a change of 5 kHz).

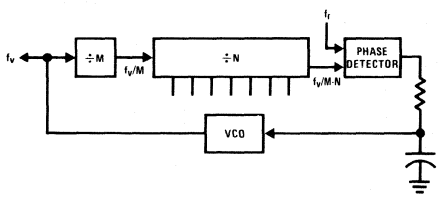


FIGURE 2(a). Frequency Prescaling

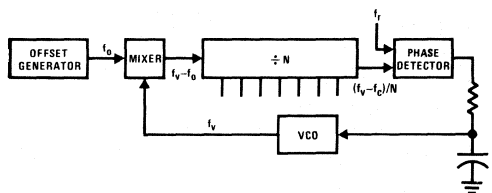


FIGURE 2(b). Frequency Offset

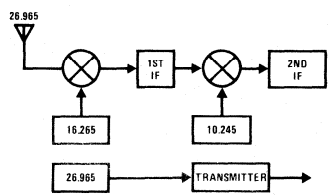


FIGURE 3. Signals Needed to Transmit and Receive Ch 1

typical applications (con't)

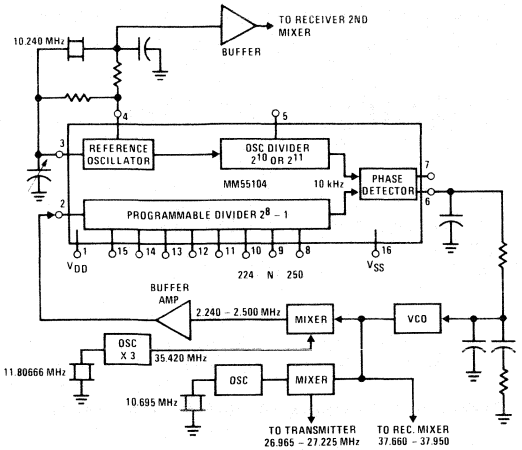


FIGURE 4(a). MM55104 or MM55114 3-Crystal Application

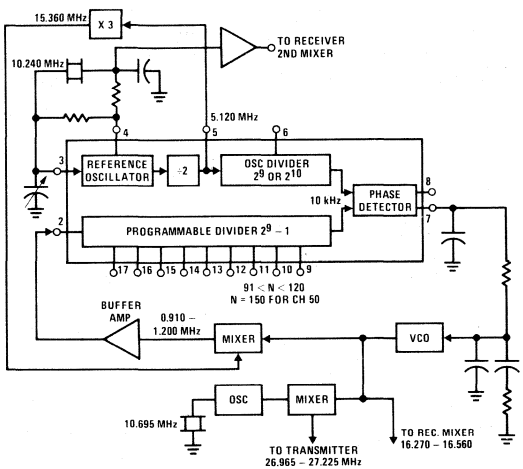


FIGURE 4(b). MM55106 or MM55116 2-Crystal, 23-Channel Application

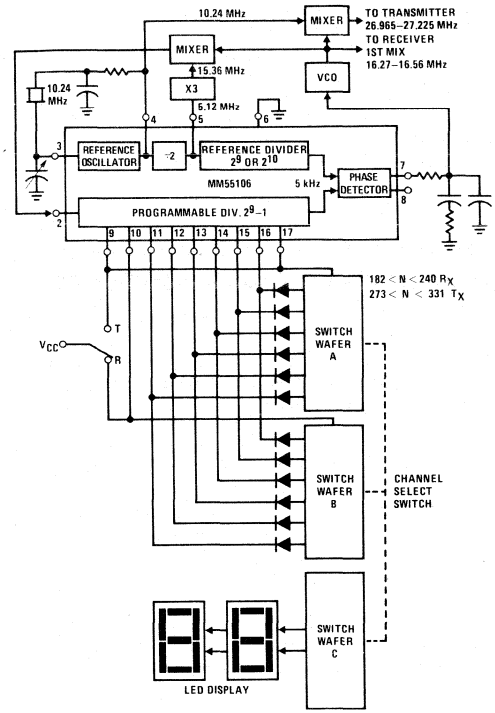


FIGURE 4(c). MM55106 or MM55116 Single Crystal, 23-Channel Application

National Semiconductor

MM5840 TV Channel Number (16 Channels) and Time Display Circuit

general description

The MM5840 TV Channel Number and Time Display Chip is a monolithic metal gate CMOS integrated circuit which generates a display of channel numbers (up to 16 channels) and time readouts on the television screen.

By external connection, it has the option of displaying the channel number only while switching channels with a period controlled by the external RC time constant of a timeout monostable.

This chip includes all the logic required to provide two modes of operation, namely channel number, or channel number and time display.

In addition, it can have a five (hour tens, hour units, colon, minute tens, and minute units) or eight digit (hour tens, hour units, colon, minute tens, minute units, colon, second tens, and second units) display, depending on the digit select input logic level.

By employing the video gating input together with the video output, a symmetrical blanked rectangular frame around the display may be generated on the TV screen.

This chip serves as a display generator with BCD channel inputs, as provided from the clock chips MM5318, MM53100 or MM53105. The position of the display on the TV screen can be controlled by adjusting external RC time constants.

functional description

The channel number and time readout circuit operates with a 2 to 4.5 MHz input clock. Counters are incorporated in the chip, operated by the input clock to keep track of the time slots of the display.

The position of the display is controlled by adjusting the external RC time constants of the horizontal and vertical monostable multivibrators.

A 7-segment decoder is used to decode either channel inputs or time which is stored temporarily in the channel number buffers or 4-bit latches, respectively, depending on the time slot of the display. Each digit of time is stored in a 4-bit latch while it is being decoded and displayed, and the next digit enters the latch while the horizontal sweep is between digits.

A time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that modulates the sweep of the television tube for the display on the screen.

features

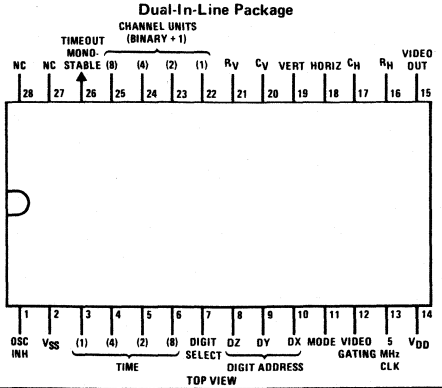
- 12 or 24-hour operation (controlled by clock chip)
- 5 or 8-digit display
- Channel number leading zero blanking
- Single power supply
- Channel number only or channel number and time display
- Video gating output for generating a symmetrical blanked rectangular frame around the display
- Oscillator inhibit output
- Channel number display only while switching channels
- 4-bit binary plus one code for channel numbers

functions

- 8-digit mode is selected by a logic "1" at digit select input
- Channel number and time mode is selected by a logic "1" at mode input
- Permanent channel number display is selected by a logic "1" at timeout monostable input

connection diagram

Dual-In-Line Package



Order Number MM5840N
See Package 23

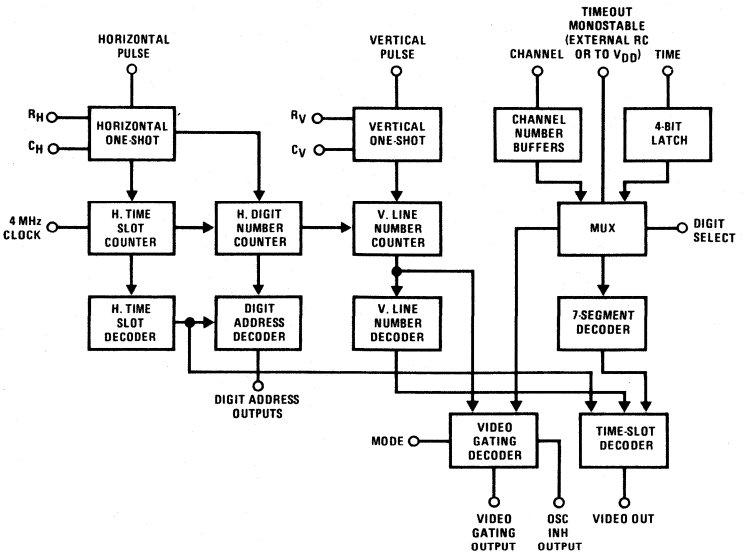
absolute maximum ratings

Supply Voltage ($V_{DD} - V_{SS}$)	−0.3V to +15V
Voltage at Any Pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics V_{DD} = 12V, V_{SS} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
V_{DD}	V_{SS} = 0	11	12	14	V
Power Supply Current				800	μA
Input Voltage Levels					
Time, Oscillator, Digit					
Select, and Mode Inputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Channel Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Input Frequency	Interfacing with MM53100, MM53105	2		4.5	MHz
Oscillator	Interfacing with MM5318	2		4.5	MHz
Horizontal	Pulse Width = 14 μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Video Gating, Osc. Inhibit					
Digit Address and Video Outputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal		15		50	μs
Vertical		1.5		13	ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1V	|−1|			mA
Logical High	V_{DD} − 1V	1			mA
Video Gating and Osc.					
Inhibit Outputs					
Logical Low	Output Forced Up to V_{DD} − 4.5V	|−2|			mA
Logical High	V_{DD} − 1V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			50		kΩ
$R_{HORIZONTAL}$			100		kΩ
$C_{TIMEOUT}$			5		μF
$R_{TIMEOUT}$				1	MΩ
Propagation Delay					
Video Gating and Osc.	From Input Clock to Oscillator			2	clock
Inhibit Outputs	Inhibit or Video Gating Outputs				pulses
Input Leakage				1	μA
Input Capacitance				5	pF

block diagram



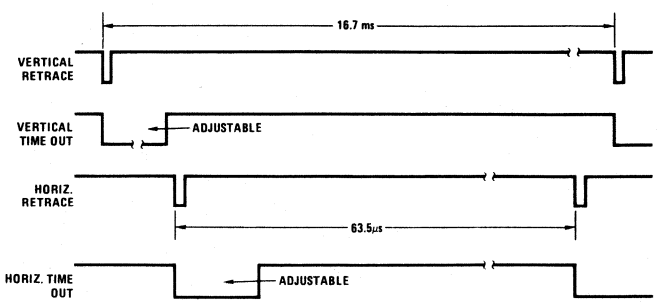
truth table

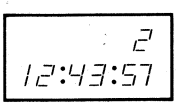
Digit Address (DX, DY, DZ) Codes

CODES	DURING RESET	DIGITS 1	2	3	4	5	6	7	8
DX	1	0	0	1	1	0	0	1	1
DY	1	1	0	0	0	0	1	1	1
DZ	1	1	1	1	0	0	0	0	1

timing diagram

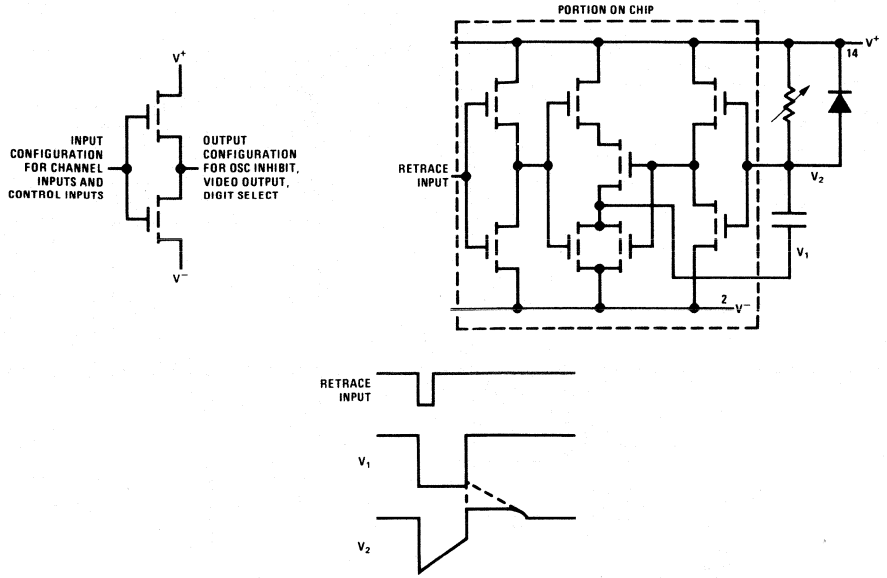
With Video Gating, Output Gated with Video Output



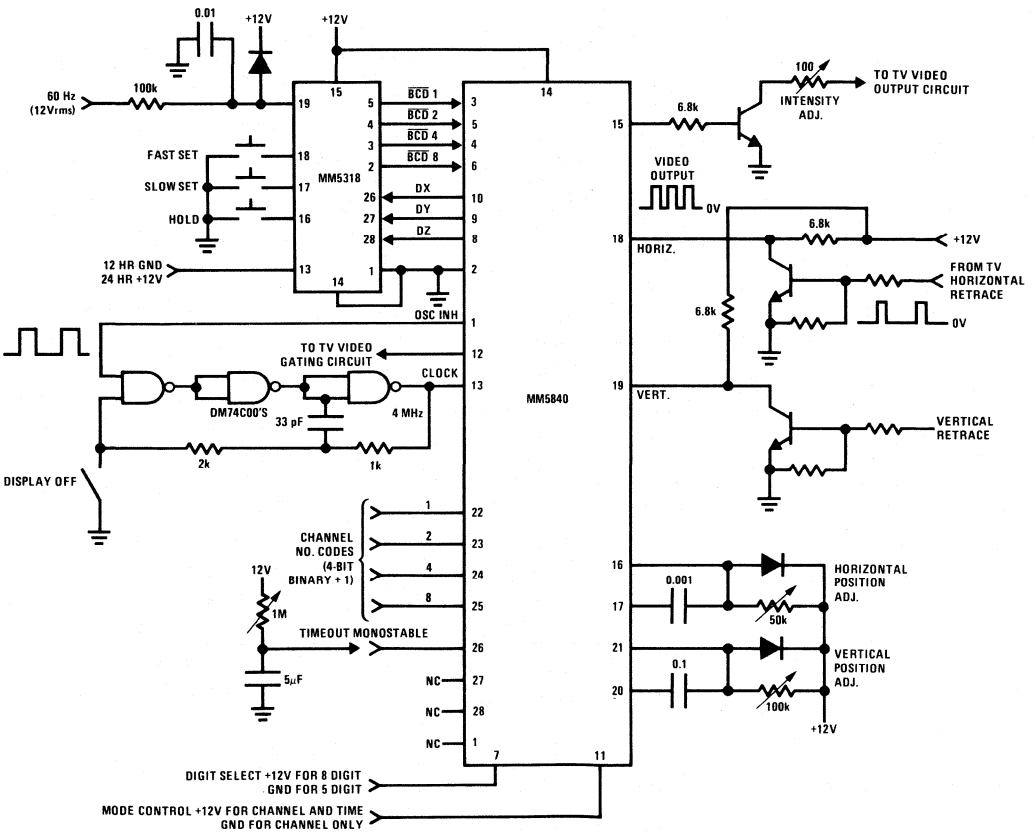


typical applications

Horizontal and Vertical One-Shot Circuit

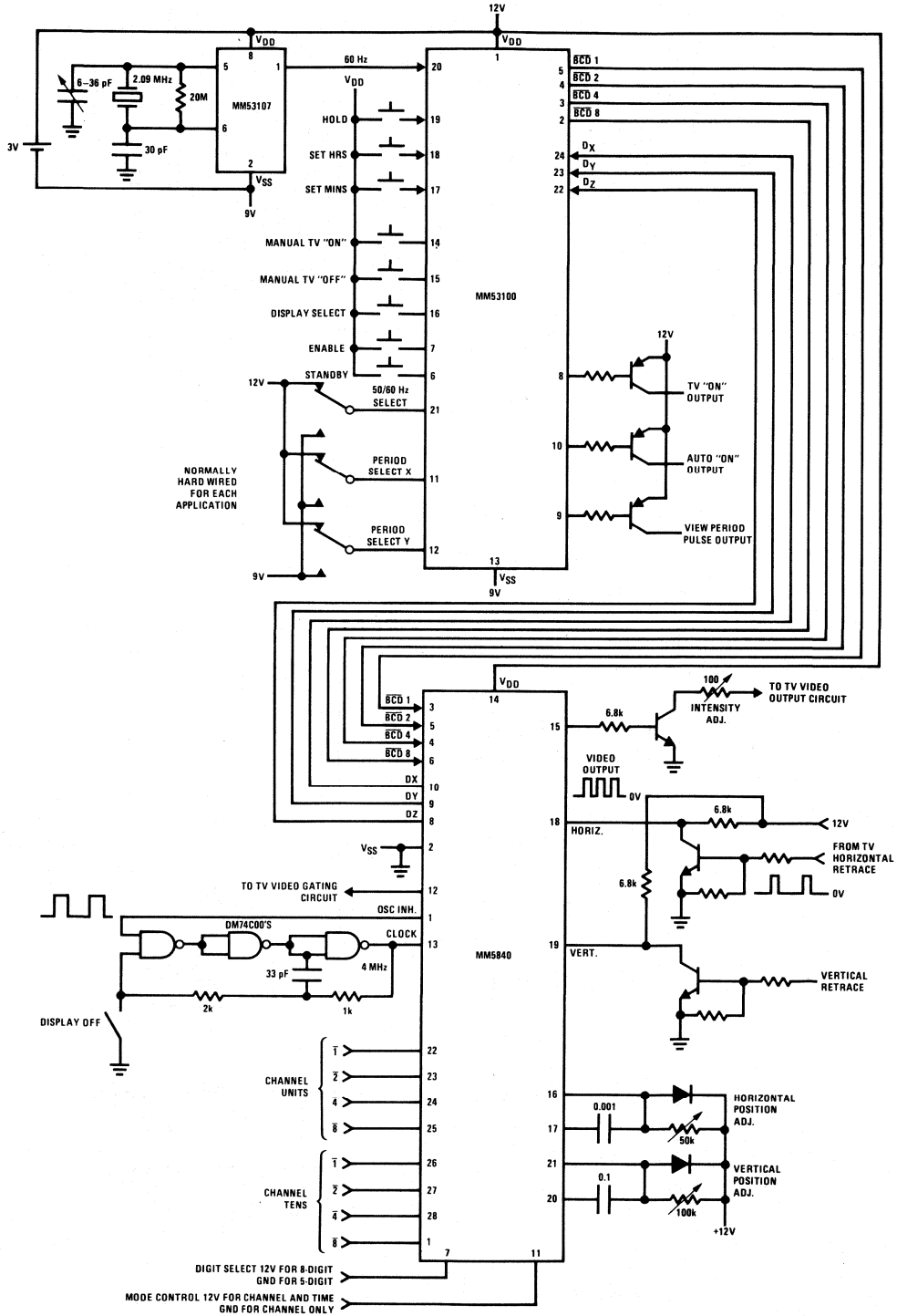


TV Channel and Time Display Interfacing MM5318



typical applications (Continued)

TV Channel and Time Display Interfacing MM53100



Note. For interfacing with MM53105, refer to MM53105 specifications.

National Semiconductor

MM5841 TV Channel Number and Time Readout Circuit

general description

The MM5841 TV Channel Number and Time Readout Circuit is a monolithic metal gate CMOS integrated circuit, which generates a display of channel number and time readouts on the television screen.

This chip includes all the logic required to provide two modes of operation, namely channel number, or channel number and time displays.

In addition, it can have a five (hour tens, hour units, colon, minute tens, and minute units) or eight digit (hour tens, hour units, colon, minute tens, minute units, colon, second tens, and second units) display, depending on the digit select input logic level.

This chip serves as a display generator between the BCD channel inputs, the clock chip (MM5318) and the television set. The position of the display on the TV screen can be controlled by adjusting the external RC time constants.

functional description

The channel number and time readout circuit operates with a 4 MHz input clock. Counters are incorporated in the chip, operated by the input clock to keep track of the time slots of the display.

The position of the display is controlled by adjusting the external RC time constants of the horizontal and vertical monostable multivibrators.

A 7-segment decoder is used to decode either channel inputs or time which is stored temporarily in the channel number buffers or 4 bit latches, respectively, depending on the time slot of the display. Each digit of time is stored in a 4-bit latch while it is being decoded and displayed, and the next digit enters the latch while the horizontal sweep is between digits.

A time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that modulates the sweep of the television tube for the display on the screen.

features

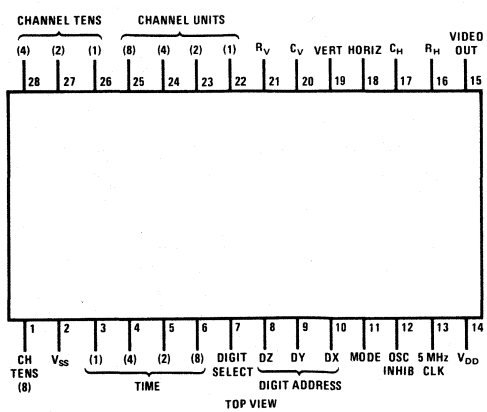
- 12 or 24 hour operation (controlled by clock chip)
- 5 or 8 digit display
- Channel number leading zero blanking
- Single power supply
- Channel number only or channel number and time display

functions

- 8 digit mode is selected by a logic "1" at digit select input
- Channel number and time mode is selected by a logic "1" at mode input

connection diagram

Dual-In-Line Package



Order Number MM5841N
See Package 23

absolute maximum ratings

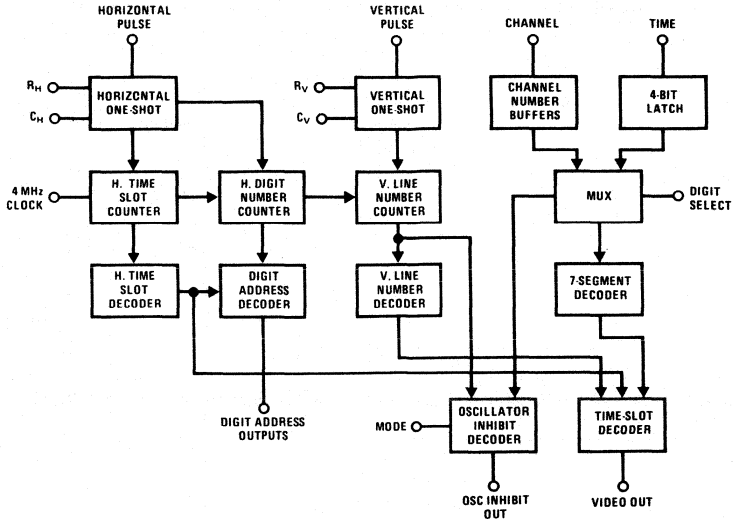
Supply Voltage ($V_{DD} - V_{SS}$)	−0.3V to +15V
Voltage at Any Pin	V_{SS} − 0.3V to V_{DD} + 0.3V
Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics

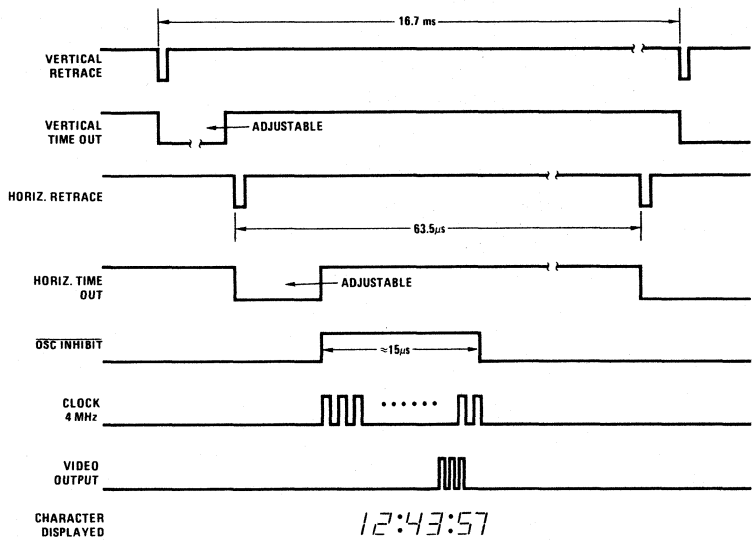
V_{DD} = 12V, V_{SS} = 0V, unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage					
V_{DD}	V_{SS} = 0	11	12	14	V
Power Supply Current				800	μA
Input Voltage Levels					
Time, Oscillator, Digit Select, and Mode Inputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Channel Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}−0.3	V_{DD}−5	V_{DD}−4.5	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
Input Frequency					
Oscillator		1	4	4.5	MHz
Horizontal	Pulse Width = 14μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Oscillator Inhibit, Digit Address and Video Outputs					
Logical Low		V_{SS}−0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}−0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal		15		50	μs
Vertical		1.5		13	ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1.0V	|−1|			mA
Logical High	V_{DD} − 1.0V	1			mA
Oscillator Inhibit Output					
Logical Low	Output Forced Up to V_{DD} − 4.5V	|−2|			mA
Logical High	V_{DD} − 1.0V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			50		kΩ pot
$R_{HORIZONTAL}$			100		kΩ pot
Propagation Delay					
Oscillator Inhibit Output	From Input Clock to Oscillator Inhibit Output			2	clock pulses
Input Leakage				1	μA
Input Capacitance				5	pF

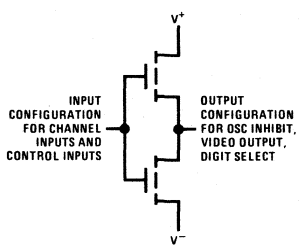
block diagram

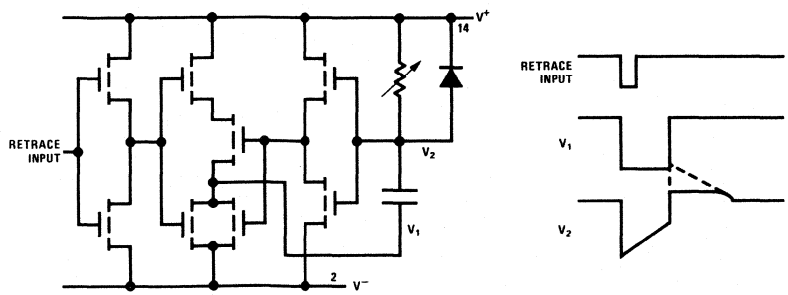


timing diagram



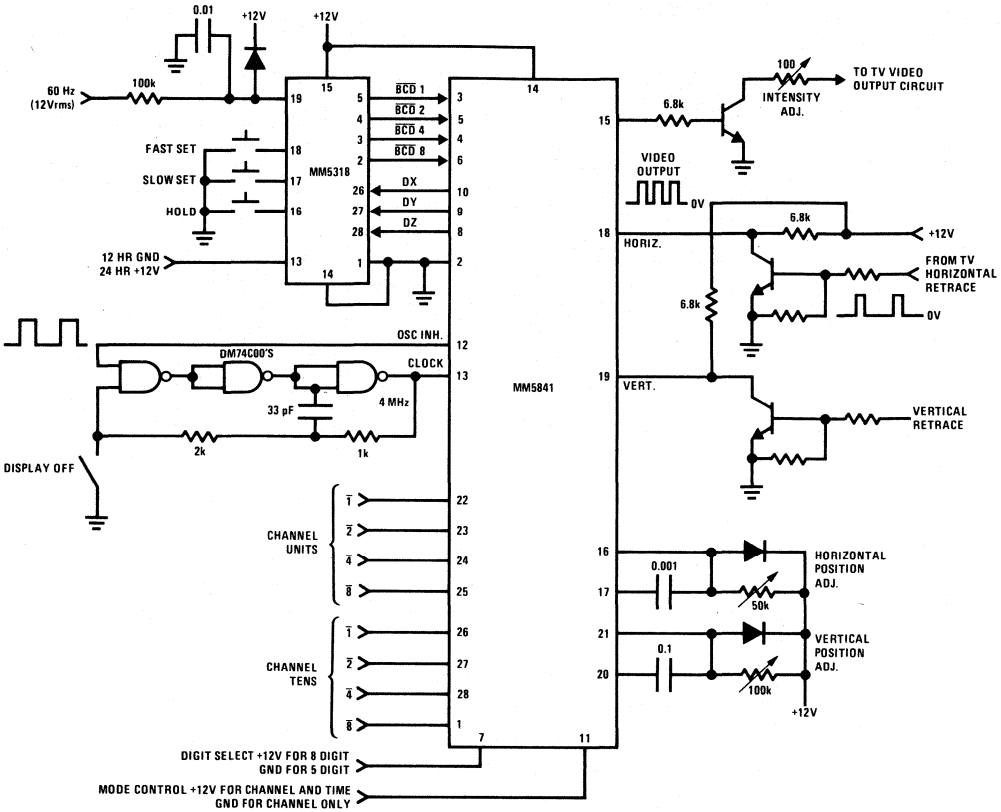
typical applications





Horizontal and Vertical One-Shot Circuit

typical applications (con't)



TV Channel and Time Display

National Semiconductor

MM58106 Digital Clock and TV Display Circuit

general description

The MM58106 is a monolithic CMOS integrated circuit which generates a display of channel number and time on the television screen. The circuit can either display channel number (2–83) or program number (1–16). Time display can be 4 or 6-digit, in either 12 or 24-hour mode. Timekeeping is controlled from a 50 Hz or 60 Hz input. The position of the display on the TV screen is controlled by adjusting the external RC time constants.

The circuit is packaged in a 28-lead dual-in-line epoxy package.

features

- Single chip clock and display
- 12 or 24-hour operation
- 5 or 8-digit time display
- Channel or program number display
- 50/60 Hz operation
- Channel and time display on channel change

block diagram

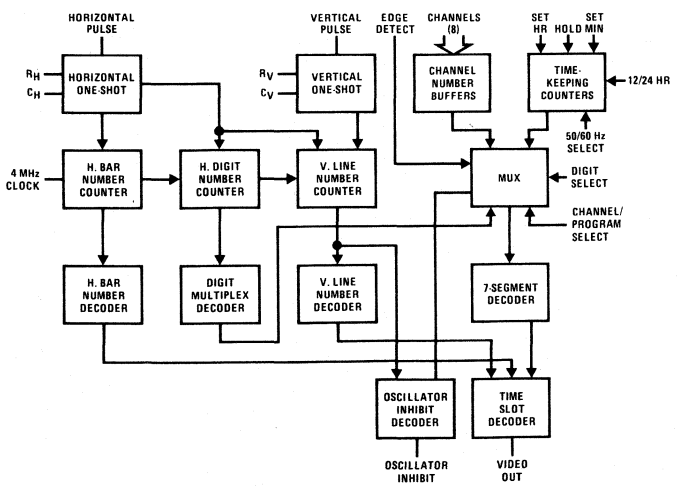


FIGURE 1

connection diagram

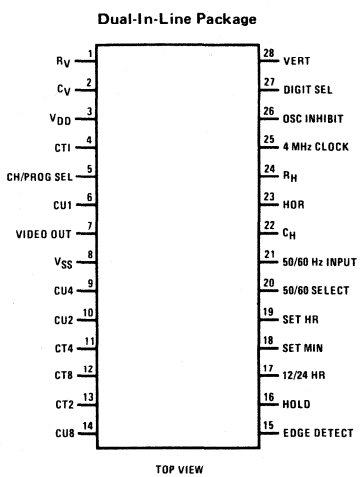


FIGURE 2

Order Number MM58106N
See Package 23

absolute maximum ratings

Supply Voltage ($V_{DD} - V_{SS}$)	5.5V
Voltage at Any Pin	V_{SS} – 0.3V to +5.5V
Operating Temperature	0°C to +70°C
Storage Temperature	–55°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

electrical characteristics V_{DD} = 5V, V_{SS} = 0V, unless otherwise specified

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage, V_{DD}	V_{SS} = 0	4.75	5	5.25	V
Power Supply Current				800	μA
Input Voltage Levels					
Channel Inputs					
Logical Low		V_{SS}–0.3	V_{DD}–5	V_{DD}–4.5	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Horizontal and Vertical Inputs					
Logical Low		V_{SS}–0.3	V_{DD}–5	V_{DD}–4.5	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Set Mins, Set Hours, Hold, 12/24-Hour Select, 50/60 Hz Select, Channel/ Program Select	Internal Pull-Up Resistor to V_{DD} (600k Min)				
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.3	V
Logical High			Open		
All Others					
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.3	V
Logical High		V_{DD}–0.3	V_{DD}	V_{DD}+0.3	V
Input Frequency					
4 MHz Clock		1	4	4.5	MHz
Horizontal	Pulse Width = 14 μs		15.75		kHz
Vertical	Pulse Width = 1 ms		60		Hz
Output Voltage Levels					
Oscillator Inhibit and Video Output					
Logical Low		V_{SS}–0.3	V_{SS}	V_{SS}+0.9	V
Logical High		V_{DD}–0.5	V_{DD}	V_{DD}+0.3	V
One-Shot Output Pulse Duration					
Horizontal			50		μs
Vertical			13		ms
Output Drive					
Video Output					
Logical Low	V_{SS} + 1V	(–1)			mA
Logical High	V_{DD} – 1V	1			mA
Oscillator Inhibit Output					
Logical Low	Output Forced Up to V_{DD}–4.5V	(–2)			mA
Logical High	V_{DD} – 1V	0.2			mA
External RC					
$C_{VERTICAL}$			0.1		μF
$C_{HORIZONTAL}$			0.001		μF
$R_{VERTICAL}$			100		kΩ pot
$R_{HORIZONTAL}$			100		kΩ pot
Propagation Delay Oscillator Inhibit Output	From Input Clock to Oscillator Inhibit Output			2	clock pulses
Input Leakage				1	μA
Input Capacitance				5	pF
Edge Detect Pulse Duration	C = 2 μF, R = 1 MΩ		2		sec

functional description

A block diagram of the MM58106 TV timer is shown in *Figure 1*. A connection diagram is shown in *Figure 2*. Unless otherwise indicated, the following discussions are based on *Figure 1*.

50 or 60 Hz Input: This input has a shaping circuit which allows using a filtered sinewave input. A simple RC filter such as shown in *Figure 4* should be used to remove possible line voltage transients that could either cause the clock to gain time or damage the device. The input should swing between V_{SS} and V_{DD}. The shaper output drives a counter chain which performs the timekeeping function.

Alternatively, in a crystal controlled battery operated system, an oscillator and prescaler circuit such as the MM5369 could be used as a timebase.

50 or 60 Hz Select Input: This input programs the prescale counter to divide by either 50 or 60 to obtain a 1 pps timebase. The counter is programmed for 60 Hz operation by connecting this input to V_{SS}. An internal 1 MΩ pull-up resistor is common to this pin; simply leaving this input unconnected programs the clock for 50 Hz operation.

Time Setting Inputs: Inputs to set hours and set minutes as well as a hold input, are provided. Internal 1 MΩ pull-up resistors provide the normal timekeeping function. Switching any one of these inputs (one at a time) to "0" results in the desired time setting function. Set Hours advances hours information at 1 hour per second, and Set Minutes advances minutes information at one minute per second, without roll over into the hours counter. The hold input stops the clock to the minutes counter and resets the seconds counter.

Display Control: The channel number and time display circuits operate from the 4 MHz input clock frequency. The horizontal and vertical position of the display is controlled by adjusting the external RC time constants (R_H, C_H, R_V, C_V).

These monostables are triggered by the horizontal and vertical retrace signals as shown in the timing diagram in *Figure 3*.

A 7-segment decoder is used to decode either channel inputs or time. Also a time slot decoder is employed to decode the appropriate time slot and the digit to be displayed. It generates a video output signal that can modulate the sweep of the television tube for the on-screen display.

Channel/Program Number Select: This control pin has a pull-up resistor to V_{DD} and, with the input open, the chip will accept a binary plus 1 code on the CU1 to CU8 inputs and display the program number. For example, an input code of 0000 will indicate channel 1 and 1111 will indicate channel 16.

With this input at "0", inputs CU1 to CU8 and CT1 to CT8 will accept BCD inputs for channel units and channel tens respectively, and display channels 2–83.

Edge Detect: On program change, the time and number will be displayed for a period depending on the external capacitor and resistor connected to the Edge Detect pin *(Figure 4)*.

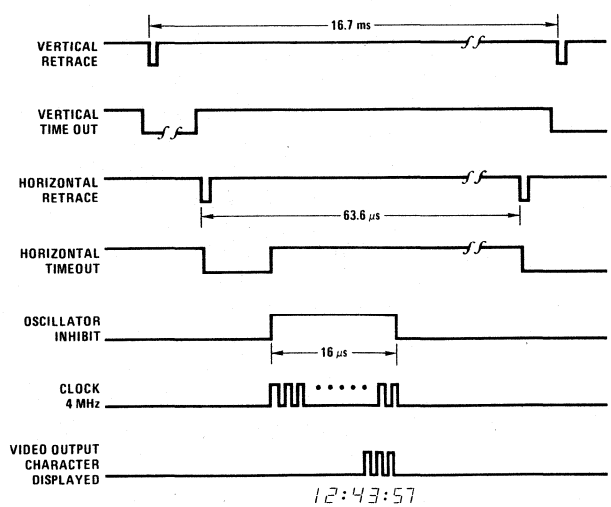


FIGURE 3. Timing Diagram

typical applications

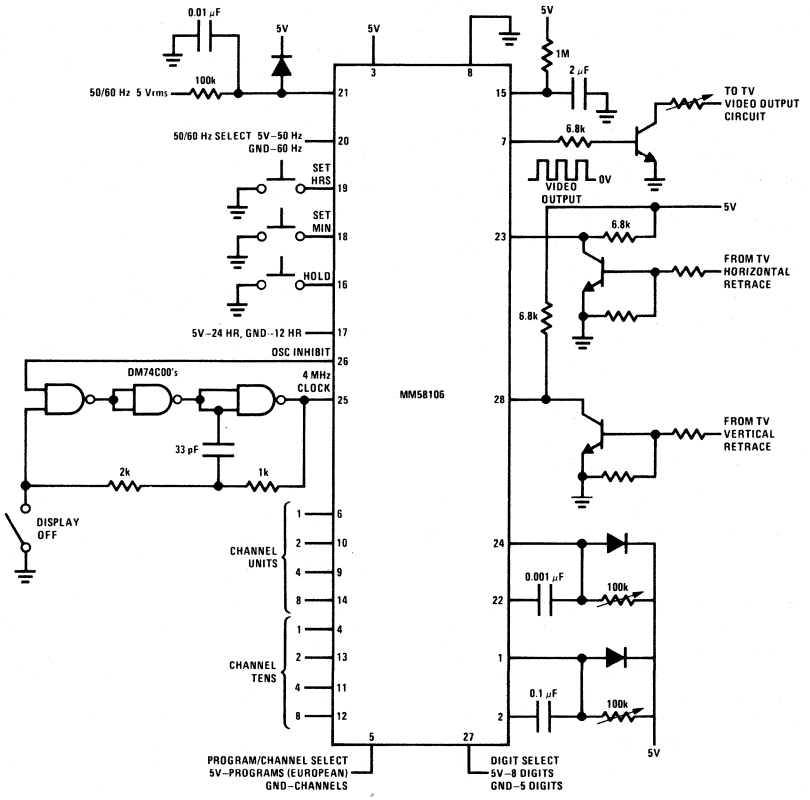


FIGURE 4.

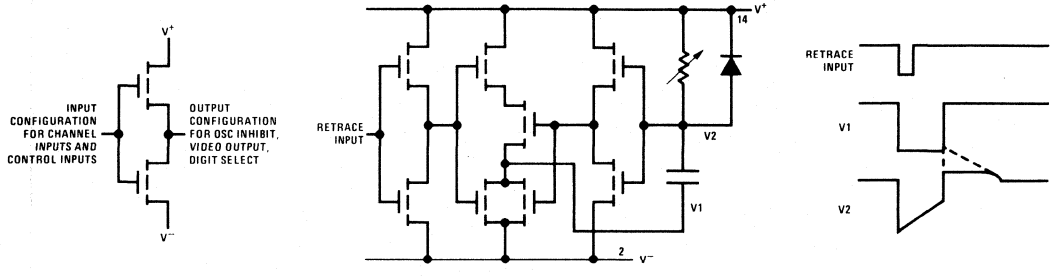


FIGURE 5. Horizontal and Vertical One-Shot Circuit

High Reliability CMOS

National Semiconductor

High Reliability CMOS

Introduction

For years National's products have been acknowledged as among the most reliable available. It is only natural, therefore, that National should be committed to the Military/Aerospace semiconductor market, where reliability is of paramount importance. In the forefront of our Hi-Rel product line, our CMOS devices (both 4000 series and 54C series) are available with a wide range of screening options tailored to meet all levels of user needs. In addition to the basic flows shown on the following pages (and ANY of our Mil-grade CMOS devices can be screened to any of those flows), we also offer rad-hardened CMOS (1×10^6 rads [Si]), SEM acceptance, and numerous other special tests. Regardless of your screening needs, whether you have designed around A series, B series, or 54C, we have what you need. And, since we can meet those needs with *standard* flows, we can meet them economically. We can also offer these devices, at the chip level, for use in hybrid circuits, with screening on a sample basis, if required.

CMOS 883/RETS Reliability Program

Purpose

This specification establishes the requirements for screening and processing of integrated circuits in accordance with MIL-STD-883, Class B or C.

Intent

This program is intended to provide the user with the ability to procure standardized, off-the-shelf integrated circuits manufactured by National Semiconductor Corporation that are fully compliant to MIL-STD-883.

APPLICABLE DOCUMENTS

The following specifications and standards, of the issue in effect on the date of invitation for bids or request for proposal, form a part of this specification to the extent specified herein.

Specifications

Military

MIL-M-55565	Microcircuits, Packaging of
MIL-M-38510	General Specification for Microcircuits
MIL-C-45662	Calibration System Requirements
MIL-Q-9858	Quality System Requirements

Standards

Military

MIL-STD-105	Sampling Procedures and Tables
MIL-STD-883	Test Methods and Procedures for Microelectronics

Detail Specifications

The detail specification for a particular device is the manufacturer's RETS (Rel Electrical Test Spec. — see figure 2).

GENERAL REQUIREMENTS

The individual requirements shall be as specified herein and in accordance with the applicable detail specification. The static and dynamic electrical performance requirements of the integrated circuits and electrical test methods shall be as specified in the detail specification.

Process Conditioning, Testing, Reliability and Quality Assurance Screening

Two levels of reliability and quality assurance for integrated circuits are provided for in this specification. Process conditioning, screening and testing shall be as specified in "Conditions and Methods of Test."

MIL-STD-883 Q.A. Process Level	Applicable Process Flow Chart	Suffix Indicator
B	figure 1a	/883B
C	figure 1b	/883C

Qualification

The devices furnished under this specification shall be products which have been produced and tested and have passed the qualification tests specified herein. Successful qualification for a given level results in qualification approval for that level and all lower product assurance levels of that device (reference appendix E, MIL-M-83510C).

Alternate Qualification

In lieu of meeting the requirements of qualification, the manufacturer may establish qualification by performing an initial, one-time qualification test. Qualification testing shall be performed on each generic family supplied. Upon successful completion of the qualification program, the manufacturer shall remain qualified for a period not to exceed 12 months.

Quality Conformance Inspection

Devices furnished under this specification shall be products which have been produced and tested in conformance with all the provisions of this specification for the applicable level. Devices which have been accepted as conforming to a given product assurance level may be furnished as conforming to any other level for which they meet or exceed the quality conformance requirements.

MARKING

Marking on Each Device

The following marking shall be placed on each integrated circuit:

a) Index point
b) Part number
c) Product assurance level
d) Inspection lot identification code
e) Manufacturer's identification

Marking on Initial Container

All of the marking specified in b through e above shall appear on the initial protection or wrapping for delivery.

Marking Permanence

Marking shall be permanent in nature and remain legible after testing. Damage to marking caused by mechanical fixturing in Group B and C tests shall not be cause for lot rejection.

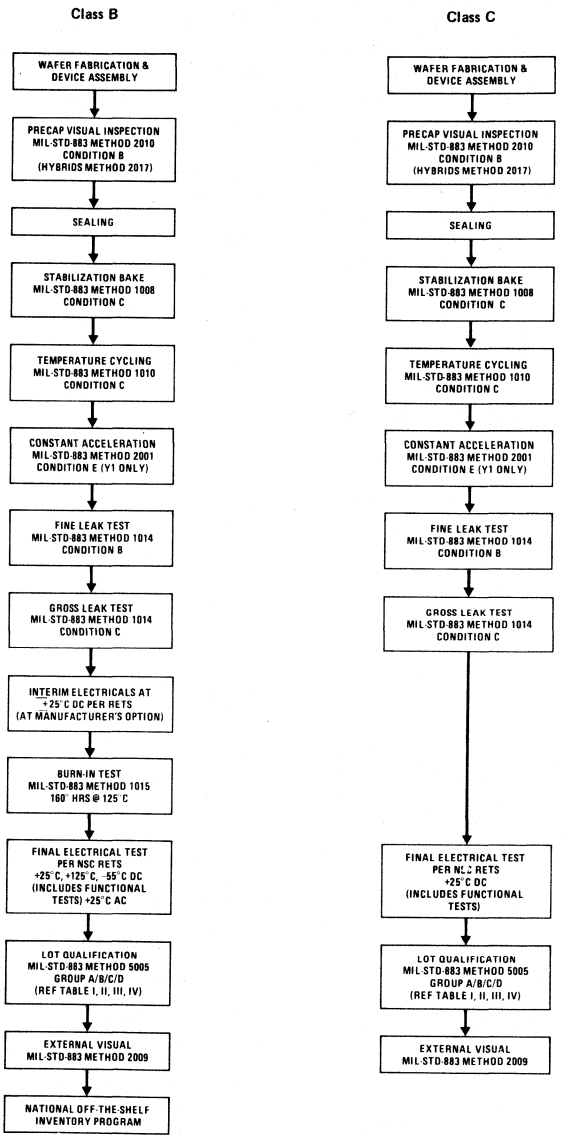


Figure 1. MIL-STD-883 Screening

Device: MM4601B

Parameter	Symbol	Conditions	Test #	RC4601BXRA +25°C Min	RC4601BXRA +25°C Max	RC4601BXHA +125°C Min	RC4601BXHA +125°C Max	RC4601BXLA -55°C Min	RC4601BXLA -55°C Max	Drift Limits +25°C	Units
The following parameters are measured directly:											
Logical "0" Output Voltage	V_{OL}	V_{DD} = 10V, I_{OUT} = 0μA, V_{IH} = 10V, V_{IL} = 0V (4)	120, 121		0.05		0.05		0.05		V
		V_{DD} = 5V, I_{OUT} = 0μA, V_{IH} = 5V, V_{IL} = 0V (4)	112, 113		0.05		0.05		0.05		V
		V_{DD} = 15V, I_{OUT} = 0μA, V_{IH} = 15V, V_{IL} = 0V (4)	126, 127		0.05		0.05		0.05		V
Logical "1" Output Voltage	V_{OH}	V_{DD} = 10V, I_{OUT} = 0μA, V_{IH} = 10V, V_{IL} = 0V (4)	70, 71	9.95		9.95		9.95			V
		V_{DD} = 15V, I_{OUT} = 0μA, V_{IH} = 15V, V_{IL} = 0V (4)	76, 77	14.95		14.95		14.95			V
		V_{DD} = 5V, I_{OUT} = 0μA, V_{IH} = 5V, V_{IL} = 0V (4)	62, 63	4.95		4.95		4.95			V
Logical "1" Input Current	I_{IH}	V_{DD} = 15V, V_{IN} = 15V (all inputs tied) (2)	33		100		1000		100		nA
Logical "0" Input Current	I_{IL}	V_{DD} = 15V, V_{IN} = 0V (all inputs tied) (2)	34		-100		-1000		-100		nA
Output Source Current	I_{SOURCE}	V_{DD} = 15V, V_{OUT} = 13.5V, V_{IH} = 15V, V_{IL} = 0V (4)	74, 75	-3.4		-2.4		-4.2			mA
		V_{DD} = 10V, V_{OUT} = 9.5V, V_{IH} = 10V, V_{IL} = 0V (4)	66, 67	-1.3		-0.9		-1.6			mA
		V_{DD} = 5V, V_{OUT} = 4.6V, V_{IH} = 5V, V_{IL} = 0V (4)	55, 57	-0.51		-0.36		-0.64			mA
		V_{DD} = 5V, V_{OUT} = 0V, V_{IH} = 5V, V_{IL} = 0V (4)	60, 61	-1.85		-1.26		-2.2			mA
Output Sink Current	I_{SINK}	V_{DD} = 15V, V_{OUT} = 1.5V, V_{IH} = 15V, V_{IL} = 0V (4)	124, 125	3.4		2.4		4.2			mA
		V_{DD} = 10V, V_{OUT} = 0.5V, V_{IH} = 10V, V_{IL} = 0V (4)	116, 117	1.3		0.9		1.6			mA
		V_{DD} = 5V, V_{OUT} = 0.4V, V_{IH} = 5V, V_{IL} = 0V (8)	102-105	0.51		0.36		0.64			mA
		V_{DD} = 5V, V_{OUT} = 5V, V_{IH} = 5V, V_{IL} = 0V (8)	106-111	2.06		1.4		2.2			mA
Power Supply Current	I_{CC}	V_{DD} = 15V, V_{IH} = 15V, V_{IL} = 0V (4)	42-45		1.0		30		1.0		μA
		V_{DD} = 10V, V_{IH} = 10V, V_{IL} = 0V (4)	46-51		0.5		15		0.5		μA
		V_{DD} = 5V, V_{IH} = 5V, V_{IL} = 0V (4)	52-55		0.25		7.5		0.25		μA
		V_{DD} = 18V, V_{IH} = 18V, V_{IL} = 0V (4)	36-41		50						μA
The following parameters are measured indirectly or go-no-go only:											
Logical "1" Input Voltage	V_{IH}	V_{DD} = 5V, V_{OUT} = 4.5V (min) (4)	64, 65	3.5		3.5		3.5			V
		V_{DD} = 10V, V_{OUT} = 9.0V (min) (4)	72, 73	7		7		7			V
		V_{DD} = 15V, V_{OUT} = 13.5V (min) (4)	100, 101	11		11		11			V
Logical "0" Input Voltage	V_{IL}	V_{DD} = 5V, V_{OUT} = 0.5V (max) (2)	130B, 131B		1.5		1.5		1.5		V
		V_{DD} = 10V, V_{OUT} = 1.0V (max) (4)	122, 123		3		3		3		V
		V_{DD} = 15V, V_{OUT} = 1.5V (max) (2)	130A, 131A		4		4		4		V
		Note: V_{OUT} is measured with inputs at V_{IH}, V_{IL}									
The following parameters are guaranteed by design (but may be measured at extra cost):											
Propagation Delay Time	t_{pd0}, t_{pd1}	V_{DD} = 5V			250						ns
Transition Time	t_{t0}, t_{t1}	V_{DD} = 5V			200						ns

Figure 2. Rel Electrical Test Spec

Device: MM4601B

Parameter	Symbol	Conditions	Test #	RC4601BXRA +25°C Min	RC4601BXRA +25°C Max	RC4601BXHA +125°C Min	RC4601BXHA +125°C Max	RC4601BXLA −55°C Min	RC4601BXLA −55°C Max	Drift Limits +25°C	Units
The following parameters are guaranteed by design:											
Propagation Delay Time	t_{pd0}, t_{pd1}	V_{DD} = 10V			100						ns
		V_{DD} = 15V			70						ns
Transition Time	t_{t0}, t_{t1}	V_{DD} = 10V			100						ns
		V_{DD} = 15V			80						ns
Average Input Capacitance	C_{IN}				7.5						pF

Figure 2. Rel Electrical Test Spec (cont.)

Device: MM54C00

Parameter	Symbol	Conditions	Test #	RC54C00BRA +25°C Min	RC54C00BRA +25°C Max	RC54C00BHA +125°C Min	RC54C00BHA +125°C Max	RC54C00BLA -55°C Min	RC54C00BLA -55°C Max	Drift Limits +25°C	Units
The following parameters are measured directly:											
Logical "1" Output Voltage	V_{OH}	V_{CC} = 5V, I_{OUT} = -10 μA, V_{IN} = 1.5V (all inputs)	45	4.5		4.5		4.5			V
		V_{CC} = 10V, I_{OUT} = -10 μA, V_{IN} = 2V (all inputs)	47	9.0		9.0		9.0			V
		V_{CC} = 4.5V, I_{OUT} = -360 μA, V_{IN} = 1V (all inputs)	43	2.4		2.4		2.4			V
Logical "0" Output Voltage	V_{OL}	V_{CC} = 5V, I_{OUT} = 10 μA, V_{IN} = 3.5V (all inputs)	46		0.5		0.5		0.5		V
		V_{CC} = 10V, I_{OUT} = 10 μA, V_{IN} = 8V (all inputs)	50		1.0		1.0		1.0		V
		V_{CC} = 4.5V, I_{OUT} = 360 μA, V_{IN} = 4V (all inputs)	44		0.4		0.4		0.4		V
Logical "1" Input Current	I_{IH}	V_{CC} = 15V, V_{IN} = 15V, other inputs at 0	33		0.15		1.0		0.15		μA
Logical "0" Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V, other inputs at 15V	34		-0.15		-1.0		-0.15		μA
Quiescent Device Current	I_{CC}	V_{CC} = 15V, V_{IH} = 15V, V_{IL} = 0V	40,41,42		0.15		15		0.15		μA
Output Source Current	I_{SOURCE}	V_{CC} = 5V, V_{OUT} = 0V, V_{IN} = 5V (1 input per gate, other inputs at 0)	51, 52	-1.75		-1.2		-1.75			mA
		V_{CC} = 10V, V_{OUT} = 0V, V_{IN} = 10V (1 input per gate, other inputs at 0)	53, 54	-8.0		-5.6		-8.0			mA
Output Sink Current	I_{SINK}	V_{CC} = 5V, V_{OUT} = 5V, V_{IN} = 5V (all inputs)	55	1.75		1.20		1.75			mA
		V_{CC} = 10V, V_{OUT} = 10V, V_{IN} = 10V (all inputs)	56	8.0		5.6		8.0			mA
		V_{CC} = 4.5V, V_{OUT} = 0.4V, V_{IN} = 4V (all inputs)	57	360		360		360			pA
The following parameters are measured indirectly (go-no-go only):											
Logical "1" Input Voltage	V_{IH}	V_{CC} = 5V		3.5		3.5		3.5			V
		V_{CC} = 10V		8.0		8.0		8.0			V
		V_{CC} = 4.5V (LP to CMOS)		3.0		3.0		3.0			V
		V_{CC} = 4.5V (CMOS to LP)		4.0		4.0		4.0			V
Logical "0" Input Voltage	V_{IL}	V_{CC} = 5V			1.5		1.5		1.5		V
		V_{CC} = 10V			2.0		2.0		2.0		V
		V_{CC} = 4.5V (LP to CMOS)			0.8		0.8		0.8		V
		V_{CC} = 4.5V (CMOS to LP)			1.0		1.0		1.0		V
Power Dissipation	PD	V_{CC} = 15V			2.25		2.25		2.25		μW
The following parameters are tested go-no-go, but may be read and recorded at extra cost:											
Propagation Delay	t_{pd1}	V_{CC} = 5V, C_L = 50 pF			90						ns
	t_{pd0}	V_{CC} = 5V, C_L = 50 pF			90						ns
The following parameters are guaranteed through other testing:											
Logical "1" Output Voltage	V_{OH}	V_{CC} = 4.5V, I_{OUT} = -10 μA		4.4		4.4		4.4			V
Logical "0" Output Voltage	V_{OL}	V_{CC} = 4.5V, I_{OUT} = 10 μA			0.4		0.4		0.4		V
Propagation Delay	t_{pd1}	V_{CC} = 10V, C_L = 50 pF			60						ns
	t_{pd0}	V_{CC} = 10V, C_L = 50 pF			60						ns

Figure 2. Rel Electrical Test Spec (cont.)

Index Point

The index point indicating the starting point for numbering of leads and/or mechanical orientation of the integrated circuit may be a tab, color dot, or other suitable indicator.

Part Number

The part number shall be the manufacturer's generic part number.

Product Assurance Level

Integrated circuits shall be marked with a code indicating the product assurance level to which they have been tested and found to conform. The code shall consist of /883 followed by the letter B or C corresponding to the applicable product assurance level designation.

Formation of Lots

Microcircuits shall be assembled into inspection lots as required to meet the product assurance inspection and test requirements of this specification. An inspection sublot shall consist of microcircuits of a single type contained on a single detail specification, manufactured on the same production line(s) through final seal by the same product techniques, and to the same device design rules and package with the same material requirements, and within the same period not exceeding 6 weeks.

Inspection Lot Identification Code

Integrated circuits shall be marked by a 4-digit date code indicating the date the lot was submitted for inspection. The first 2 numbers in the code shall be the last 2 digits of the number of the year. The third and fourth numbers shall be 2 digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right, the code number shall designate year, year, week, week.

Manufacturer's Identification

Integrated circuits shall be marked with the name, logo, or trademark of the manufacturer.

CONDITIONS AND METHODS OF TEST

Conditions and methods of test shall be in accordance with Method 5004 of MIL-STD-883 and as specified herein on a 100% basis. The general requirements of MIL-STD-883 apply as applicable. This section establishes the stress screening tests and quality conformance inspection tests for this program. The purpose of these tests is to assure the quality and reliability of the product to a particular process level commensurate with the product's intended application.

Internal Visual Inspection (Precap)

Internal visual inspection shall be performed per MIL-STD-883, Method 2010, Condition B. Hybrid internal visual shall be performed per Method 2017.

Stabilization Bake

Stabilization bake shall be performed per MIL-STD-883, Method 1008, Condition C. The devices shall be stored for 24 hours minimum at 150°C minimum. No end point measurements shall be performed.

Temperature Cycling

Temperature cycling shall be performed per MIL-STD-883, Method 1010, Condition C, 10 cycles, from −65°C to +150°C.

Constant Acceleration

Constant acceleration shall be performed per MIL-STD-883, Method 2001, Condition E, at 30,000 G's, in Y1 plane only.

Hermeticity

Hermeticity tests shall be performed per the following to determine the seal integrity of the package.

Fine Leak Testing: Fine leak testing shall be performed per MIL-STD-883, Method 1014, Condition B. The criterion for rejection will be in accorance with MIL-STD-883.

Gross Leak Testing: Gross leak testing shall be performed per MIL-STD-883, Method 1014, Condition C. The rejection criterion will be per MIL-STD-883.

Interim Electrical Parameters

Interim electrical parameters shall be the 25°C DC parameters, specified in the detail specification (RETS). (Interim electrical parameters are performed at the manufacturer's option.)

Burn-In

Burn-in shall be performed per MIL-STD-883, Method 1015, Conditions A, B, C or D on all Class B devices. (Burn-in condition varies with product type.)

The ambient temperature shall be 125°C.

Final Electrical Parameters

Final electrical parameters shall be as specified in the applicable detail specification (RETS). DC testing shall be performed at 25°C, −55°C, 125°C. AC testing shall be performed at 25°C. The PDA (Percent Defective Allowable) shall be 10% maximum and shall only apply to DC measurements at 25°C.

External Visual Inspection

All National Semiconductor products regardless of class shall receive external visual inspection per MIL-STD-883, Method 2009.

QUALITY ASSURANCE PROVISIONS

Quality Conformance Inspection

Quality conformance inspection shall be in accordance with tables I, II, III and IV. Inspection lot sampling shall be in accordance with Method 5005 of MIL-STD-883. Inspection lots failing to meet quality conformance inspection for a given product assurance level shall be rejected.

Group A Inspection

Group A inspection shall consist of the electrical parameters in the RETS (Rel Electrical Test Spec). If an inspection lot is made up of a collection of sublots, each sublot shall be subjected to Group A, as specified (see table I).

Group B Inspection

Group B inspection consists of construction testing. This sample test sequence includes physical dimensions, resistance to solvents, internal visual and mechanical, bond strength and solderability (see table II). The Group B qualifies the inspection sublot the sample is pulled from. It also qualifies all generically similar devices if the date code is within 6 weeks of the sample date code.

Group C Inspection

Group C inspection consists of die stress testing. This sample test sequence includes operating life, temperature cycling, constant acceleration, hermeticity, visual examination and end point electricals (see table III). A Group C qualifies the lot the sample is pulled from and all generically similar die types for a period of 90 days.

Group D Inspection

Group D testing further stresses the package and the die. The Group D tests include physical dimensions, lead integrity, hermeticity, thermal shock, temperature cycling, moisture resistance, mechanical shock, vibration variable frequency, constant acceleration, salt atmosphere, visual examination, and end point electricals (see table IV). A Group D qualifies the lot the sample is pulled from and all devices built in the same package for a period of 6 months.

Table I. Group A Electrical Test

Subgroups	Class B LTPD	Class C LTPD
Subgroup 1 Static tests at 25°C	5	5
Subgroup 2 Static tests at maximum rated operating temperature	7	10
Subgroup 3 Static tests at minimum rated operating temperature	7	10
Subgroup 4 Dynamic tests at 25°C	5	5
Subgroup 5 Dynamic tests at maximum rated operating temperature	7	10
Subgroup 6 Dynamic tests at minimum rated operating temperature	7	10
Subgroup 7 Functional tests at 25°C	5	5
Subgroup 8 Functional tests at maximum and minimum rated operating temperature	10	15
Subgroup 9 Switching tests at 25°C	7	10

Table II. Group B Inspection

Test	Method	Conditions	NSC Class B and C
Subgroup 1			
Physical dimension	2016		2 devices (no failures)
Subgroup 2			
a) Resistance to solvents	2015		3 devices (no failures)
b) Visual and mechanical	2014	Failure criteria from design & construction requirements of applicable procurement document	1 device (no failures)
c) Bond strength	2011	Test condition C or D	15 bonds (10 units min, no failures)
Subgroup 3			
Solderability	2003	Soldering temperature of 260 ± 10°C	15 leads (3 units min, no failures)

Table III. Group C Inspection

Test	Method	Conditions	NSC Class B and C LTPD
Subgroup 1			
Operating life test	1005	Test conditions to be specified 1000 hours	5
Subgroup 2			
Temperature cycling	1010	Test condition C	15
Constant acceleration	2001	Test condition E, Y1 axis followed by X or Z	
Seal Fine Gross	1014	As applicable	
Visual examination	1010		
End point electrical parameters		As specified in applicable device specification	

Table IV. Group D Inspection

Test	Method	Conditions	NSC Class B and C LTPD
Subgroup 1			
Physical dimensions	2016		15
Subgroup 2			
Lead Integrity	2004	Test conditions B2 (lead fatigue)	15
Seal Fine Gross	1014	As applicable	
Subgroup 3			
Thermal shock	1011	Test condition B – 15 cycles	15
Temperature cycling	1010	Test condition C – 100 cycles	
Moisture resistance	1004		
Seal Fine Gross	1014	As applicable	
Visual examination	1010		
End point electrical parameters		As specified in the applicable device specification	
Subgroup 4			
Mechanical shock	2002	Test condition B	15
Vibration variable freq.	2007	Test condition A	
Constant acceleration	2001	Test condition E	
Seal Fine Gross	1014	As applicable	
Visual examination	2007		
End point electrical parameters		As specified in the applicable device specification	
Subgroup 5			
Salt atmosphere	1009	Test condition A	15
Visual examination	1009	Paragraph 3.3.1 of Method 1009	

883 Process Flow

Test	MIL-STD-883 Method	CMOS
Internal visual	2010, Cond. B	100%
Bake	1008, Cond. C	100%
Temperature cycling	1010, Cond. C	100%
Constant acceleration	2001, Cond. E	100%
Fine leak	1014, Cond. B	100%
Gross leak	1014, Cond. C	100%
Burn-in	1015, Cond. A, B, C or D	100%
Electrical test	Per the applicable detail specification	100% RETS
Group A		LTPD Sample (RETS)
External visual	2009	100%

DATA

Certificate of Conformance

All 883/RETS material shipped shall be accompanied by a Certificate of Conformance as shown on the opposite page.

Attributes Data

Attributes data for 100% screening will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

Quality Conformance Data

Quality conformance data will not normally be provided, but shall be retained on file. Copies are available at nominal cost.

National Semiconductor Corporation

883/RETS* PROGRAM CERTIFICATE OF CONFORMANCE

TEST	MIL-STD-883 METHOD**	REQUIREMENT
INTERNAL VISUAL	2010B	100%
STABILIZATION BAKE	1008 C 24 HRS @ +150°C	100%
TEMPERATURE CYCLING	1010 C 10 CYCLES -65°C/+150°C	100%
CONSTANT ACCELERATION	2001 E	100%
FINE LEAK	1014 B 5×10^{-8}	100%
GROSS LEAK	1014 C2	100%
BURN-IN	1015 160 HRS @ +125°C	100%
FINAL ELECTRICAL PDA	+25°C DC PER NSC RETS 10% MAX ALLOWABLE	100%
	+125°C DC PER NSC RETS	100%
	-55°C DC PER NSC RETS	100%
	+25°C AC PER NSC RETS	100%
QA ACCEPTANCE	LTPD SAMPLE	
EXTERNAL VISUAL	2009	100%

* RETS = REL ELECTRICAL TEST SPECIFICATION
** All METHODS TO CURRENT REVISION LEVELS

THIS IS TO CERTIFY THAT ALL 883/RETS MATERIALS SUPPLIED TO YOUR PURCHASE ORDER COMPLY WITH ALL THE REQUIREMENTS, SPECIFICATIONS, AND DOCUMENTS PERTINENT TO THE NATIONAL 883/RETS PROGRAM. ALL TEST DATA AND CERTIFICATION IS ON FILE AT OUR FACILITY.

Part Number_____
P.O. Number_____
Date Code(s)_____
Lot Code(s)_____

_____
QUALITY ASSURANCE REPRESENTATIVE

Figure 3. Certificate of Conformance

CMOS MIL-M-38510 High Reliability Circuits

National Semiconductor Corporation is totally committed to the MIL-M-38510 Program.

The Joint Army Navy (JAN) program is designed to standardize microcircuits while increasing their inherent quality and reliability.

The MIL-M-38510 Program is totally controlled by the Defense Electronics Supply Center (DESC) of Dayton, Ohio. DESC controls the certification, qualification and quality conformance of all microcircuit manufacturers participating in the JAN MIL-38510 Program. DESC also issues the detailed specifications (slash sheets) that specify the test requirements for each device.

Defense Contract Administration Service Regions (DCASR) acts as an agent for DESC and performs on-site quality conformance surveillance at all microcircuit manufacturers' facilities.

The maintenance of the MIL-M-38510 Program is an ongoing process. Once a manufacturer is qualified, he must continue to perform quality conformance testing and submit quality conformance reports approved by DCASR to DESC.

Screening Procedures (MIL-M-38510 tested to MIL-STD-883)

The screening requirements for MIL-M-38510 are detailed in MIL-STD-883, Method 5004. They are designed to achieve the maximum quality and reliability commensurate with the application requirements. The three levels of quality are as follows:

Class S: Manned and unmanned space programs where repair or replacement is difficult or impossible and reliability is imperative.

Class B: Avionics or space satellite programs where repair or replacement is difficult or impossible and reliability is vital.

Class C: Complexed ground support equipment programs where repair or replacement is readily accomplished and down time is *not* critical.

MIL-M-38510 JAN-Qualified Products

National Semiconductor Corporation provides the flexibility to produce integrated circuits to the full specifications of MIL-M-38510 and to three levels of processing which meet the screening requirement of MIL-STD-883:

A. Product can be supplied to 883, S, B, or C.

B. JAN qualified parts provide:
   1. Full JAN marking.
   2. Manufacturing in a Government approved facility.
   3. Inventories will be maintained in factory warehouse and distributors' stock.

Table 1. MIL-M-38510 Circuit Availability

(Contact NS Representative for new circuit availability.)

National Part Type	MIL-M-38510 Specification
MM4611	MIL-M-38510/05001
MM4612	/05002
MM4623	/05003
MM4613	MIL-M-38510/05101
MM4627	/05102
MM4601	MIL-M-38510/05202
MM4602	/05203
MM4625	/05204
MM4607	MIL-M-38510/05301
MM4619	/05302
MM4630	/05303
MM4609	MIL-M-38510/05501
MM4610	/05502
MM4649	/05503
MM4650	/05504
MM4617	MIL-M-38510/05601
MM4618	/05602
MM4620	/05603
MM4622	/05604
MM4624	/05605
MM4606	MIL-M-38510/05701
MM4614	/05702
MM4615	/05703
MM4621	/05704
MM4631	/05705

Additional products will be added to this list in the future. Please contact our local representative for an updated list.

Table 2. MIL-M-38510 Screening Requirements

Screen	Class S		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
Internal visual	2010, test condition A	100%	2010, test condition B	100%	2010, test condition B	100%
Stabilization bake no end point measurements ments required	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%	1008 24 hrs, min, test condition C min	100%
Temperature cycling	1010, test condition C	100%	1010, test condition C	100%	1010, test condition C	100%
Constant acceleration	2001, test condition E (min), Y_1 orientation only	100%	2001, test condition E (min), Y_1 orientation only	100%	2001, test condition E (min), Y_1 orientation only	100%
Visual inspection		100%		100%		100%
Seal (a) Fine (b) Gross	1014	100%	1014	100%	1014	100%
Particle impact noise detection (PIND)	2020, test condition A or B	100%		—		—
Serialization		100%		—		—
Interim (pre-burn-in) electrical parameters	Per applicable device specification	100%	Per applicable device specification	100%		—
Burn-in test	1015, 240 hrs @ 125°C min	100%	1015, 160 hrs @ 125°C min	100%		—
Interim (post-burn-in) electrical parameters	Per applicable device specification	100%		—		—
Reverse bias burn-in	1015, test condition A or C, 72 hrs @ 150°C min	100%		—		—
Interim (post-burn-in) electrical parameters	Per applicable device specification	100%	Per applicable device specification	100%		—
Seal (a) Fine (b) Gross	1014	100%		—		—

Table 2. MIL-M-38510 Screening Requirements (cont.)

Screen	Class S		Class B		Class C	
	Method	Reqmt	Method	Reqmt	Method	Reqmt
Final electrical test (a) Static tests (1) 25°C (subgroup 1, table I, 5005) (2) Maximum and minimum rated operating temp (subgroups 2, 3, table I, 5005) (b) Dynamic tests and switching tests, 25°C (subgroups 4 and 9, table I, 5005) (c) Functional test, 25°C (subgroup 7, table I, 5005)	Per applicable device specification	100%	Per applicable device specification	100%	Per applicable device specification	100%
Radiographic	2012, two views	100%		—		—
Qualification or quality conformance inspection test sample selection	5005	Per applicable DOC	5005	Per applicable DOC	5005	Per applicable DOC
External visual	2009	100%	2009	100%	2009	100%

Table 3. MM54CXXX Availability to MIL-M-38510 Processing

NS Part Type	DC and AC Electricals		
	−55°C	25°C	125°C
MM54C00	Yes	Yes	Yes
MM54C02	Yes	Yes	Yes
MM54C04	Yes	Yes	Yes
MM54C08	Yes	Yes	Yes
MM54C10	Yes	Yes	Yes
MM54C20	Yes	Yes	Yes
MM54C32	Yes	Yes	Yes
MM54C42	Yes	Yes	Yes
MM54C74	Yes	Yes	Yes
MM54C76	Yes	Yes	Yes
MM54C85	Yes	Yes	Yes
MM54C86	Yes	Yes	Yes
MM54C107	Yes	Yes	Yes
MM54C151	Yes	Yes	Yes
MM54C157	Yes	Yes	Yes
MM54C161	Yes	Yes	Yes
MM54C164	Yes	Yes	Yes
MM54C165	Yes	Yes	Yes
MM54C173	Yes	Yes	Yes
MM54C174	Yes	Yes	Yes
MM54C175	Yes	Yes	Yes
MM54C193	Yes	Yes	Yes
MM54C195	Yes	Yes	Yes

MIL-M-38510 JAN Processed Products

A. Product can be supplied to 883, S, B, or C.

B. JAN processed parts provide:
1. Product will be screened to the full MIL-M-38510 electricals.
2. Devices will be manufactured using design and processing guidelines contained in MIL-M-38510.
3. Inventories will be maintained in factory warehouse.
4. No JAN marking.
5. Government approved facility not required.

C. MM54CXXX are available as MIL-M-38510 JAN processed. DC & AC electrical screening is comparable to MIL-M-38510 slash sheet testing to insure the same quality and reliability standards as specified for 38510 devices. See table 4.

Table 4.

Parameter	Symbol	Conditions	Test #	JC54C00- BRD +25°C Min	BRD +25°C Max	BHD +125°C Min	BHD +125°C Max	BLD -55°C Min	BLD -55°C Max	Drift Limits +25°C	Units
The following parameters are measured directly:			See Note								
Input Clamping Voltage	$V_{IC}+$	V_{CC} = 0V, GND = OPEN, I_{IN} = 1 mA (other inputs grounded)	6-15		1.5		1.5		1.5		V
	$V_{IC}-$	V_{CC} = 5V, I_{IN} = -1 mA (other inputs grounded)	16-25		-6.0		-6.0		-6.0		V
Power Supply Current	I_{SS}	V_{CC} = 15V, V_{IL} = 0V (all inputs)	46, 47		-25		-750		-25		
		V_{CC} = 15V, V_{IH} = 15V (all inputs)	50		-25		-750		-25		nA
Logical "1" Output Voltage	V_{OH1}	V_{CC} = 5V, I_{OUT} = -10μA, V_{IN} = 1.5V (one input per gate, other at 3.5V)	51-54	4.5		4.5		4.5		±0.08	V
	V_{OH2}	V_{CC} = 15V, I_{OUT} = -10μA, V_{IN} = 2.5V (one input per gate, other at 12.5V)	55-60	13.5		13.5		13.5			V
	V_{OH3}	V_{CC} = 4.5V, I_{OUT} = -10μA, V_{IN} = 0.8V (one input per gate, other at 3.0V)	71-74	4.4		4.4		4.4			V
	V_{OH4}	V_{CC} = 4.5V, I_{OUT} = -360μA, V_{IN} = 1V (one input per gate, other at 4V)	101-104	2.4		2.4		2.4			V
Logical "0" Output Voltage	V_{OL1}	V_{CC} = 5V, I_{OUT} = 10μA, V_{IN} = 3.5V (both inputs)	61-64		0.5		0.5		0.5	±0.04	V
	V_{OL2}	V_{CC} = 15V, I_{OUT} = 10μA, V_{IN} = 12.5V (both inputs)	65-70		1.5		1.5		1.5		V
	V_{OL3}	V_{CC} = 4.5V, I_{OUT} = 10μA, V_{IN} = 3.0V (both inputs)	75-100		0.4		0.4		0.4		V
	V_{OL4}	V_{CC} = 4.5V, I_{OUT} = 360μA, V_{IN} = 40V (both inputs)	105-110		0.4		0.4		0.4		V
Low Level Input Current	I_{IL}	V_{CC} = 15V, V_{IN} = 0V (all inputs together)	26		8.0				-8.0		nA
		V_{CC} = 15V, V_{IN} = 0V (all inputs separately)	26-35				-45				nA
High Level Input Current	I_{IH}	V_{CC} = 15V, V_{IN} = 15V (all inputs together)	36		8.0				8.0		nA
		V_{CC} = 15V, V_{IN} = 15V (each input separately)	36-45				45				nA
Output Source Current	$I_{SOURCE1}$	V_{CC} = 5V, V_{OUT} = 0V, V_{IN} = 0V (all inputs)	111-114	-1.75		-1.2		-1.92			mA
	$I_{SOURCE2}$	V_{CC} = 10V, V_{OUT} = 0V, V_{IN} = 0V (all inputs)	121-124	-8.0		-5.6		-8.8			mA
	$I_{SOURCE3}$	V_{CC} = 4.5V, V_{OUT} = 2.4V, V_{IN} = 1V (all inputs)	131-134	-470		-360		-520			μA
Output Sink Current	I_{SINK1}	V_{CC} = 5V, V_{OUT} = 5V, V_{IN} = 5V (all inputs)	115-120	1.75		1.2					mA
	I_{SINK2}	V_{CC} = 10V, V_{OUT} = 10V, V_{IN} = 10V (all inputs)	125-130	8.0		5.6					mA
	I_{SINK3}	V_{CC} = 4.5V, V_{OUT} = 0.4V, V_{IN} = 4V (all inputs)	135-140	470		360		520			μA

Table 4. (cont.)

Parameter	Symbol	Conditions	Test #	JC54C00- BRD +25°C Min	BRD +25°C Max	BHD +125°C Min	BHD +125°C Max	BLD -55°C Min	BLD -55°C Max	Drift Limits +25°C	Units
The following parameters are measured go-no-go, but may be read and recorded at extra cost.											
				BAA		BDA		BCA			
Propagation Delay	t_{pd0}	V_{CC} = 5V, C_L = 50 pF, R_L = 200 kΩ			90		120		80		ns
	t_{pd1}	V_{CC} = 5V, C_L = 50 pF, R_L = 200 kΩ	5-34		90		120		80		ns
The following parameters are tested indirectly (go-no-go only):											
Logical "1" Input Voltage	V_{IH}	V_{CC} = 5V		3.5		3.5		3.5			V
		V_{CC} = 10V		12.5		12.5		12.5			V
		V_{CC} = 4.5V		3.0		3.0		3.0			V
Logical "0" Input Voltage	V_{IL}	V_{CC} = 5V			1.5		1.5		1.5		V
		V_{CC} = 10V			2.5		2.5		2.5		V
		V_{CC} = 4.5V			0.8		0.8		0.8		V
The following parameter is guaranteed but may be tested on a sample basis:											
Input Capacitance	C_{IN}	V_{CC} = 0V, f = 1 MHz			12						pF

Radiation Hardened High Reliability Program

I. Total Dose Performance

National Semiconductor manufactures CMOS parts which can withstand exposure to total doses of ionizing radiation in excess of 10^6 rads (Si) [see AN-000.] The primary impact of radiation on circuit performance is lowering of device threshold voltages. The N-channel device is of primary concern since excessive lowering of its threshold voltage will cause depletion mode operation with resultant increased circuit quiescent current drain and loss of functionality.

Table A outlines a plan used to assure hardness of devices built from a given wafer lot. Sample devices are assembled in accordance with sampling plan A or B, depending on whether 10^5 or 10^6 rads (Si) hardness, respectively, is required. Sample devices are tested, irradiated, and retested, and must pass the appropriate post-radiation electrical limits outlined in table B for the production lot to be qualified. The production units are capable of meeting MIL-M-38510 electrical test limits, when available, as well as MIL-STD-883 limits.

Table A. Hardness Assurance Plan

	Lot Size (Wafers)	
I. Plan A	1-11	12-22
Sample Size (Wafers)	2	3
Sample Size (Devices/Wafer)	3	3
Total Devices Irradiated	6	9
Accept Level	0/6 Rejects	0/9 Rejects
Reject Level	1/6 Rejects	1/9 Rejects
II. Plan B	No. of Wafers in Lot = N	
Sample Size (Wafers)	N	
Sample Size (Devices/Wafer)	3	
Total Devices Irradiated	3xN	
Accept Level	0/3 Rejects per Wafer	
Reject Level	⩾ 1/3 Rejects per Wafer	

III. Product Flow:

A. For 1×10^5 rad qualification:
   1. Qualify lot with Plan A
   2. If lot fails, qualify wafers individually with Plan B

B. For 1×10^6 rad qualification:
   1. Qualify wafers individually with Plan B

Table B. Post-Radiation Specification*

Parameter	Post 10^5 Rads (Si)	Post 10^6 Rads (Si)
Threshold Voltage		
$\|V_{TN}\|$	0.45V (min)	0.30V (min)
$\|V_{TP}\|$	2.50V (max)	2.80V (max)
Quiescent Current (I_{SS}), V_{DD} = 10V		
Gates	2.0μA (max)	10.0μA (max)
Flip-Flops	5.0μA (max)	20.0μA (max)
MSI	15.0μA (max)	50.0μA (max)
LSI	50.0μA (max)	100.0μA (max)
Prop Delay, V_{DD} = 10V, C_D = 50pF	⩽ 25% degradation from pre-rad spec	⩽ 45% degradation from pre-rad spec

*Gamma irradiation from a Cobalt 60 source, worst case biasing at V_{DD} = 10 volts.

In figures 1 through 6, data are presented which illustrate the variation of significant circuit parameters in the 10^5 - 10^6 rads (Si) total dose range. These data were obtained from nearly 300 samples of a group of 13 different SSI, MSI, and LSI circuits listed in table C. The parameters plotted are:

Figure	Symbol	Parameter
1	ΔV_{TN}	Difference between initial & post-radiation value of N-channel threshold voltage
2	ΔV_{TP}	Difference between initial & post-radiation value of P-channel threshold voltage
3	V_{TN}	N-channel device threshold voltage
4	V_{TP}	P-channel device threshold voltage
5	I_{SS}	Supply quiescent current
6	t_{PD}	Circuit propagation delay

Table C. Radiation Effects Data

[Graphs were obtained from the following devices which were irradiated with a Cobalt-60 source.]

SSI Devices	Function	Sample Size (at each rad level)
1. CD4001	Qual 2-Input NOR	7
2. CD4011	Quad 2-Input NAND	7
3. CD4023	Triple 3-Input NAND	7
4. CD4049	Hex Buffer	7
5. CD4050	Hex Buffer	7
MSI Devices		
1. CD4013	Dual "D" Flip-Flop	7
2. CD4014	8 Stage SR	7
3. CD4017	Decade Counter	7
4. CD4027	Dual "J-K" Flip-Flop	7
5. CD4029	Up/Down Counter	7
6. CD4053	Analog Multiplexer	7
7. CD4066	Quad Switch	7
LSI Devices		
1. MM54C200	256-Bit RAM	7

Note: 91 parts irradiated at each of three radiation levels:
1×10^5 Rads (Si)
3×10^5 Rads (Si)
1×10^6 Rads (Si)

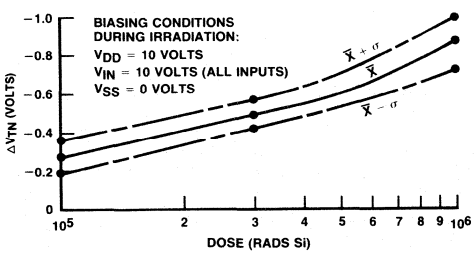


Figure 1. ΔV_{TN} vs Dose

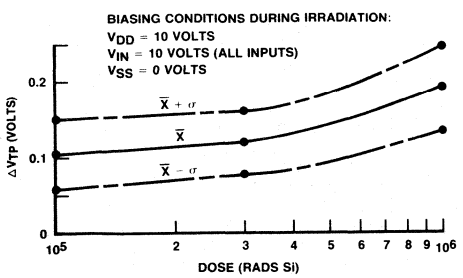


Figure 2. ΔV_{TP} vs Dose

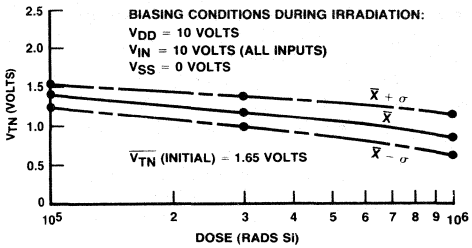


Figure 3. Final V_{TN} vs Dose

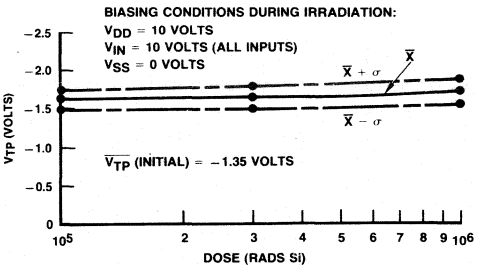


Figure 4. Final V_{TP} vs Dose

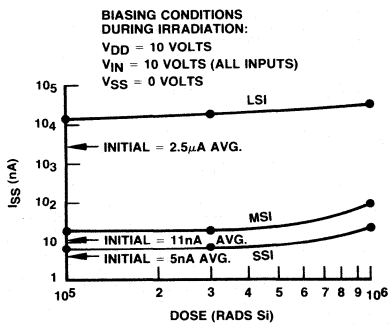


Figure 5. I_{SS} vs Dose

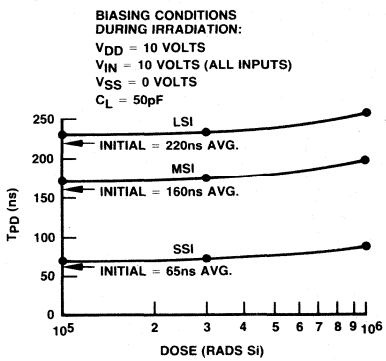


Figure 6. T_{PD} vs Dose

Table D lists those devices which have been qualified by NSC for megarad hardness along with those devices which will be qualified during 1978. A total of 68 devices appear on these lists, and any other of our commercially available metal gate CMOS parts can be quickly qualified per customer requirements.

Table D. Radiation Hardened CMOS Qualified Parts List
Devices Hard to 10^6 Rads (Si)

1.	CD4001	Quad 2-Input NOR
2.	CD4002	Dual 4-Input NOR
3.	CD4006	18-Stage S/R
4.	CD4007	Dual Pair Plus Inverter
5.	CD4008	4-Bit Adder
6.	CD4009	Hex Buffer
7.	CD4010	Hex Buffer
8.	CD4011	Quad 2-Input NAND
9.	CD4012	Dual 4-Input NAND
10.	CD4013	Dual "D" Flip-Flop
11.	CD4014	8-Stage S/R
12.	CD4015	Dual 4-Bit Register
13.	CD4016	Quad Switch
14.	CD4017	Decade Counter/Divider
15.	CD4019	Quad AND/OR Select
16.	CD4020	14-Stage Counter
17.	CD4021	8-Stage S/R
18.	CD4022	Octal Counter/Divider
19.	CD4023	Triple 3-Input NAND
20.	CD4024	7-Stage Counter/Divider
21.	CD4025	Triple 3-Input NOR
22.	CD4027	Dual "J-K" Flip-Flop
23.	CD4028	BCD-to-Decimal Decoder
24.	CD4029	Up/Down Counter
25.	CD4030	Quad Exclusive-OR
26.	CD4031	64-Stage Static Shift Register
27.	CD4040	14-Stage Counter
28.	CD4041	True/Complement Buffer
29.	CD4044	Quad 3-State NAND R/S Latch
30.	CD4049	Hex Buffer
31.	CD4050	Hex Buffer
32.	CD4051	Analog Multiplexer/Demultiplexer
33.	CD4052	Analog Multiplexer/Demultiplexer
34.	CD4053	Analog Multiplexer/Demultiplexer
35.	CD4066	Quad Switch
36.	CD4070	Quad Exclusive-OR
37.	CD4076	Quad "D" Flip-Flop
38.	CD4093	Schmitt Trigger
39.	MM54C86	Quad Exclusive-OR
40.	MM54C173	Quad "D" Flip-Flop
41.	MM54C200	256-Bit RAM
42.	MM54C901	Hex Buffers
43.	MM54C902	
44.	MM54C903	
45.	MM54C904	
46.	MM54C906	
47.	MM54C907	

Additional devices will be added in the future. Please contact our local representative for an updated list.

Future Plans
Megarad Product Available During 1978

	Device	Function
1.	CD4000	Dual 3-Input NOR Plus Inverter
2.	CD4001B	Quad 2-Input NOR
3.	CD4011B	Quad 2-Input NAND
4.	CD4018	Divide-by-N Counter
5.	CD4023B	Triple 3-Input NAND
6.	CD4025B	Triple 3-Input NOR
7.	CD4034	8-Stage Register
8.	CD4035	4-Bit S/R
9.	CD4042	Quad Latch
10.	CD4043	Quad NOR Latch
11.	CD4047	Multivibrator
12.	CD4048	8-Function Gate
13.	CD4069	Hex Inverter
14.	CD4071B	Quad 2-Input OR
15.	CD4073B	Triple 3-Input AND
16.	CD4075B	Triple 3-Input OR
17.	CD 4081B	Quad 2-Input AND
18.	CD4518	Dual Up Counter
19.	CD4520	Dual Up Counter
20.	MM54C04	Hex Inverter
21.	MM54C89	64-Bit RAM

*All of National's metal gate CMOS circuits can be radiation hardened. Quick response can be given to customer requirements for rad hard parts not appearing on the above lists.

II. Extended Total Dose Rate [to 10^7 Rads (Si)]

Recently acquired data indicate that the resistance of our CMOS product extends at least one order of magnitude above the 10^6 level already demonstrated. Figure I illustrates measured shifts from pre-irradiation values in P- and N-channel threshold voltage, ΔV_{TP} and ΔV_{TN} respectively, up to total γ dose levels of 10^7 rads (Si). Of special interest is the change in slope of the ΔV_{TN} versus dose characteristic at levels just above 10^6 rads (Si).

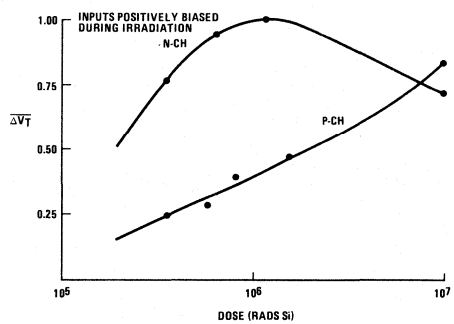


Figure 1. Normalized ΔV_T vs Dose

At this level, negative charge from the silicon substrate arrives in the gate oxide at a rate faster than radiation-created positive charge. This causes V_{TN} to return toward its initial value as dose level is increased even further while increases in $|V_{TP}|$ still remain within reasonable limits for satisfactory circuit operation.

III. Dose Rate Performance

When CMOS ICs are subjected to large bursts of ionizing radiation, hole-electron pairs are created in the silicon substrate. The resultant currents flowing through the high resistivity P- and N- substrates can cause voltage differences which may impair circuit performance in one of the following two ways.

Latch-Up: A CMOS circuit contains the structural elements required to form a four layered Schockley diode switching device as illustrated in figure 1. The emitter-base junctions of the lateral PNP and vertical NPN which comprise the Schockley diode are normally prevented from becoming forward biased by the circuit metallization. Because of this, the Schockley diode will be in the off state during normal circuit operation and will pose no threat to reliable circuit performance.

Sufficiently high values of burst radiation can cause currents to flow through substrate resistances, R_{N-} and R_{P-}, to cause forward biasing of the parasitic PNP and NPN emitter-base junctions and turn on the Schockley diode. The excessive flow of supply current which accompanies turn-on of the Schockley diode has been found to occur in the range of 10^8-10^{10} rads (Si)/sec on many CMOS circuits.

This problem can be completely eliminated by reducing to less than unity the product of the common emitter current gains of the NPN and PNP devices comprising the Schockley diode. One technique which has been successfully employed to eliminate the latch-up problem has been the use of neutron irradiation to lower minority carrier lifetime in the silicon substrate which directly affects parasitic bipolar current gains. As the values in table I indicate, neutron treatment of parts which exhibited latch-up at 3×10^8 and 3×10^9 rads (Si)/sec resulted in latch-up free operation up to the limit of the burst simulation equipment, 10^{10} rads (Si)/sec. By treating wafers with neutron fluxes on the order of 10^{14} cm^{-2}, this enhanced circuit performance is obtained without sacrificing parametric performance. This is illustrated in figures 2 and 3, which plot supply current drain and propagation delay, respectively, versus neutron flux and show no significant degradation at the 10^{14} cm^{-2} level.

Table I. Latch-Up Performance

Device	Dose Required for Latch-Up		Units
	Control	Neutron Treated*	
CD4011	3.1×10^9	$>9.4\times10^9$	Rads (Si)/sec
CD4053	3.2×10^8	$>9.4\times10^9$	Rads (Si)/sec
MM54C200	$>2.2\times10^{10}$	$>8.8\times10^{11}$	Rads (Si)/sec

*Neutron treated parts were subjected to a neutron flux of 1×10^{14} neutrons (fast)/cm^2.

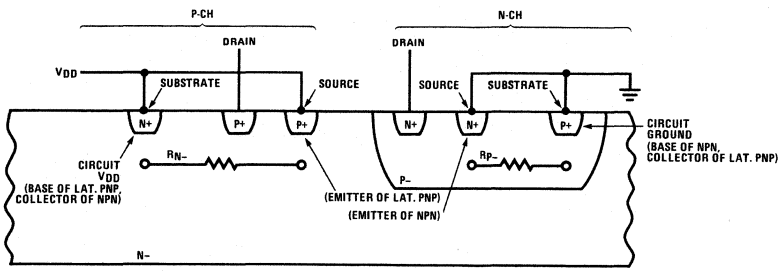


Figure 1. Cross Section of CMOS Circuit Elements Which May Lead to Latch-Up or Data Upset During Ionizing Radiation Bursts

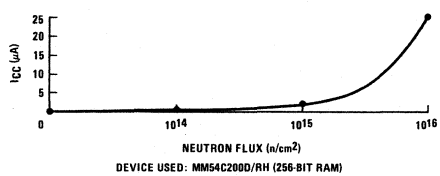


Figure 2. Device Leakage vs Neutron Flux

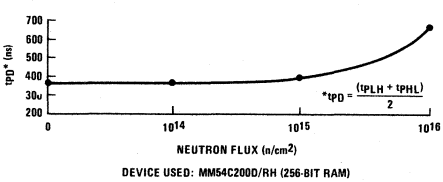


Figure 3. Propagation Delay vs Neutron Flux

Another method which may be used to reduce minority carrier lifetime and achieve latch-up free operation is the use of gold doping in the wafer fabrication process. This approach is presently being investigated in the National Semiconductor development laboratory.

Data-Upset: This effect results in the loss of stored data in a circuit after being subjected to burst radiation. It is typically of most concern in circuits such as memories and shift registers, where stored data bits are not directly coupled to circuit inputs. The problem is apparently caused during ionizing burst radiation exposure when one or more of the circuit's parasitic bipolar devices becomes turned on and causes asymmetric current flows in the data storage circuit, leading to a reversal of the stored data state.

Table II shows the effect of neutron treatment of a MM54C200D/RH 256-bit static RAM on the dose rate at which upset occurs. The effect of gain degradation of parasitic devices on data upset is not nearly as dramatic as it is in the case of latch-up. Although neutron fluxes in excess of 10^{15} cm^{-2} cause significant alterations in semiconductor material properties and circuit electrical parameters, figures 2 and 3 indicate that the circuits tested would still meet data sheet requirements after irradiation in excess of 2×10^{15} cm^{-2}. At this level the tolerance to data upset exhibits about a threefold improvement over untreated devices. Almost an entire order of magnitude improvement in data upset tolerance can be obtained with treatment at 10^{16} cm^{-2} if the user can tolerate the degraded propagation delay and increased supply current drain occurring at this level.

Table II. Data Upset Performance

Neutron Flux (n-fast/cm^2)	Dose Rate Needed to Induce Data Upset (MM54C200D memory enabled)
0 (control)	1.76×10^8 Rads (Si)/sec
1×10^{14}	2.00×10^8 Rads (Si)/sec
1×10^{15}	5.00×10^8 Rads (Si)/sec
1×10^{16}	1.17×10^9 Rads (Si)/sec

IV. Reliability

1. Device Types: CD4001AD/RH (Lot nos. 1, 2, 3)
   CD4001AD/RH (Lot no. 4)
   MM54C200D/RH (Lot no. 5)
2. Package: Dual-In-Line ceramic
3. HTOPL Conditions: V_{BIAS} = 12.0V/15.0V
   Temp = 125°C
4. Results:

Lot	Sample Size	V_{DD}	Rejects at 168 Hr	336 Hr	504 Hr	1008 Hr	2016 Hr
1*	115	+15V	0	0	0	0	0
2	119	+12V	0	0	0	0	0
3	112	+12V	0	0	0	0	0
4	90	+12V	0	0	0	0	0
5*	40	+12V	0	0	0	0	0
Total:	476		0	0	0	0	0

*These lots included a pre burn-in for 168 hrs.

Total Device-Hours = 804,384
Failure Rate: 0.11%/1000 hrs with 60% confidence level.

A+ PROGRAM

A+ Program: A comprehensive program that utilizes National's experience gained from participation in the many Military/Aerospace programs.

A program that not only assures high quality but also increases the reliability of molded integrated circuits.

The A+ program is intended for users who cannot perform incoming inspection of ICs or does not wish to do so, yet needs significantly better than usual incoming quality and higher reliability levels for his standard integrated circuit.

Users who specify A+ processed parts will find that the program:

- Eliminates incoming electrical inspection.
- Eliminates the need for, and thus the added cost of, independent testing laboratories.
- Reduces the cost of reworking assembly boards.
- Reduces field failures.
- Reduces equipment down time.
- Reduces the need for excess inventories due to yield loss incurred as a result of processing performed at independent testing laboratories.

The A+ Program Saves You Money

It is widely accepted fact that down-time of equipment is costly not only in lost hours of machine usage but also costly in the repair and maintenance cycle. One of the added advantages of the A+ program is the burn-in screen, which is one of the most effective screening procedures in the semiconductor industry. Failure rates as a result of the burn-in can be decreased many times. The objective of burn-in is to stress the device much higher than it would be stressed during normal usage.

Reliability vs. Quality

The words "reliability" and "quality" are often used interchangeably, as though they connoted identical facets of a product's merit. But reliability and quality are different, and IC users must understand the essential difference between the two concepts in order to evaluate properly the various vendors' programs for products improvement that are generally available, and National's A+ program in particular.

The concept of quality gives us information about the population and faulty IC devices among good devices, and generally relates to the number of faulty devices that arrive at a user's plant. But looked at in another way, quality can instead relate to the number of faulty ICs that escape detection at the IC vendor's plant.

It is the function of a vendor's Quality Control arm to monitor the degree of success of that vendor in reducing the number of faulty ICs that escape detection. Quality Control does this by testing the outgoing parts on a sampled basis. The Acceptable Quality Level (AQL) in turn determines the stringency of the sampling. As the AQL decreases it becomes more difficult for defective parts to escape detection, thus the quality of the shipped parts increases.

The concept of reliability, on the other hand, refers to how well a part that is initially good will withstand its environment. Reliability is measured by the percentage of parts that fail in a given period of time.

Thus the difference between quality and reliability means the ICs of high quality may, in fact, be of low reliability, while those of low quality may be of high reliability.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate marginal, short-life parts.

In any test of reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time of failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in fact demonstrate a higher reliability in use.

National's A+ Program

National has combined the successful B+ program with the Military/Aerospace processing specifications and provides the A+ program as the best practical approach to maximum quality and reliability on molded devices. The following flow chart shows how we do it step by step.

SEM
Randomly selected wafers are taken from production regularly and subjected to SEM analysis.

Epoxy B Seal
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections and QC monitoring are designed to provide highly reliable products. (A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National, and reliability data that proves its success.)

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and

helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (0°C to 100°C)
Exercising the circuits over 100°C temperature range further stresses the bonds and generally eliminates any marginal bonds missed during the bake.

Electrical Testing
Every device will be tested at 25°C for functional and DC parameters.

Burn-in Test
Devices are stressed at maximum operating conditions to eliminate marginal devices. Test is performed per Mil-Std-883A Method 1015.1.

High Temperature (100°C) Functional Electrical Test
A high temperature test with voltages applied places the die under the most severe stress possible. The test is actually performed at 100°C – 30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient.

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Tighter-than-Normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.65% AQL. Some even use a looser 1% AQL. When you specify the A+ program, however, not only do we sample your parts to a 0.28% AQL for all data-sheet DC parameters, but they receive 0.14% AQL for functionality as well. Now functional failures – not parameter shifts beyond spec – cause most system failures. Thus, the five-times to seven-times tightening of the sampling procedure (from 0.65% to 0.14% AQL) gives a substantially higher quality to your A+ parts. And you can rely on the integrity of your received ICs without incoming tests at your facility.

Ship Parts

Here are the QC sampling plans used in our A+ test program:

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, DC	25°C	0.28%
Major Mechanical	25°C	0.25%
Minor Mechanical	25°C	1%

B+ PROGRAM

B+ Program: a comprehensive program that assures high quality *and* high reliability of molded integrated circuits.

The B+ program improves both the quality *and* the reliability of National's digital, linear, and CMOS Epoxy B integrated circuit products. It is intended for the manufacturing user who cannot perform incoming inspection of his ICs, or does not wish to do so, yet needs significantly-better-than-usual incoming quality and reliability levels for his standard ICs.

Integrated circuit users who specify B+ processed parts will find that the program:

- Eliminates incoming electrical inspection
- Eliminates the need for, and thus the costs of, independent testing laboratories
- Reduces the cost of reworking assembled boards
- Reduces field failures
- Reduces equipment downtime

Reliability Saves You Money

With the increased population of integrated circuits in modern electronic systems has come an increased concern with IC failures in such systems.

And rightly so, for at least two reasons.

First of all, the effect of component reliability on system reliability can be quite dramatic. For example, suppose that you, as a system manufacturer, were to choose an IC that is 99 percent reliable. You would find that if your system used only 70 such ICs, the overall reliability of the system's IC portion would be only 50 percent. In other words, only one out of two of your systems would operate. The result? A system very costly to produce and probably very difficult to sell.

Secondly, whether the system is large or small you cannot afford to be hounded by the spectre of unnecessary maintenance costs. Not only because labor, repair and rework costs have risen — and promise to continue to rise — but also because field replacement may be prohibitively expensive. If you ship a system that contains a marginally-performing IC, an IC that later fails in the field, the cost of replacement may be — literally — hundreds of times more than the cost of the failed IC itself.

Improving the Reliability of Shipped Parts

The most important factor that affects a part's reliability is its construction: the materials used and the method by which they are assembled.

Now, it's true that reliability cannot be tested into a part. Still, there are tests and procedures that an IC vendor can implement, which will subject the IC to stresses in excess of those that it will endure in actual use, and which will eliminate most marginal, short-life parts.

In any test for reliability the weaker parts will normally fail first. Further, stress tests will accelerate, or shorten, the time to failure of the weak parts. Because the stress tests cause weak parts to fail prior to shipment to the user, the population of shipped parts will in facg demonstrate a higher reliability in use.

Quality Improvement

When an IC vendor specifies 100 percent final testing of his parts then, in theory, every shipped part should be a good part. However, in any population of mass-produced items there does exist some small percentage of defective parts.

One of the best ways to reduce the number of such faulty parts is, simply, to retest the parts prior to shipment. Thus, if there is a one percent change that a bad part will escape detection initially, retesting the parts reduces that probability to only 0.01 percent. (A comparable tightening of the QC group's sampled-test plan ensures the maintenance of the improved quality level.)

National's B+ Program Gets It All Together

We've stated that the B+ program improves both the quality *and* the reliability of National's molded integrated circuits, and pointed out the difference between those two concepts. Now, how do we bring them together? The answer is in the B+ program processing, which is a continuum of stress and double testing. With the exception of the final QC inspection, which is sampled, all steps of the B+ process are performed on 100 percent of the program parts. The following flow chart shows how we do it, step by step.

Epoxy B Processing for All Molded Parts
At National, all molded semiconductors, including ICs, have been built by this process for some time now. All processing steps, inspections and QC monitoring are designed to provide highly reliable products. [A reliability report is available that gives, in detail, the background of Epoxy B, the reason for its selection at National and reliability data that proves its success.]

Six Hour, 150°C Bake
This stress places the die bond and all wire bonds into a combined tensile and shear stress mode, and helps eliminate marginal bonds and electrical connections.

Five Temperature Cycles (0°C to 100°C)
Exercising the circuits over a 100°C temperature range further stresses the bonds and generally eliminates any marginal bonds missed during the bake.

High Temperature (100°C) Functional Electrical Test
A high-temperature test such as this with voltages

applied places the die under the most severe stress possible. The test is actually performed at 100°C – 30°C higher than the commercial ambient limit. All devices are thoroughly exercised at the 100°C ambient. [Even though Epoxy B processing has virtually eliminated thermal intermittents, we perform this test to ensure againnt even the remote possibility of such a problem. Remember, the emphasis in the B+ program is on the elimination of those marginally-performing devices that would otherwise lower field reliability of the parts.]

DC Functional and Parametric Tests
These room-temperature functional and parametric tests are the normal, final tests through which all National products pass.

Tighter-than-Normal QC Inspection Plans
Most vendors sample inspect outgoing parts to a 0.65% AQL. Some use even a looser 1% AQL. When you specify the B+ program, however, not only do we sample your parts to a 0.28% AQL for all data-sheet DC parameters, but they receive a 0.14% AQL for functionality as well. Now, functional failures – not parameter shifts beyond spec – cause most system failures. Thus, the five-times to seven-times tightening of the sampling procedure (from 0.65 - 1% to 14% AQL) gives a substantially higher quality to your B+ parts. And you can rely on the integrity of your received ICs without incoming tests at your facility.

Ship Parts

Here are the QC sampling plans used in our B+ test program:

TEST	TEMPERATURE	AQL
Electrical Functionality	25°C	0.14%
Parametric, DC	25°C	0.25%
Parametric, DC	100°C	1%
Parametric, AC	25°C	1%
Major Mechanical	–	0.25%
Minor Mechanical	–	1%

Application Notes/Briefs

CMOS, the Ideal Logic Family

National Semiconductor
Application Note 77
Stephen Calebotta

INTRODUCTION

Let's talk about the characteristics of an ideal logic family. It should dissipate no power, have zero propagation delay, controlled rise and fall times, and have noise immunity equal to 50% of the logic swing.

Well, that ideal logic family is here – almost. The properties of CMOS (complementary MOS) begin to approach these ideal characteristics.

First, CMOS dissipates low power. Typically, the static power dissipation is 10 nW per gate which is due to the flow of leakage currents. The active power depends on power supply voltage, frequency, output load and input rise time, but typically, gate dissipation at 1MHz with a 50 pF load is less than 10mW.

Second, the propagation delays through CMOS are short, though not quite zero. Depending on power supply voltage, the delay through a typical gate is on the order of 25 to 50 ns.

Third, rise and fall times are controlled, tending to be ramps rather than step functions. Typically, rise and fall times tend to be 20 to 40% longer than the propagation delays.

Last, but not least, the noise immunity approaches 50%, being typically 45% of the full logic swing.

Besides the fact that it approaches the characteristics of an ideal logic family and besides the obvious low power battery applications, why should designers choose CMOS for new systems? The answer is cost.

On a component basis, CMOS is still more expensive than TTL. However, system level cost may be lower. The power supplies in a CMOS system will be cheaper since they can be made smaller and with less regulation. Because of lower currents, the power supply distribution system can be simpler and therefore, cheaper. Fans and other cooling equipment are not needed due to the lower dissipation. Because of longer rise and fall times, the transmission of digital signals becomes simpler making transmission techniques less expensive. Finally, there is no technical reason why CMOS prices cannot approach present day TTL prices as sales volume and manufacturing experience increase. So, an engineer about to start a new design should compare the system level cost of using CMOS or some other logic family. He may find that, even at today's prices, CMOS is the most economical choice.

National is building two lines of CMOS. The first is a number of parts of the CD4000A series. The second is the 54C/74C series which National introduced and which will become the industry standard in the near future.

The 54C/74C line consists of CMOS parts which are pin and functional equivalents of many of the most popular parts in the 7400 TTL series. This line is typically 50% faster than the 4000A series and sinks 50% more current. For ease of design, it is spec'd at TTL levels as well as CMOS levels, and there are two temperature ranges available: 54C, −55°C to +125°C or 74C, −40°C to +85°C. Table 1 compares the port parameters of the 54C/74C CMOS line to those of the 54L/74L low power TTL line.

TABLE 1. Comparison of 54L/74L Low Power TTL and 54C/74C CMOS Port Parameters.

FAMILY	V_{CC}	V_{IL} MAX	I_{IL} MAX	V_{IH} MIN	I_{IH} 2.4V	V_{OL} MAX	I_{OL}	V_{OH} MIN	I_{OH}	t_{pd0} TYP	t_{pd1} TYP	P_{DISS}/GATE STATIC	P_{DISS}/GATE 1 MHz, 50 pF LOAD
54L/74L	5	0.7	0.18 mA	2.0	10 μA	0.3	2.0 mA	2.4	100μA	31	35	1 mW	2.25 mW
54C/74C	5	0.8	–	3.5	–	0.4	*360μA	2.4	*100μA	60	45	0.00001 mW	1.25 mW
54C/74C	10	2.0	–	8.0	–	1.0	**10μA	9.0	**10μA	25	30	0.00003 mW	5 mW

*Assumes interfacing to low power TTL.

**Assumes interfacing to CMOS.

CHARACTERISTICS OF CMOS

The aim of this section is to give the system designer not familiar with CMOS, a good feel for how it works and how it behaves in a system. Much has been written about MOS devices in general. Therefore, we will not discuss the design and fabrication of CMOS transistors and circuits.

The basic CMOS circuit is the inverter shown in Figure 2-1. It consists of two MOS enhancement mode transistors, the upper a P-channel type, the lower an N-channel type.

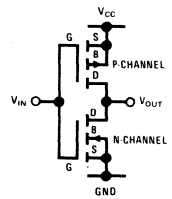


FIGURE 2-1. Basic CMOS Inverter.

The power supplies for CMOS are called V_{DD} and V_{SS}, or V_{CC} and Ground depending on the manufacturer. V_{DD} and V_{SS} are carryovers from conventional MOS circuits and stand for the drain and source supplies. These do not apply directly to CMOS since both supplies are really source supplies. V_{CC} and Ground are carryovers from TTL logic and that nomeclature has been retained with the introduction of the 54C/74C line of CMOS. V_{CC} and Ground is the nomenclature we shall use throughout this paper.

The logic levels in a CMOS system are V_{CC} (logic "1") and Ground (logic "0"). Since "on" MOS transistor has virtually no voltage drop across it if there is no current flowing through it, and since the input impedance to CMOS device is so high (the input characteristic of an MOS transistor is essentially capacitive, looking like a $10^{12}\Omega$ resistor shunted by a 5 pF capacitor), the logic levels seen in a CMOS system will be essentially equal to the power supplies.

Now let's look at the characteristic curves of MOS transistors to get an idea of how rise and fall times, propagation delays and power dissipation will vary with power supply voltage and capacitive loading. Figure 2-2 shows the characteristic curves of N-channel and P-channel enhancement mode transistors.

There are a number of important observations to be made from these curves. Refer to the curve of V_{GS} = 15V (Gate to Source Voltage) for the N-channel transistor. Note that for a constant drive voltage V_{GS}, the transistor behaves like a current source for V_{DS}'s (Drain to Source Voltage) greater than $V_{GS} - V_T$ (V_T is the threshold voltage of an MOS transistor). For V_{DS}'s below $V_{GS} - V_T$, the transistor behaves essentially like a resistor. Note also that for lower V_{GS}'s, there are similar curves except that the magnitude of the I_{DS}'s are significantly smaller and that in fact, I_{DS} increases approximately as the square of increasing V_{GS}. The P-channel transistor exhibits essentially identical, but complemented, characteristics.

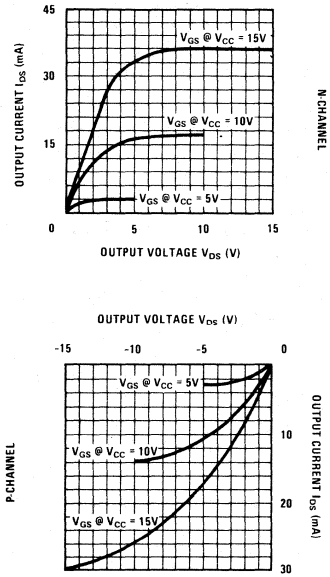


FIGURE 2-2. Logical "1" Output Voltage vs Source Current.

If we try to drive a capacitive load with these devices, we can see that the initial voltage change across the load will be ramp-like due to the current source characteristic followed by a rounding off due to the resistive characteristic dominating as V_{DS} approaches zero. Referring this to our basic CMOS inverter in Figure 2-1, as V_{DS} approaches zero, V_{OUT} will approach V_{CC} or Ground depending on whether the P-channel or N-channel transistor is conducting.

Now if we increase V_{CC} and, therefore, V_{GS} the inverter must drive the capacitor through a larger voltage swing. However, for this same voltage increase, the drive capability (I_{DS}) has increased roughly as the square of V_{GS} and, therefore, the rise times and the propagation delays through the inverter as measured in Figure 2-3 have decreased.

So, we can see that for a given design, and therefore fixed capacitive load, increasing the power supply voltage will increase the speed of the system.

Increasing V_{CC} increases speed but it also increases power dissipation. This is true for two reasons. First, CV^2f power increases. This is the power dissipated in a CMOS circuit, or any other circuit for that matter, when driving a capacitive load.

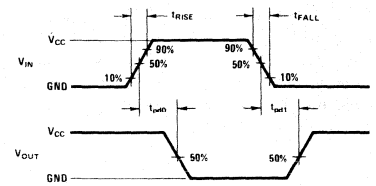


FIGURE 2-3. Rise and Fall Times and Propagation Delays as Measured in a CMOS System.

For a given capacitive load and switching frequency, power dissipation increases as the square of the voltage change across the load.

The second reason is that the VI power dissipated in the CMOS circuit increases with V_{CC} (for V_{CC}'s $> 2V_T$). Each time the circuit switches, a current momentarily flows from V_{CC} to Ground through both output transistors. Since the threshold voltages of the transistors do not change with increasing V_{CC}, the input voltage range through which the upper and lower transistors are conducting simultaneously increases as V_{CC} increases. At the same time, the higher V_{CC} provides higher V_{GS} voltages which also increase the magnitude of the I_{DS} currents. Incidently, if the rise time of the input signal was zero, there would be no current flow from V_{CC} to Ground through the circuit. This current flows because the input signal has a finite rise time and, therefore, the input voltage spends a finite amount of time passing through the region where both transistors conduct simultaneously. Obviously, input rise and fall times should be kept to a minimum to minimize VI power dissipation.

Let's look at the transfer characteristics, Figure 2-4, as they vary with V_{CC}. For the purposes of this discussion we will assume that both transistors in our basic inverter have identical but complementary characteristics and threshold voltages. Assume the threshold voltages, V_T, to be 2V. If V_{CC} is less than the threshold voltage of 2V, neither transistor can ever be turned on and the circuit cannot operate. If V_{CC} is equal to the threshold voltage exactly then we are on the curve Figure 2-4a. We appear to have 100% hysteresis. However, it is not truly hysteresis since both output transistors are off and the output voltage is being held on the gate capacitances of succeeding circuits. If V_{CC} is somewhere between one and two threshold voltages (Figure 2-4b), then we have diminishing amounts of "hysteresis" as we approach V_{CC} equal to $2V_T$ (Figure 2-4c). At V_{CC} equal to two thresholds we have no "hysteresis" and no current flow through both the upper and lower transistors during switching. As V_{CC} exceeds two thresholds the transfer curves begin to round off (Figure 2-4d). As V_{IN} passes through the region where both transistors are conducting, the currents flowing through the transistors cause voltage drops across them giving the rounded characteristic.

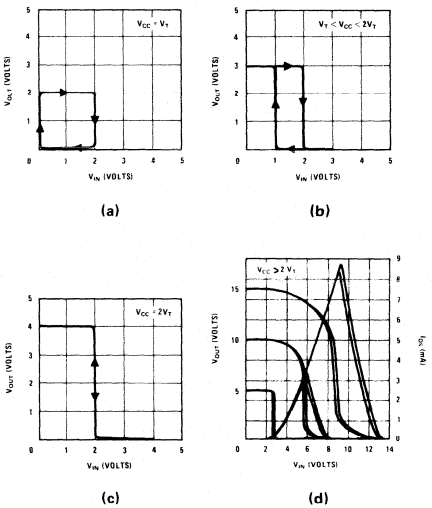


FIGURE 2-4. Transfer Characteristics vs V_{CC}.

Considering the subject of noise in a CMOS system, we must discuss at least two specs: noise immunity and noise margin.

National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 0.45 V_{CC} or less away from V_{CC} or Ground typically will not propagate through the system as an erroneous logic level. This does not mean that no signal at all will appear at the output of the first circuit. In fact, there will be an output signal as a result of the spurious input, but it will be reduced in amplitude. As this signal propagates through the system, it will be attenuated even more by each circuit it passes through until it finally disappears. Typically, it will not change any signal to the opposite logic level. In a typical flip flop, a 0.45 V_{CC} spurious pulse on the clock line would not cause the flop to change state.

National also guarantees that its CMOS circuits have a 1V DC noise margin over the full power supply range and temperature range and with any combination of inputs. This is simply a variation of the noise immunity spec only now a specific set of input and output voltages have been selected and guaranteed. Stated verbally, the spec says that for the output of a circuit to be within 0.1 V_{CC} volts of a proper logic level (V_{CC} or Ground), the input

can be as much as 0.1 V_{CC} plus 1V away from power supply rail. Shown graphically we have:

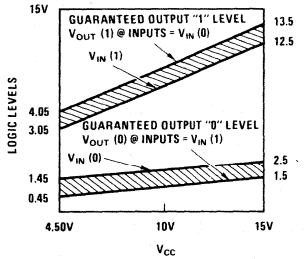


FIGURE 2-5. Guaranteed CMOS DC Margin Over Temperature as a Function of V_{CC}. CMOS Guarantees 1V.

This is similar in nature to the standard TTL noise margin spec which is 0.4V.

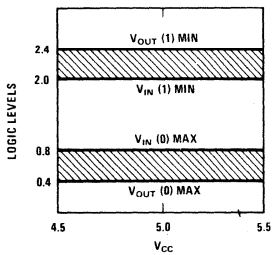


FIGURE 2-6. Guaranteed TTL DC Margin Over Temperature as a Function of V_{CC}. TTL Guarantees 0.4V.

For a complete picture of V_{OUT} vs V_{IN} refer to the transfer characteristic curves in Figure 2-4.

SYSTEM CONSIDERATIONS

This section describes how to handle many of the situations that arise in normal system design such as unused inputs, paralleling circuits for extra drive, data bussing, power considerations and interfaces to other logic families.

Unused inputs: simply stated, unused inputs should not be left open. Because of the very high impedance ($\sim 10^{12}\Omega$), a floating input may drift back and forth between a "0" and "1" creating some very intriguing system problems. All unused inputs should be tied to V_{CC}, Ground or another used input. The choice is not completely arbitrary, however, since there will be an effect on the output drive capability of the circuit in question. Take, for example, a four input NAND gate being used as a two input gate. The internal structure is shown in Figure 3-1. Let inputs A & B be the unused inputs.

If we were going to tie the unused inputs to a logic level, inputs A & B would have to be tied to V_{CC} to enable the other inputs to function. That would turn on the lower A and B transistors and turn off the upper A and B transistors. At most, only two of the upper transistors could ever be turned on. However, if inputs A and B were tied to input C, the input capacitance would triple, but each time C went low, the upper A, B and C transistors would turn on, tripling the available source current. If input D was low also, all four of the upper transistors would be on.

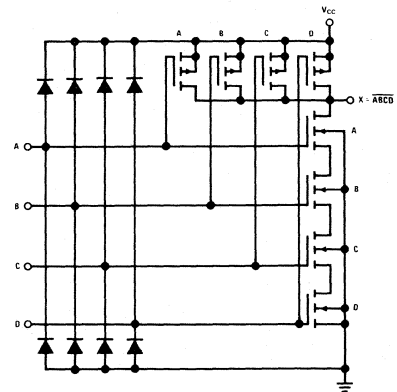


FIGURE 3-1. MM74C20 Four Input NAND Gate.

So, tying unused NAND gate inputs to V_{CC} (Ground for NOR gates) will enable them, but tying unused inputs to other used inputs guarantees an increase in source current in the case of NAND gates (sink current in the case of NOR gates). There is no increase in drive possible through the series transistors. By using this approach, a multiple input gate could be used to drive a heavy current load such as a lamp or a relay.

Parallel gates: depending on the type of gate, tying inputs together guarantees an increase in either source or sink current but not both. To guarantee an increase in both currents, a number of gates must be paralleled as in Figure 3-2. This insures that there are a number of parallel combinations of the series string of transistors (Figure 3-1), thereby increasing drive in that direction also.

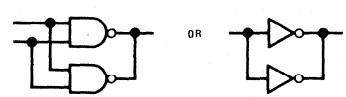


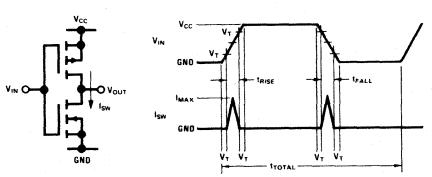
FIGURE 3-2. Paralleling Gates or Inverters Increases Output Drive in Both Directions.

Data bussing: there are essentially two ways to do this. First, connect ordinary CMOS parts to a bus using transfer gates (part no. CD4016C). Second,

and the preferred way, is to use parts specifically designed with a CMOS equivalent of a TRI-STATE® output.

Power supply filtering: since CMOS can operate over a large range of power supply voltages (3V to 15V), the filtering necessary is minimal. The minimum power supply voltage required will be determined by the maximum frequency of operation of the fastest element in the system (usually only a very small portion of any system operates at maximum frequency). The filtering should be designed to keep the power supply voltage somewhere between this minimum voltage and the maximum rated voltage the parts can tolerate. However, if power dissipation is to be kept to a minimum, the power supply voltage should be kept as low as possible while still meeting all speed requirements.

Minimizing system power dissipation: to minimize power consumption in a given system, it should be run at the minimum speed to do the job with the lowest possible power supply voltage. AC and DC transient power consumption both increase with frequency and power supply voltage. The AC power is described as CV^2f power. This is the power dissipated in a driver driving a capacitive load. Obviously, AC power consumption increases directly with frequency and as the square of the power supply. It also increases with capacitive load, but this is usually defined by the system and is not alterable. The DC power is the VI power dissipated during switching. In any CMOS device during switching, there is a momentary current path from the power supply to ground, (when $V_{CC} > 2V_T$) Figure 3-3.



VI POWER IS GIVEN BY:

$$P_{VI} = V_{CC} \times \frac{1}{2} I_{MAX} \times \text{RISE TIME TO PERIOD RATIO}$$

$$\text{RISE TIME TO PERIOD RATIO} = \frac{V_{CC} - 2V_T}{V_{CC}} \times \frac{t_{RISE} + t_{FALL}}{t_{TOTAL}}$$

$$\text{WHERE } \frac{1}{t_{TOTAL}} = \text{FREQUENCY}$$

$$P_{VI} = 1/2\,(V_{CC} - 2V_T)\, I_{CC\,MAX}\, (t_{RISE} + t_{FALL})\, \text{FREQ.}$$

FIGURE 3-3. DC Transient Power.

The maximum amplitude of the current is a rapidly increasing function of the input voltage which in turn is a direct function of the power supply voltage. See Figure 2-4d.

The actual amount of VI power dissipated by the system is determined by three things: power supply voltage, frequency and input signal rise time. A very important factor is the input rise time. If the rise time is long, power dissipation increases since the current path is established for the entire period that the input signal is passing through the region between the threshold voltages of the upper and lower transistors. Theoretically, if the rise time were zero, no current path would be established and the VI power would be zero. However, with a finite rise time there is always some current flow and this current flow increases rapidly with power supply voltage.

Just a thought about rise time and power dissipation. If a circuit is used to drive many loads, its output rise time will suffer. This will result in an increase in VI power dissipation in every device being driven by that circuit (but not in the drive circuit itself). If power consumption is critical, it may be necessary to improve the rise time of that circuit by buffering or by dividing the loads in order to reduce overall power consumption.

So, to summarize the effects of power supply voltage, input voltage, input rise time and output load capacitance on system power dissipation, we can say the following:

1. **Power supply voltage:** CV^2f power dissipation increases as the square of power supply voltage. VI power dissipation increases approximately as the square of the power supply voltage.
2. **Input voltage level:** VI power dissipation increases if the input voltage lies somewhere between Ground plus a threshold voltage and V_{CC} minus a threshold voltage. The highest power dissipation occurs when V_{IN} is at 1/2 V_{CC}. CV^2f dissipation is unaffected.
3. **Input rise time:** VI power dissipation increases with longer rise times since the DC current path through the device is established for a longer period. The CV^2f power is unaffected by slow input rise times.
4. **Output load capacitance:** the CV^2f power dissipated in a circuit increases directly with load capacitance. VI power in a circuit is unaffected by its output load capacitance. However, increasing output load capacitance will slow down the output rise time of a circuit which in turn will affect the VI power dissipation in the devices it is driving.

INTERFACES TO OTHER LOGIC TYPES

There are two main ideas behind all of the following interfaces to CMOS. First, CMOS outputs should satisfy the current and voltage requirements of the other family's inputs. Second, and probably most important, the other family's outputs should swing as near as possible to the full voltage range of the CMOS power supplies.

P-Channel MOS: there are a number of things to watch for when interfacing CMOS and P-MOS. The first is the power supply set. Most of the more popular P-MOS parts are specified with 17 to 24V power supplies while the maximum power supply voltage for CMOS is 15V. Another problem

is that unlike CMOS, the output swing of a push-pull P-MOS output is significantly less than the power supply voltage across it. P-MOS swings from very close to its more positive supply (V_{SS}) to quite a few volts above its more negative supply (V_{DD}). So, even if P-MOS uses a 15V or lower power supply set, its output swing will not go low enough for a reliable interface to CMOS. There are a number of ways to solve this problem depending on the configuration of the system. We will discuss two solutions for systems that are built totally with MOS and one solution for systems that include bipolar logic.

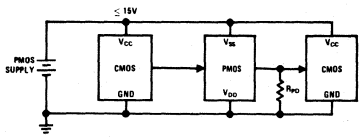
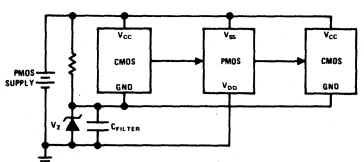


FIGURE 3-4. A One Power Supply System Built Entirely of CMOS and P-MOS.

First, MOS only. P-MOS and CMOS using the same power supply of less than 15V, Figure 3-4.

In this configuration CMOS drives P-MOS directly. However, P-MOS cannot drive CMOS directly because of its output will not pull down close enough to the lower power supply rail. R_{PD} (R pull down) is added to each P-MOS output to pull it all the way down to the lower rail. Its value is selected such that it is small enough to give the desired RC time constant when pulling down but not so small that the P-MOS output cannot pull it virtually all the way up to the upper power supply rail when it needs to. This approach will work with push-pull as well as open drain P-MOS outputs.

Another approach in a purely MOS system is to build a cheap zener supply to bias up the lower power supply rail of CMOS, Figure 3-5.

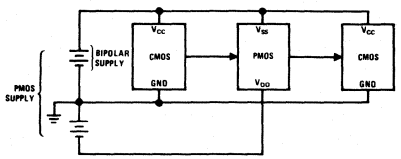


Use a bias supply to reduce the voltage across the CMOS to match the logic swing of the P-MOS. Make sure the resulting voltage across the CMOS is less than 15V.

FIGURE 3-5. A P-MOS and CMOS System Where The P-MOS Supply is Greater Than 15V.

In this configuration the P-MOS supply is selected to satisfy the P-MOS voltage requirement. The bias supply voltage is selected to reduce the total voltage across the CMOS (and therefore its logic swing) to match the minimum swing of the P-MOS outputs. The CMOS can still drive P-MOS directly and now the P-MOS can drive CMOS with no pull-down resistors. The other restrictions are that the total voltage across the CMOS is less than 15V and that the bias supply can handle the current requirements of all the CMOS. This approach is useful if the P-MOS supply must be greater than 15V and the CMOS current requirement is low enough to be done easily with a small discrete component regulator.

If the system has bipolar logic, it will usually have at least two power supplies. In this case, the CMOS is run off the bipolar supply ,and it interfaces directly to P-MOS, Figure 3-6.

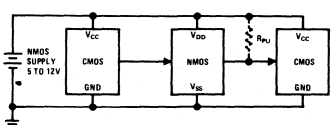


Run the CMOS from the bipolar supply and interface directly to P-MOS

FIGURE 3-6. A System With CMOS, P-MOS and Bipolar Logic.

N-Channel MOS: interfacing to N-MOS is somewhat simpler than interfacing to P-MOS although similar problems exist. First, N-MOS requires lower power supplies than P-MOS, being in the range of 5V to 12V. This is directly compatible with CMOS. Second, N-MOS logic levels range from slightly above the lower power supply rail to about 1 to 2V below the upper rail.

At the higher power supply voltages, N-MOS and CMOS can be interfaced directly since the N-MOS high logic level will be only about 10 to 20 percent below the upper rail. However, at lower supply voltages the N-MOS output level will be down 20 to 40 percent below the upper rail and something may have to be done to raise it. The simplest solution is to add pull up resistors on the N-MOS outputs as shown in Figure 3-7.



Both operate off same supply with pull up resistors optional from N-MOS to CMOS.

FIGURE 3-7. A System With CMOS and N-MOS Only.

TTL, LPTTL, DTL: two questions arise when interfacing bipolar logic families to CMOS. First, is the bipolar family's logic "1" output voltage high enough to drive CMOS directly?

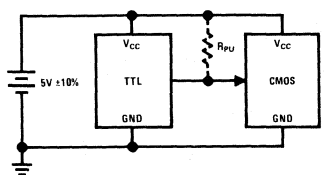
TTL, LPTTL, and DTL can drive 74C series CMOS directly over the commercial temperature range without external pull up resistors. However, TTL and LPTTL cannot drive 4000 series CMOS directly (DTL can) since 4000 series specs do not guarantee that a direct interface with no pull up resistors will operate properly.

DTL and LPTTL manufactured by National (NS LPTTL pulls up one diode drop higher than the LPTTL of other vendors) will also drive 74C directly over the entire military temperature range. LPTTL manufactured by other vendors and standard TTL will drive 74C directly over most of the mil temperature range. However, the TTL logic "1" drops to a somewhat marginal level toward the lower end of the mil temperature range and a pull up resistor is recommended.

According to the curve of DC margin vs V_{CC} for CMOS in Figure 2-5, if the CMOS sees an input voltage greater than $V_{CC} - 1.5V$ ($V_{CC} = 5V$), the output is guaranteed to be less than 0.5V from Ground. The next CMOS element will amplify this 0.5V level to the proper logic levels of V_{CC} or Ground. The standard TTL logic "1" spec is a V_{OUT} min. of 2.4V sourcing a current of 400μA. This is an extremely conservative spec since a TTL output will only approach a one level of 2.4V under the extreme worst case conditions of lowest temperature, high input voltage (0.8V), highest possible leakage currents (into succeeding TTL devices), and V_{CC} at the lowest allowable (V_{CC} = 4.5V).

Under nominal conditions (25°C, V_{IN} = 0.4V, nominal leakage currents into CMOS and V_{CC} = 5V) a TTL logic "1" will be more like $V_{CC} - 2V_D$, or $V_{CC} - 1.2V$. Varying only temperature, the output will change by two times −2mV per °C, or −4 mV per °C. $V_{CC} - 1.2V$ is more than enough to drive CMOS reliably without the use of a pull up resistor.

If the system is such that the TTL logic "1" output can drop below $V_{CC} - 1.5V$, use a pull up resistor to improve the logic "1" voltage into the CMOS.



Pull up resistor, R_{PU}, is needed only at the lower end of the Mil temperature range.

FIGURE 3-8. TTL to CMOS Interface.

The second question is, can CMOS sink the bipolar input current and not exceed the maximum value of the bipolar logic zero input voltage? The logic "1" input is no problem.

The LPTTL input current is small enough to allow CMOS to drive two loads directly. Normal power TTL input currents are ten times higher than those in LPTTL and consequently the CMOS output voltage will be well above the input logic "0" maximum of 0.8V. However, by carefully examining the CMOS output specs we will find that a two input NOR gate can drive one TTL load, albeit somewhat marginally. For example, the logical "0" output voltage for both an MM74C00 and MM74C02 over temperature is specified at 0.4V sinking 360μA (about 420μA at 25°C) with an input voltage of 4.0V and a V_{CC} of 4.75V. Both schematics are shown in Figure 3-9.

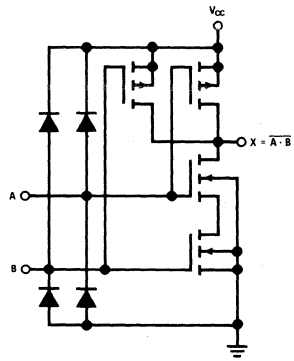


FIGURE 3-9a. MM74C00.

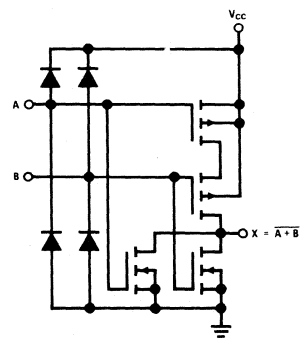


FIGURE 3-9b. MM74C02.

Both parts have the same current sinking spec but their structures are different. What this means is that either of the lower transistors in the MM74C02 can sink the same current as the two lower series transistors in the MM74C00. Both MM74C02 transistors together can sink twice the specified current for a given output voltage. If we allow the output voltage to go to 0.8V, then a MM74C02 can sink four times 360μA, or 1.44 mA which is nearly 1.6 mA. Actually, 1.6 mA is the maximum

spec for the TTL input current and most TTL parts run at about 1 mA. Also, 360μA is the minimum CMOS sink current spec, the parts will really sink somewhere between 360 and 540μA (between 2 and 3 LPTTL input loads). The 360μA sink current is specified with an input voltage of 4.0V. With an input voltage of 5.0V, the sink current will be about 560μA over temperature, making it even easier to drive TTL. At room temperature with an input voltage of 5V, a CMOS output can sink about 800μA. A 2 input NOR gate, therefore, will sink about 1.6 mA with a V_{OUT} of about 0.4V if both NOR gate inputs are at 5V.

The main point of this discussion is that a common 2 input CMOS NOR gate such as an MM74C02 can be used to drive a normal TTL load in lieu of a special buffer. However, the designer must be willing to sacrifice some noise immunity over temperature to do so.

TIMING CONSIDERATIONS IN CMOS MSIs

There is one more thing to be said in closing. All the flip-flops used in CMOS designs are genuinely edge sensitive. This means that the J-K flip-flops do not "ones catch" and that some of the timing restrictions that applied to the control lines on MSI functions in TTL have been relaxed in the 74C series.

CMOS Linear Applications

National Semiconductor
Application Note 88
Gene Taajes

PNP and NPN bipolar transistors have been used for many years in "complementary" type of amplifier circuits. Now, with the arrival of CMOS technology, complementary P-channel/N-channel MOS transistors are available in monolithic form. The MM74C04 incorporates a P-channel MOS transistor and an N-channel MOS transistor connected in complementary fashion to function as an inverter.

Due to the symmetry of the P- and N-channel transistors, negative feedback around the complementary pair will cause the pair to self bias itself to approximately 1/2 of the supply voltage. Figure 1 shows an idealized voltage transfer characteristic curve of the CMOS inverter connected with negative feedback. Under these conditions the inverter is biased for operation about the midpoint in the linear segment on the steep transition of the voltage transfer characteristic as shown in Figure 1.

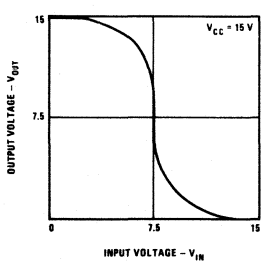


FIGURE 1. Idealized Voltage Transfer Characteristics of an MM74C04 Inverter.

Under AC conditions, a positive going input will cause the output to swing negative and a negative going input will have an inverse effect. Figure 2 shows 1/6 of a MM74C04 inverter package connected as an AC amplifier.

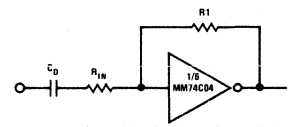


FIGURE 2. A 74CMOS Invertor Biased for Linear Mode Operation.

The power supply current is constant during dynamic operation since the inverter is biased for Class A operation. When the input signal swings near the supply, the output signal will become distorted because the P-N channel devices are driven into the non-linear regions of their transfer characteristics. If the input signal approaches the supply voltages, the P- or N-channel transistors become saturated and supply current is reduced to essentially zero and the device behaves like the classical digital inverter.

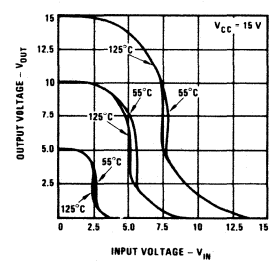


FIGURE 3. Voltage Transfer Characteristics for an Inverter Connected as a Linear Amplifier.

Figure 3 shows typical voltage characteristics of each inverter at several values of the V_{CC}. The shape of these transfer curves are relatively constant with temperature. Temperature affects for the self biased inverter with supply voltage is shown in Figure 4. When the amplifier is operating at 3 volts, the supply current changes drastically as a function of supply voltage because the MOS transistors are operating in the proximity of their gate-source threshold voltages.

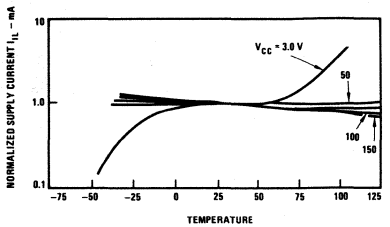


FIGURE 4. Normalized Amplifier Supply Current Versus Ambient Temperature Characteristics.

Figure 5 shows typical curves of voltage gain as a function of operating frequency for various supply voltages.

Output voltages can swing within millivolts of the supplies with either a single or dual supply.

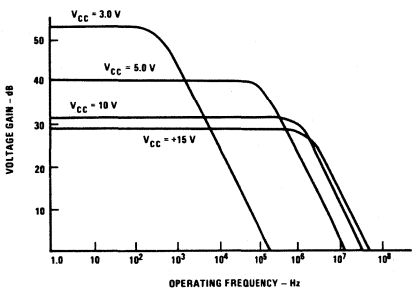


FIGURE 5. Typical Voltage Gain Versus Frequency Characteristics for Amplifier Shown in Figure 2.

APPLICATIONS

Cascading Amplifiers for Higher Gain.

By cascading the basic amplifier block shown in Figure 2 a high gain amplifier can be achieved. The gain will be multiplied by the number of stages used. If more than one inverter is used inside the feedback loop (as in Figure 6) a higher open loop gain is achieved which results in more accurate closed loop gains.

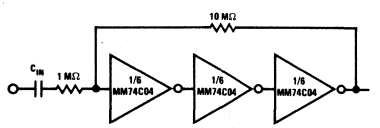


FIGURE 6. Three CMOS Inverters Used as an X10 AC Amplifier.

Post Amplifier for Op Amps.

A standard operational amplifier used with a CMOS inverter for a Post Amplifier has several advantages. The operational amplifier essentially sees no load condition since the input impedance to the inverter is very high. Secondly, the CMOS inverters will swing to within millivolts of either supply. This gives the designer the advantage of operating the operational amplifier under no load conditions yet having the full supply swing capability on the output. Shown in Figure 7 is the LM4250 micropower Op Amp used with a 74C04 inverter for increased output capability while maintaining the low power advantage of both devices.

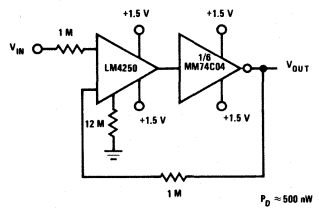


FIGURE 7. MM74C04 Inverter Used as a Post Amplifier for a Battery Operated Op Amp.

The MM74C04 can also be used with single supply amplifier such as the LM324. With the circuit shown in Figure 8, the open loop gain is approximately 160 dB. The LM324 has 4 amplifiers in a package and the MM74C04 has 6 amplifiers per package.

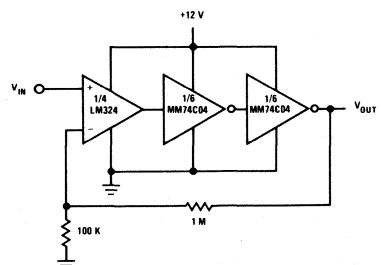


FIGURE 8. Single Supply Amplifier Using a CMOS Cascade Post Amplifier with the LM324.

CMOS inverters can be paralleled for increased power to drive higher current loads. Loads of 5.0 mA per inverter can be expected under AC conditions.

Other 74C devices can be used to provide greater complementary current outputs. The MM74C00 NAND Gate will provide approximately 10 mA

from the V_{CC} supply while the MM74C02 will supply approximately 10 mA from the negative supply. Shown in Figure 9 is an operational amplifier using a CMOS power post amplifier to provide greater than 40 mA complementary currents.

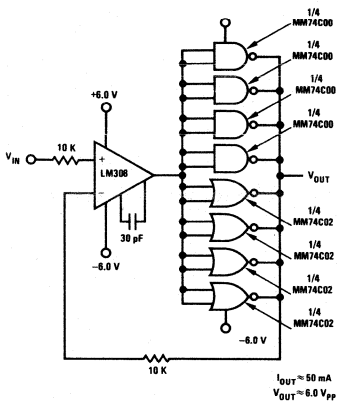


FIGURE 9. MM74C00 and MM74C02 Used as a Post Amplifier to Provide Increased Current Drive.

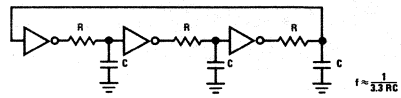
Other Applications.

Shown in Figure 10 is a variety of applications utilizing CMOS devices. Shown is a linear phase shift oscillator and an integrator which use the CMOS devices in the linear mode as well as a few circuit ideas for clocks and one shots.

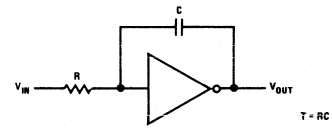
Conclusion

Careful study of CMOS characteristics show that CMOS devices used in a system design can be used for linear building blocks as well as digital blocks.

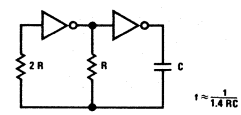
Utilization of these new devices will decrease package count and reduce supply requirements. The circuit designer now can do both digital and linear designs with the same type of device.



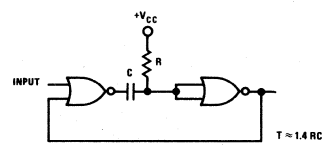
Phase Shift Oscillator Using MM74C04



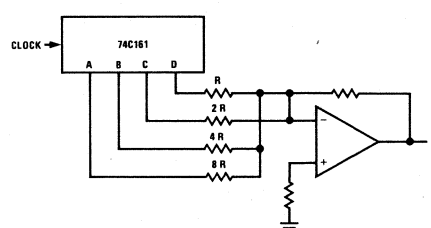
Integrator Using Any Inverting CMOS Gate



Square Wave Oscillator



One Shot



Staircase Generator

FIGURE 10. Variety of Circuit Ideas Using CMOS Devices.

54C/74C Family Characteristics

National Semiconductor
Application Note 90
Thomas P. Redfern

INTRODUCTION

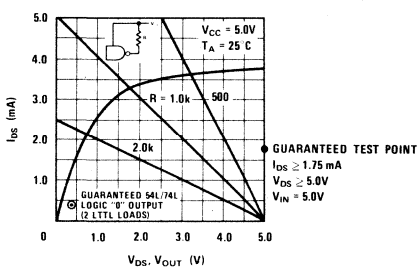
The purpose of this 54C/74C Family Characteristics application note is to set down, in one place, all those characteristics which are common to the devices in the MM54C/MM74C logic family. The characteristics which can be considered to apply are:

1. Output voltage-current characteristics
2. Noise characteristics
3. Power consumption
4. Propagation delay (speed)
5. Temperature characteristics

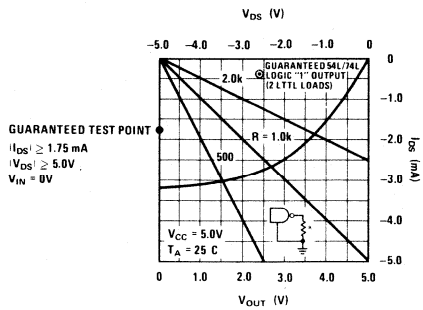
With a good understanding of the above characteristics the designer will have the necessary tools to optimize his system. An attempt will be made to present the information in as simple a manner as possible to facilitate its use. This coupled with the fact that 54C/74C has the same function and pin-out as standard series 54L/74L will make the application of CMOS to digital systems very straightforward.

OUTPUT CHARACTERISTICS

Figure 1 and Figure 2 show typical output drain characteristics for the basic inverter used in the 54C/74C family. For more detailed information on the operation of the basic inverter the reader is directed to application note AN-77, "CMOS, The Ideal Logic Family." Although more complex gates, and MSI devices, may be composed of combinations of parallel and series transistors the considerations that govern the output characteristics of the basic inverter apply to these more complex structures as well.

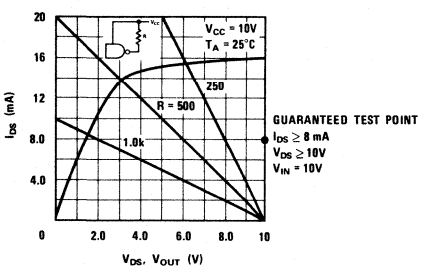


(A) Typical Output Sink Characteristic (N-Channel)

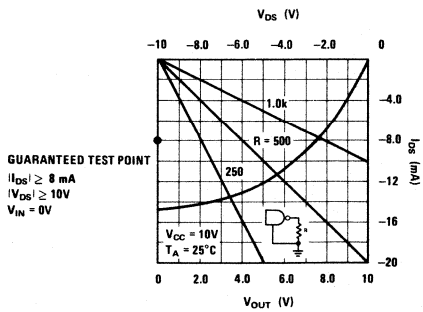


(B) Typical Output Source Characteristic (P-Channel)

FIGURE 1



(A) Typical Output Sink Characteristic (N-Channel)



(B) Typical Output Source Characteristic (P-Channel)

FIGURE 2

The 54C/74C family is designed so that the output characteristics of all devices are matched as closely as possible. To ensure uniformity all devices are tested at four output conditions (see Figures 1 and 2). These points are:

V_{CC} = 5.0V	V_{IN} = 5.0V $I_{DS} \geq$ 1.75 mA $V_{DS} \geq$ 5.0V	V_{IN} = 0V $\|I_{DS}\| \geq$ 1.75 mA $\|V_{DS}\| \geq$ 5.0V
V_{CC} = 10V	V_{IN} = 10V $I_{DS} \geq$ 8.0 mA $V_{DS} \geq$ 10V	V_{IN} = 0V $\|I_{DS}\| \geq$ 8.0 mA $\|V_{DS}\| \geq$ 10V

Note that each device data sheet guarantees these points in the table of electrical characteristics.

The output characteristics can be used to determine the output voltage for any load condition. Figures 1 and 2 show load lines for resistive loads to V_{CC} for sink currents and to GND for source currents. The intersections of this load line with the drain characteristic in question gives the output voltage. For example at V_{CC} = 5.0V, V_{OUT} = 1.5V (typ) with a load of 500Ω to ground.

These figures also show the guaranteed points for driving two 54L/74L standard loads. As can be seen there is typically ample margin at V_{CC} = 5.0V.

In the case where the 54C/74C device is driving another CMOS device the load line is coincident with the I_{DS} = 0 axis and the output will then typically switch to either V_{CC} or ground.

NOISE CHARACTERISTICS

Definition of Terms

Noise Immunity: The noise immunity of a logic element is that voltage which applied to the input will cause the output to change its output state.

Noise Margin: The noise margin of a logic element is the difference between the guaranteed logical "1" ("0") level output voltage and the guaranteed logical "1" ("0") level input voltage.

The transfer characteristic of Figure 3 shows typical noise immunity and guaranteed noise margin for a 54C/74C device operating at V_{CC} = 10V. The typical noise immunity does not change with voltage and is 45% of V_{CC}.

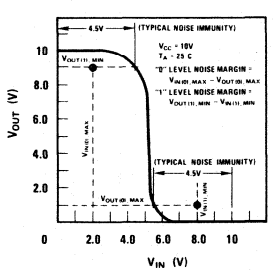


FIGURE 3. Typical Transfer Characteristic

All 54C/74C devices are guaranteed to have a noise margin of 1.0V or greater over all operating conditions (see Figure 4).

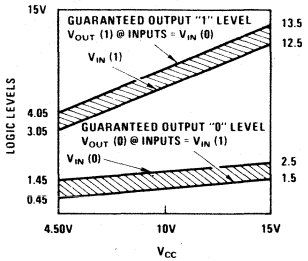
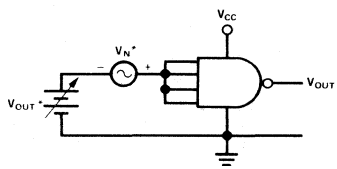


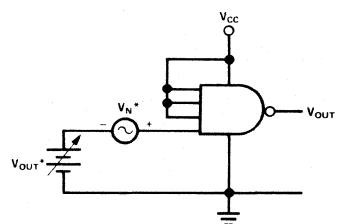
FIGURE 4. Guaranteed Noise Margin Over Temperature vs V_{CC}

Noise immunity is an important device characteristic. However, noise margin is of more use to the designer because it very simply defines the amount of noise a system can tolerate under any circumstances and still maintain the integrity of logic levels.

Any noise specification to be complete must define how measurements are to be made. Figure 5 indicates two extreme cases; driving all inputs simultaneously and driving one input at a time. Both conditions must be included because each represents one worst case extreme.



(A)



*V_{OUT} = $V_{OUT(1)MIN}$, $V_{OUT(0)MAX}$
V_N = ALLOWABLE NOISE VOLTAGE = 1.0V

(B)

FIGURE 5. Noise Margin Test Circuits

To guarantee a noise margin of 1.0V, all 54C/74C devices are tested under both conditions. It is important to note that this guarantees that every node within a system can have 1.0V of noise, in logic "1" or logic "0" state, without malfunctioning. This could not be guaranteed without testing for both conditions in Figure 5.

POWER CONSUMPTION

There are four sources of power consumption in CMOS devices: (1) leakage current (2) transient power due to load capacitance (3) transient power due to internal capacitance and (4) transient power due to current spiking during switching.

The first, leakage current, is the easiest to calculate and is simply the leakage current times V_{CC}. The data sheet for each specific device specifies this leakage current.

The second, transient power due to load capacitance, can be derived from the fact that the energy stored on a capacitor is 1/2 CV^2. Therefore every time the load capacitance is charged or discharged this amount of energy must be provided by the CMOS device. The energy per cycle is then 2 [(1/2) CV_{CC}^2] = CV_{CC}^2. Energy per unit time, or power, is then CV_{CC}^2 f, where C is the load capacitance and f is the frequency.

The third, transient power due to internal capacitance takes exactly the same form as the load capacitance. Every device has some internal nodal capacitance which must be charged and discharged. This then represents another power term which must be considered.

The fourth, transient power due to switching current, is caused by the fact that whenever a CMOS device goes through a transition, with $V_{CC} \geq 2\ V_T$, there is a time when both N-channel and P-channel devices are both conducting. An expression for this current is derived in application note AN-77. The expression is:

$$P_{VI} = \frac{1}{2} (V_{CC} - 2\ V_T)\ I_{CC\,MAX}\ (t_{RISE} + t_{FALL})\ f$$

where:

V_T = threshold voltage

$I_{CC(MAX)}$ = peak non-capacitive current during switching

f = frequency

Note that this expression, like the capacitive power term is directly proportional to frequency. If the P_{VI} term is combined with the term arising from the internal capacitance, a capacitance C_{PD} may be defined which closely approximates the no load power consumption for a CMOS device when used in the following expression:

Power (no load) = $C_{PD}\ V_{CC}^2\ f$

The total power consumption is then simplified to:

Total Power = $(C_{PD} + C_L)\ V_{CC}^2\ f + I_{LEAK}\ V_{CC}$ (1)

The procedure for obtaining C_{PD} is to measure the no load power at V_{CC} = 10V vs frequency and calculate the value of C_{PD} which corresponds to the measured power consumption. This value of C_{PD} is given on each 54C/74C data sheet and with equation (1) the computation of power consumption is straightforward.

To simplify the task even further Figure 6 gives a graph of normalized power vs frequency for different power supply voltages. To obtain actual power consumption find the normalized power for a particular V_{CC} and frequency, then multiply by $C_{PD} + C_L$.

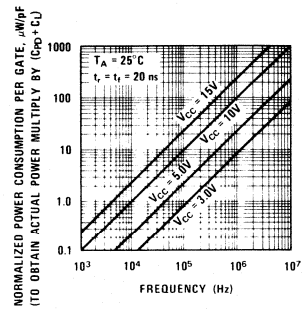


FIGURE 6. Normalized Typical Power Consumption vs Frequency

As an example let's find the total power consumption for an MM74C00 operating at f = 100 kHz, V_{CC} = 10V and C_L = 50 pF. From the curve, normalized power per gate equals 10μW/pF. From the data sheet C_{PD} = 12 pF; therefore, actual power per gate is:

$$\frac{\text{power}}{\text{gate}} = \frac{10\mu W}{pF} \times (12\ pF + 50\ pF) = \frac{0.62\ mW}{\text{gate}}$$

$$\text{total power} = \frac{\text{no. of gates}}{\text{package}} \times \frac{\text{power}}{\text{gate}} + I_{LEAKAGE} \times V_{CC}$$

$$= 4 \times 0.62\ mW + 0.01\mu A \times 10V \cong 2.48\ mW$$

Up to this point the discussion of power consumption has been limited to simple gate functions. Power consumption for an MSI function is more complex but the same technique just derived applies. To demonstrate the technique let's compute the total power consumption of a MM74C161, four bit binary counter, at V_{CC} = 10V, f = 1 MHz and C_L = 50 pF on each output.

The no load power is still given by P (no load) = $C_{PD}\ V_{CC}^2$ f. This demonstrates the usefulness of the concept of the internal capacitance, C_{PD}. Even through the circuit is very complex and has many nodes charging and discharging at various rates, all of the effects can be easily lumped into one easy to use term, C_{PD}.

Calculation of transient power due to load capacitance is a little more complex since each output is switched at one half the rate of the previous output: Taking this into account the complete expression for power consumption is:

$$P_{TOTAL} = \underbrace{C_{PD} V_{CC}^2 f}_{\text{no load power}} + \underbrace{C_L V_{CC}^2 \frac{f}{2}}_{\text{output power of 1st stage}} + \underbrace{C_L V_{CC}^2 \frac{f}{4}}_{\text{2nd stage}}$$

$$+ \underbrace{C_L V_{CC}^2 \frac{f}{8}}_{\text{3rd stage}} + \underbrace{2 C_L V_{CC}^2 \frac{f}{16}}_{\text{4th stage \& carry output}} + \underbrace{I_L V_{CC}}_{\text{leakage term}}$$

This reduces to:

$$P_{TOTAL} = (C_{PD} + C_L) V_{CC}^2 f + I_L V_{CC}$$

From the data sheet C_{PD} = 90 pF and I_L = 0.05μA. Using Figure 6 total power is then:

$$P_{TOTAL} = (90\text{ pF} + 50\text{ pF}) \times \frac{100\mu\text{W}}{\text{pF}} + 0.05 \times 10^{-6} \times 10\text{V} \cong 14\text{ mW}$$

This demonstrates that with more complex devices the concept of C_{PD} greatly simplifies the calculation of total power consumption. It becomes an easy task to compute power for different voltages and frequencies by use of Figure 6 and the equations above.

PROPAGATION DELAY

Propagation delay for all 54C/74C devices is guaranteed with a load of 50 pF *and input rise and fall times of 20 ns.* A 50 pF load was chosen, instead of 15 pF as in the 4000 series, because it is representative of loads commonly seen in CMOS systems. A good rule of thumb, in designing with CMOS, is to assume 10 pF of interwiring capacitance. Operating at the specified propagation delay would allow 5 pF fanout for the 4000 series while 54C/74C has a fanout of 40 pF. A fanout of 5 pF (one gate input) is all but useless, and specified propagation delay would most probably not be realized in an actual system.

Operating at loads other than 50 pF poses a problem since propagation is a function of load capacitance. To simplify the problem Figure 7 has been generated and gives the slope of the propagation delay vs load capacitance line (Δt_{pd}/pF) as a function of power supply voltage. Because

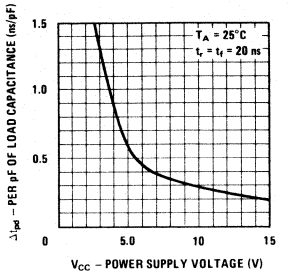


FIGURE 7. Typical Propagation Delay per pF of Load Capacitance vs Power Supply

the propagation delay for zero load capacitance is not zero and depends on the internal structure of each device, an offset term must be added that is unique to a particular device type. Since each data sheet gives propagation delay for 50 pF the actual delay for different loads can be computed with the aid of the following equation:

$$t_{pd}\Big|_{C_L = C} = (C - 50)\text{ pF} \times \frac{\Delta t_{pd}}{\text{pF}} + t_{pd}\Big|_{C_L = 50\text{ pF}}$$

where:

C = Actual load capacitance

$t_{pd}\Big|_{C_L = 50\text{ pF}}$ = propagation delay with 50 pF load, (specified on each device data sheet)

$\frac{\Delta t_{pd}}{\text{pF}}$ = Value obtained from Figure 7.

As an example let's compute the propagation delay for an MM74C00 driving 15 pF load and operating with a V_{CC} = 5.0V. The equation gives:

$$t_{pd}\Big|_{C_L = 15\text{ pF}} = (15 - 50)\text{ pF} \times 0.57 \frac{\text{ns}}{\text{pF}} + 50\text{ ns}$$

$$= -20\text{ ns} + 50\text{ ns} = 30\text{ ns}$$

The same formula and curves may be applied to more complex devices. For example the propagation delay from data to output for an MM74C157 operating at V_{CC} = 10V and C_L = 100 pF is:

$$t_{pd}\Big|_{C_L = 100\text{ pF}} = (100 - 50)\ 0.29\text{ ns} + 70\text{ ns}$$

$$= 14.5 + 70 \cong 85\text{ ns}$$

It is significant to note that this equation and Figure 7 apply to *all* 54C/74C devices. This is true because of the close match in drive characteristics of every device including MSI functions, i.e., the slope of the propagation delay vs load capacitance line at a given voltage is typically equal for all devices. The only exception is high fan-out buffers which have a smaller $\Delta t_{pd}/pF$.

Another point to consider in the design of a CMOS system is the affect of power supply voltage on propagation delay. Figure 8 shows propagation delay as a function of V_{CC} and propagation delay times power consumption vs V_{CC} for an MM74C00 operating with 50 pF load at f = 100 kHz.

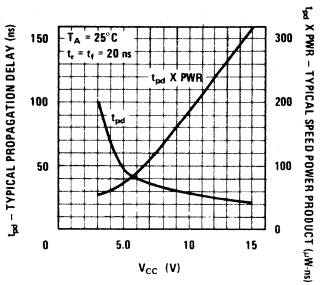


FIGURE 8. Speed Power Product and Propagation Delay vs V_{CC}

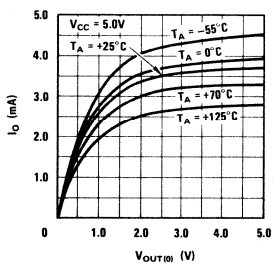
Above V_{CC} = 5.0V note the speed power product curve approaches a straight line. However the t_{pd} curve starts to "flatten out." Going from *V_{CC} = 5.0V to V_{CC} = 10V gives a 40% decrease in propagation delay and going from V_{CC} = 10V to V_{CC} = 15V only decreases propagation delay by 25%.* Clearly for V_{CC} > 10V a small increase in speed is gained by a disproportionate increase in power. Conversely, for small decreases in power below V_{CC} = 5.0V large increases in propagation delay result.

Obviously it is optimum to use the lowest voltage consistent with system speed requirements. However in general it can be seen from Figure 8 that the best speed power performance will be obtained in the V_{CC} = 5.0V to V_{CC} = 10V range.

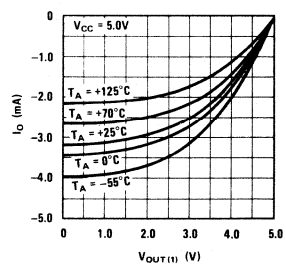
TEMPERATURE CHARACTERISTICS

Figures 9 and 10 give temperature variations in drain characteristics for the N-channel and P-channel devices operating at V_{CC} = 5.0V and V_{CC} = 10V respectively. As can be seen from these curves the output sink and source current decreases as temperature increases. The affect is almost linear and can be closely approximated by a temperature coefficient of −0.3% per degree centigrade.

Since the t_{pd} can be entirely attributed to rise and fall time, the temperature dependance of t_{pd} is a function of the rate at which the output load capacitance can be charged and discharged. This in turn is a function of the sink/source current which was shown above to vary as −0.3% per degree centigrade. Consequently we can say that t_{pd} varies as −0.3% per degree centigrade. Actual measurements of t_{pd} with temperature verifies this number.

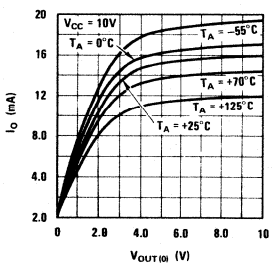


(A) Typical Output Drain Characteristic (N-Channel)

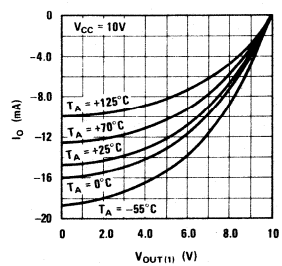


(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 9



(A) Typical Output Drain Characteristic (N-Channel)



(B) Typical Output Drain Characteristic (P-Channel)

FIGURE 10

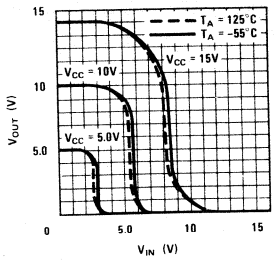


FIGURE 11. Typical Gate Transfer Characteristics

The drain characteristics of Figure 9 and 10 show considerable variation with temperature. Examination of the transfer characteristics of Figure 11 indicates that they are almost independent of temperature. The transfer characteristic is not dependent on temperature because although both the N-channel and P-channel device characteristics change with temperature these changes track each other closely. The proof of this tracking is the temperature independance of the transfer characteristics. Noise margin and maximum/minimum logic levels will then not be dependent on temperature.

As discussed previously power consumption is a function of C_{PD}, C_L, V_{CC}, f and $I_{LEAKAGE}$. All of these terms are essentially constant with temperature except $I_{LEAKAGE}$. However, the leakage current specified on each 54C/74C device applies across the entire temperature range and therefore represents a worst case limit.

CMOS Oscillators

National Semiconductor
Application Note 188
Mike Watts

INTRODUCTION

This note describes several square wave oscillators that can be built using CMOS logic elements. These circuits offer the following advantages:

- Guaranteed startability
- Relatively good stability with respect to power supply variations
- Operation over a wide supply voltage range (3V to 15V)
- Operation over a wide frequency range from less than 1 Hz to about 15 MHz
- Low power consumption (see AN-90)
- Easy interface to other logic families and elements including TTL

Several RC oscillators and two crystal controlled oscillators are described. The stability of the RC oscillator will be sufficient for the bulk of applications; however, some applications will probably require the stability of a crystal. Some applications that require a lot of stability are:

1. Timekeeping over a long interval. A good deal of stability is required to duplicate the performance of an ordinary wrist watch (about 12 ppm). This is, of course, obtainable with a crystal. However, if the time interval is short and/or the resolution of the timekeeping device is relatively large, an RC oscillator may be adequate. For example: if a stopwatch is built with a resolution of tenths of seconds and the longest interval of interest is two minutes, then an accuracy of 1 part in 1200 (2 minutes x 60 seconds/minute x 10 tenth/second) may be acceptable since any error is less than the resolution of the device.

2. When logic elements are operated near their specified limits. It may be necessary to maintain clock frequency accuracy within very tight limits in order to avoid exceeding the limits of the logic family being used, or in which the timing relationships of clock signals in dynamic MOS memory or shift register systems must be preserved.

3. Baud rate generators for communications equipment.

4. Any system that must interface with other tightly specified systems. Particularly those that use a "handshake" technique in which Request or Acknowledge pulses must be of specific widths.

LOGICAL OSCILLATORS

Before describing any specific circuits, a few words about logical oscillators may clear up some recurring confusion.

Any odd number of inverting logic gates will oscillate if they are tied together in a ring as shown in *Figure 1.* Many beginning logic designers have discovered this (to their chagrin) by inadvertently providing such a path in their designs. However, some people are confused by the circuit in *Figure 1* because they are accustomed to seeing sinewave oscillators implemented with positive feedback, or amplifiers with non-inverting gain. Since the concept of phase shift becomes a little strained when the inverters remain in their linear region for such a short period, it is far more straightforward to analyze the circuit from the standpoint of ideal switches with finite propagation delays rather than as amplifiers with 180° phase shift. It then becomes obvious that a "1" chases itself around the ring and the network oscillates.

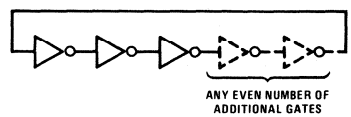


FIGURE 1. Odd Number of Inverters will Always Oscillate

The frequency of oscillation will be determined by the total propagation delay through the ring and is given by the following equation.

$$f = \frac{1}{2nTp}$$

Where:

f = frequency of oscillation
Tp = Propagation delay per gate
n = number of gates

This is not a practical oscillator, of course, but it does illustrate the maximum frequency at which such an oscillator will run. All that must be done to make this a useful oscillator is to slow it down to the desired frequency. Methods of doing this are described later.

To determine the frequency of oscillation, it is necessary to examine the propagation delay of the inverters. CMOS propagation delay depends on supply voltage and load capacitance. Several curves for propagation delay for National's 74C line of CMOS gates are reproduced in *Figure 2.* From these, the natural frequency of oscillation of an odd number of gates can be determined.

An example may be instructive.

Assume the supply voltage is 10V. Since only one input is driven by each inverter, the load capacitance on each inverter is at most about 8 pF. Examine the curve in *Figure 2c* that is drawn for V_{CC} = 10V and extrapolate it down to 8 pF. We see that the curve predicts a propagation delay of about 17 ns. We can then calculate the frequency of oscillation for three inverters using the expression mentioned above. Thus:

$$f = \frac{1}{2 \times 3 \times 17 \times 10^{-9}} = 9.8 \text{ MHz}$$

Lab work indicates this is low and that something closer to 16 MHz can be expected. This reflects the conservative nature of the curves in *Figure 2.*

Since this frequency is directly controlled by propagation delays, it will vary a great deal with temperature, supply voltage, and any external loading, as indicated by the graphs in *Figure 2.* In order to build a usefully stable oscillator it is necessary to add passive elements that determine oscillation frequency and minimize the effect of CMOS characteristics.

STABLE RC OSCILLATOR

Figure 3 illustrates a useful oscillator made with three inverters. Actually, any inverting CMOS gate or combination of gates could be used. This means left over portions

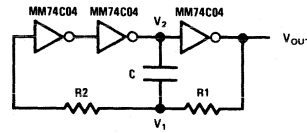


FIGURE 3. Three Gate Oscilaltor

of gate packages can be often used. The duty cycle will be close to 50% and will oscillate at a frequency that is given by the following expression.

$$f \cong \frac{1}{2 \text{ R1 C} \left(\frac{0.405 \text{ R2}}{\text{R1} + \text{R2}} + 0.693 \right)}$$

Another form of this expression is:

$$f \cong \frac{1}{2C (0.405 R_{eq} + 0.693 R1)}$$

Where:

$$R_{eq} = \frac{R1 \ R2}{R1 + R2}$$

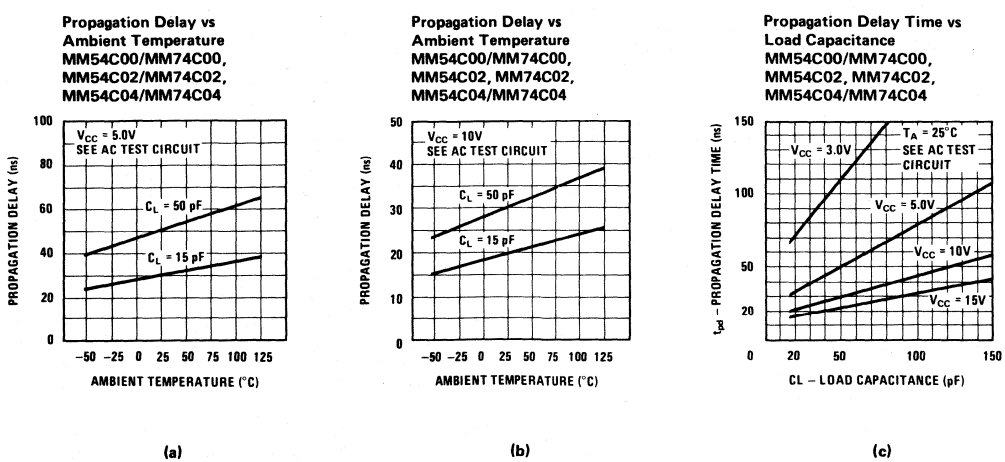


FIGURE 2. Propagation Delay for 74C Gates

The following three special cases may be useful.

If R1 = R2 = R $\quad f \cong \dfrac{0.559}{RC}$

If R2 >>> R1 $\quad f \cong \dfrac{0.455}{RC}$

If R2 <<< R1 $\quad f \cong \dfrac{0.722}{RC}$

Figure 4 illustrates the approximate output waveform and the voltage V_1 at the charging node.

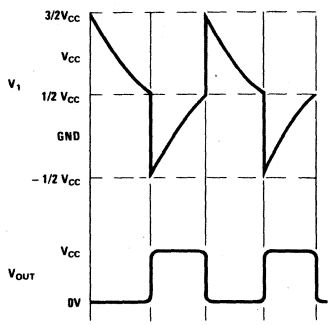


FIGURE 4. Waveforms for Oscillator in Figure 3

Note that the voltage V_2 will be clamped by input diodes when V_1 is greater than V_{CC} or more negative than ground. During this portion of the cycle current will flow through R2. At all other times the only current through R2 is a very minimal leakage term. Note also that as soon as V_1 passes through threshold (about 50% of supply) and the input to the last inverter begins to change, V_1 will also change in a direction that reinforces the switching action; i.e., providing positive feedback. This further enhances the stability and predictability of the network.

This oscillator is fairly insensitive to power supply variations due largely to the threshold tracking close to 50% of the supply voltage. Just how stable it is will be determined by the frequency of oscillation; the lower the frequency the more stability and vice versa. This is because propagation delay and the effect of threshold shifts comprise a smaller portion of the overall period. Stability will also be enhanced if R1 is made large enough to swamp any variations in the CMOS output resistance.

TWO GATE OSCILLATOR WILL NOT NECESSARILY OSCILLATE

A popular oscillator is shown in *Figure 5a.* The only undesirable feature of this oscillator is that it may not oscillate. This is readily demonstrated by letting the value of C go to zero. The network then degenerates into *Figure 5b,* which obviously will not oscillate. This illustrates that there is some value of C1 that will not force the network to oscillate. The real difference between this two gate oscillator and the three gate oscillator is that the former must be forced to oscillate by the capacitor while the three gate network will always oscillate willingly and is simply slowed down by the capacitor. The three gate network will always oscillate, regardless of the value of C1 but the two gate oscillator will not oscillate when C1 is small.

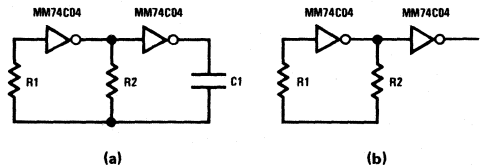


FIGURE 5. Less Than Perfect Oscillator

The only advantage the two gate oscillator has over the three gate oscillator is that it uses one less inverter. This may or may not be a real concern, depending on the gate count in each user's specific application. However, the next section offers a real minimum parts count oscillator.

A SINGLE SCHMITT TRIGGER MAKES AN OSCILLATOR

Figure 6 illustrates an oscillator made from a single Schmitt trigger. Since the MM74C14 is a hex Schmitt trigger, this oscillator consumes only one sixth of a package. The remaining 5 gates can be used either as ordinary inverters like the MM74C04 or their Schmitt trigger characteristics can be used to advantage in the normal manner. Assuming these five inverters can be used elsewhere in the system, *Figure 6* must represent the ultimate in low gate count oscillators.

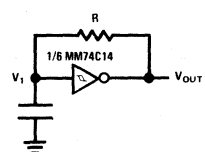


FIGURE 6. Schmitt Trigger Oscillator

Voltage V_1 is depicted in *Figure 7* and changes between the two thresholds of the Schmitt trigger. If these thresholds were constant percentages of V_{CC} over the supply voltage range, the oscillator would be insensitive to variations in V_{CC}. However, this is not the case. The thresholds of the Schmitt trigger vary enough to make the oscillator exhibit a good deal of sensitivity to V_{CC}.

Applications that do not require extreme stability or that have access to well regulated supplies should not be bothered by this sensitivity to V_{CC}. Variations in threshold can be expected to run as high as four or five percent when V_{CC} varies from 5V to 15V.

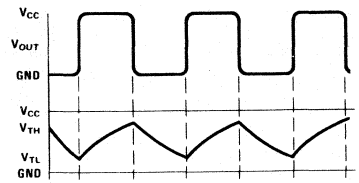


FIGURE 7. Waveforms for Schmitt Trigger Oscillator in Figure 6

A CMOS Crystal Oscillator

Figure 8 illustrates a crystal oscillator that uses only one CMOS inverter as the active element. Any odd number of inverters may be used, but the total propagation delay through the ring limits the highest frequency that can be obtained. Obviously, the fewer inverters that are used, the higher the maximum possible frequency.

CONCLUSIONS

A large number of oscillator applications can be implemented with the extremely simple, reliable, inexpensive and versatile CMOS oscillators described in this note. These oscillators consume very little power compared to most other approaches. Each of the oscillators requires less than one full package of CMOS inverters of the MM74C04 variety. Frequently such an oscillator can be built using leftover gates of the MM74C00, MM74C02, MM74C10 variety. Stability superior to that easily attainable with TTL oscillators is readily attained, particularly at lower frequencies. These oscillators are so versatile, easy to build, and inexpensive that they should find their way into many diverse designs.

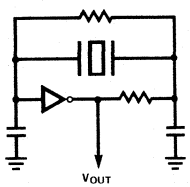


FIGURE 8. Crystal Oscillator

Using the CMOS Dual Monostable Multivibrator

National Semiconductor
Application Note 138
Thomas P. Redfern

INTRODUCTION

The MM54C221/MM74C221 is a dual CMOS monostable multivibrator. Each one-shot has three inputs (A, B and CLR) and two outputs (Q and $\overline{Q}$). The output pulse width is set by an external RC network.

The A and B inputs trigger an output pulse on a negative or positive input transition respectively. The CLR input when low resets the one-shot. Once triggered the A and B inputs have no further control on the output.

THEORY OF OPERATION

Figure 1 shows that in its stable state, the one-shot clamps C_{EXT} to ground by turning N1 ON and holds the positive comparator input at V_{CC} by turning N2 OFF. The prefix N is used to denote N-channel transistors.

The signal, G, gating N2 OFF also gates the comparator OFF thereby keeping the internal power dissipation to an absolute minimum. The only power dissipation when in the stable state is that generated by the current through R_{EXT}. The bulk of this dissipation is in R_{EXT} since the voltage drop across N1 is very small for normal ranges of R_{EXT}.

To trigger the one-shot the CLR input must be high. The gating, G, on the comparator is designed such that the comparator output is high when the one-shot is in its stable state. With the CLR input high the clear input to FF is disabled allowing the flip-flop to respond to the A or B input. A negative transition on A or a positive transition on B sets Q to a high state. This in turn gates N1 OFF, and N2 and the comparator ON.

Gating N2 ON establishes a reference of 0.63 V_{CC} on the comparator's positive input. Since the voltage on C_{EXT} can not change instantaneously V1 = 0V at this time. The comparator then will maintain its one level on the output. Gating N1 OFF allows C_{EXT} to start charging through R_{EXT} toward V_{CC} exponentially.

Assuming a perfect comparator (zero offset and infinite gain) when the voltage on C_{EXT}, V1, equals 0.63 V_{CC} the comparator output will go from a high state to a low state resetting Q to a low state. *Figure 2* is a timing diagram summarizing this sequence of events.

This diagram is idealized by assuming zero rise and fall times and zero propagation delay but it shows the basic operation of the one-shot. Also shown is the effect of taking the CLR input low. Whenever CLR goes low FF

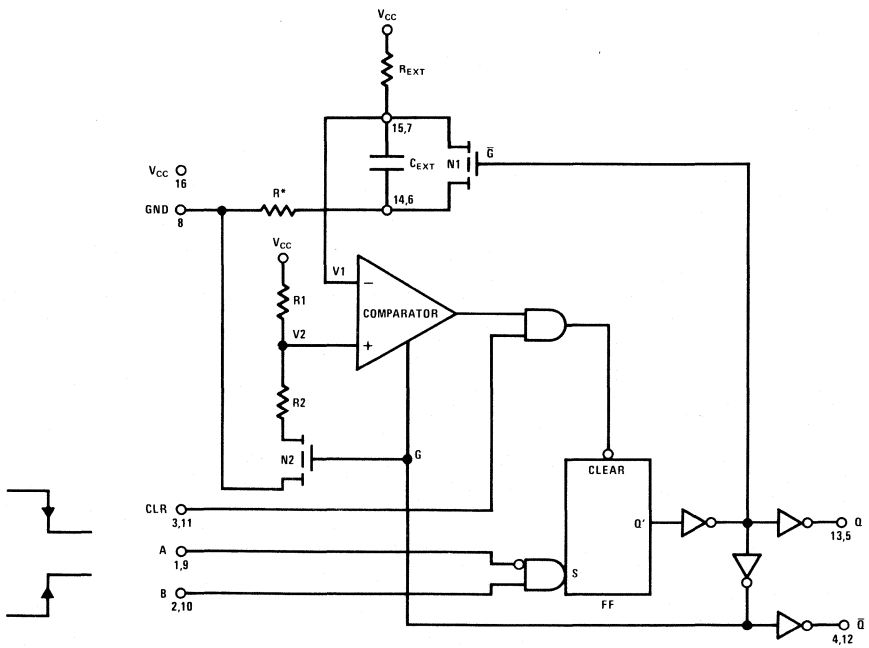


FIGURE 1. Monostable Multivibrator Logic Diagram

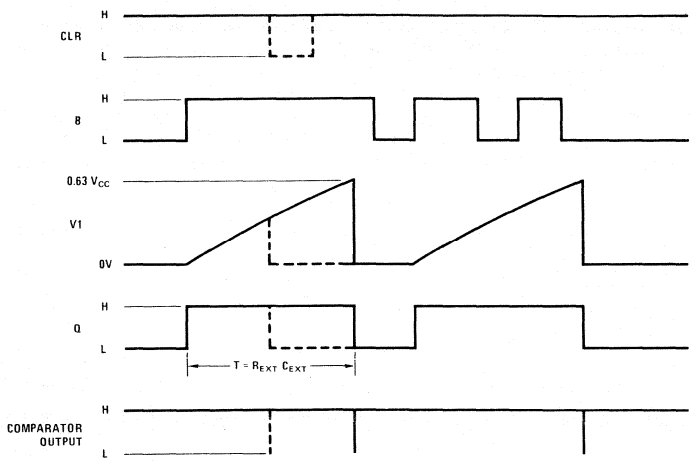


FIGURE 2. One-Shot Timing Diagram

is reset independent of all other inputs. *Figure 2* also shows that once triggered, the output is independent of any transitions on B (or A) until the cycle is complete.

The output pulse width is determined by the following equation:

$$V1 = V_{CC}\ (1 - e^{-T/R_{EXT}\,C_{EXT}}) = 0.63\ V_{CC} \qquad (1)$$

Solving for t gives:

$$T = R_{EXT}\ C_{EXT}\ \ln (1/0.37) = R_{EXT}\ C_{EXT} \qquad (2)$$

A word of caution should be given in regards to the ground connection of the external capacitor (C_{EXT}). It should always be connected as shown in *Figure 1* to pin 14 or 6 and never to pin 8. This is important because of the parasitic resistor R*. Because of the large discharge current through R*, if the capacitor is connected to pin 8, a four layer diode action can result causing the circuit to latch and possibly damage itself.

ACCURACY

There are many factors which influence the accuracy of the one-shot. The most important are:

a. Comparator input offset
b. Comparator gain
c. Comparator time delay
d. Voltage divider R1, R2
e. Delays in logic elements
f. ON impedance of N1 and N2
g. Leakage of N1
h. Leakage of C_{EXT}
i. Magnitude of R_{EXT} and C_{EXT}

The characteristics of C_{EXT} and R_{EXT} are, of course, not determined by the characteristics of the one-shot. In order to establish the accuracy of the one-shot, devices were tested using an external resistance of 10 kΩ and various capacitors. A resistance of 10 kΩ was chosen because the leakage and ON impedance of transistor N1 have a minimal effect on accuracy with this value of resistance.

Two values of C_{EXT} were chosen, 1000 pF and 0.1μF. These values give pulse widths of 10μs and 1000μs with R_{EXT} = 10 kΩ.

Figures 3 and 4 show the resulting distributions of pulse widths at 25°C for various power supply voltages. *Because propagation delays, at the same power supply voltage, are the same independent of pulse width, the shorter the pulse width the more the accuracy is*

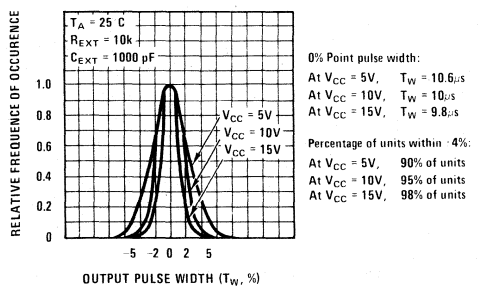


FIGURE 3. Typical Pulse Width Distribution for 10μs Pulse.

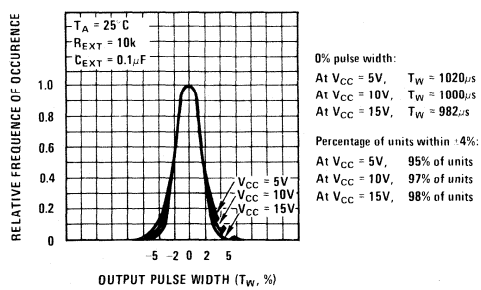


FIGURE 4. Typical Pulse Width Distribution for 1000μs Pulse.

affected by propagation delay. *Figures 3 and 4* clearly show this effect. As pointed out in application note AN-90, 54C/74C Family Characteristics, propagation delay is a function of V_{CC}. *Figure 3*, (Pulse Width = 10μs) shows much greater variation with V_{CC} than *Figure 4* (Pulse Width = 1000μs). This same information is shown in *Figures 5 and 6* in a different format. In

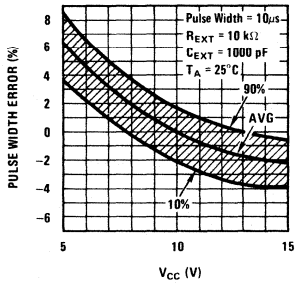


FIGURE 5. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 10μs).

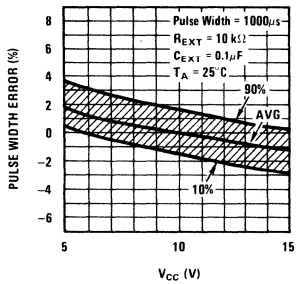


FIGURE 6. Typical Percentage Deviation from V_{CC} = 10V Value vs V_{CC} (PW = 1000μs).

these figures the percent deviation from the average pulse width at 10V V_{CC} is shown vs V_{CC}. In addition to the average value the 10% and 90% points are shown. These percentage points refer to the statistical distribution of pulse width error. As an example, at V_{CC} = 10V for 10μs pulse width, 90% of the devices have errors of less than +1.7% and 10% have errors less than −2.1%. In other words, 80% have errors between +1.7% and −2.1%.

The minimum error can be obtained by operating at the maximum V_{CC}. A price must be paid for this and this price is, of course, increased power dissipation.

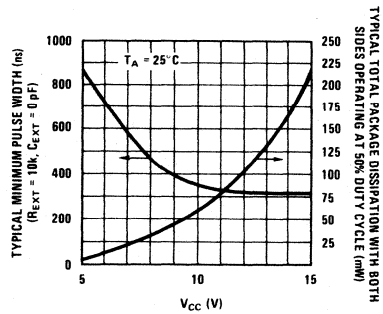


FIGURE 7. Typical Minimum Pulse Width and Power Dissipation vs V_{CC}.

Figure 7 shows typical power dissipation vs V_{CC} operating both sides of the one-shot at 50% duty cycle. Also shown in the same figure is typical minimum pulse width vs V_{CC}. The minimum pulse width is a strong function of internal propagation delays. *It is obvious from these two curves that increasing V_{CC} beyond 10V will not appreciably improve inaccuracy due to propagation delay but will greatly increase power dissipation.*

Accuracy is also a function of temperature. To determine the magnitude of its effects the one-shot was tested at temperature with the external resistance and capacitance maintained at 25°C. The resulting variation is shown in *Figures 8 and 9.*

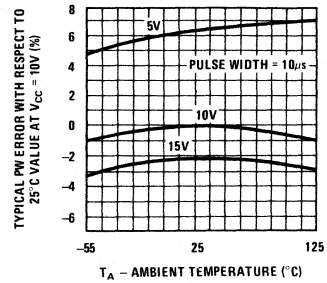


FIGURE 8. Typical Pulse Width Error vs Temperature (PW = 10μs).

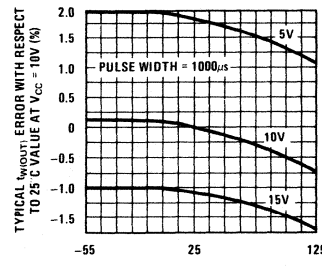


FIGURE 9. Typical Pulse Width Error vs Temperature (PW = 1000μs).

Up to this point the external timing resistor, R_{EXT}, has been held fixed at 10 kΩ. In actual applications other values may be necessary to achieve the desired pulse width. The question then arises as to what effect this will have on accuracy.

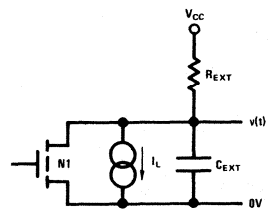


FIGURE 10.

As R_{EXT} becomes larger and larger the leakage current on transistor N1 becomes an ever increasing problem. The equivalent circuit for this leakage is shown in *Figure 10.*

v(t) is given by:

$$v(t) = (V_{CC} - I_L\ R_{EXT})\ (1 - e^{-t_L/R_{EXT}\ C_{EXT}})$$

As before, when v(t) = 0.63 V_{CC}, the output will reset. Solving for t_L gives:

$$t_L = R_{EXT}\ C_{EXT}\ \ell n\left(\frac{V_{CC} - I_L\ R_{EXT}}{0.37\ V_{CC} - I_L\ R_{EXT}}\right) \qquad (3)$$

Using T as defined in Equation 2 the pulse width error is:

$$\text{PW Error} = \frac{t_L - T}{T} \times 100\%$$

Substituting Equations 2 and 3 gives:

$$\text{PW Error} = \frac{R_{EXT}\,C_{EXT}\,\ell n\left(\frac{V_{CC} - I_L\ R_{EXT}}{0.37\ V_{CC} - I_L\ R_{EXT}}\right) - R_{EXT}C_{EXT}\,\ell n(1/0.37)}{R_{EXT}\ C_{EXT}\ \ell n\,(1/0.37)}$$

PW Error is plotted in *Figure 11* for V_{CC} = 5, 10 and 15V. As expected, decreasing V_{CC} causes PW Error to increase with fixed I_L. Note that the leakage current, although here assumed to flow through N1, is general and could also be interpreted as leakage through C_{EXT}. See MM54C221/MM74C221 data sheet for leakage limits.

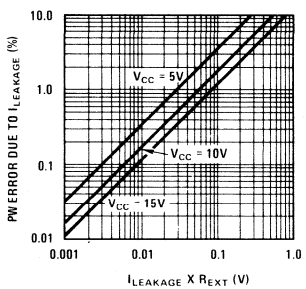


FIGURE 11. Percentage Pulse Width Error Due to Leakage.

To demonstrate the usefulness of *Figure 11* an example will be most helpful. Let us assume that N1 has a leakage of 250 x 10^{-9} amps, C_{EXT} has leakage of 150 x 10^{-9} amps, output pulse width = 0.1 seconds and V_{CC} = 5V. What R_{EXT} C_{EXT} should be used to guarantee an error due to leakage of less than 5%.

From *Figure 11* we see that to meet these conditions $R_{EXT}\ I_L < 0.14V$.

Then:

$$R_{EXT} < 0.14/(250 + 150) \times 10^{-9}$$

$$< 350\ k\Omega$$

Choosing standard component values of 250 kΩ and 0.004μF would satisfy the above conditions.

We have just defined the limitation on the maximum size of R_{EXT}. There is a corresponding limit on the minimum size that R_{EXT} can assume. This is brought about because of the finite ON impedance of N1. As R_{EXT} is made smaller and smaller the amount of voltage across N1 becomes significant. The voltage across N1 is:

$$V_{N1} = V_{CC}\ r_{ON}/(R_{EXT} + r_{ON}) \qquad (4)$$

The output pulse width is defined by:

$$v\ (t_O) = (V_{CC} - V_{N1})\ (1 - e^{-t_O/R_{EXT}\ C_{EXT}}) + V_{N1} = 0.63\ V_{CC}$$

Solving for t_O gives:

$$t_O = R_{EXT}\ C_{EXT}\ \ell n\left(\frac{V_{CC} - V_{N1}}{0.37\ V_{CC}}\right)$$

Pulse Width Error is then:

$$\text{PW Error} = \frac{t_O - T}{T} \times 100\%$$

Substituting Equations 2 and 4 gives:

$$= \frac{R_{EXT}\ C_{EXT}\ \ell n\left(\frac{V_{CC} - V_{N1}}{0.37\ V_{CC}}\right) - R_{EXT}\ C_{EXT}\ \ell n\,(1/0.37)}{R_{EXT}\ C_{EXT}\ \ell n\,(1/0.37)}$$

This function is plotted in *Figure 12* for r_{ON} of 50Ω, 25Ω and 16.7Ω. These are the typical values of r_{ON} for a V_{CC} of 5V, 10V and 15V respectively.

As an example, assume that the pulse width error due to r_{ON} must be less than 0.5% operating at V_{CC} = 5V. The typical value of r_{ON} for V_{CC} = 5V is 50Ω. Referring to

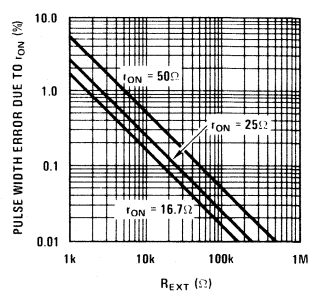
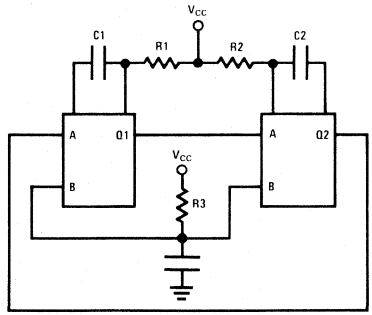


FIGURE 12. Percentage Pulse Width Error Due to Finite r_{ON} of Transistor N1 vs R_{EXT}.

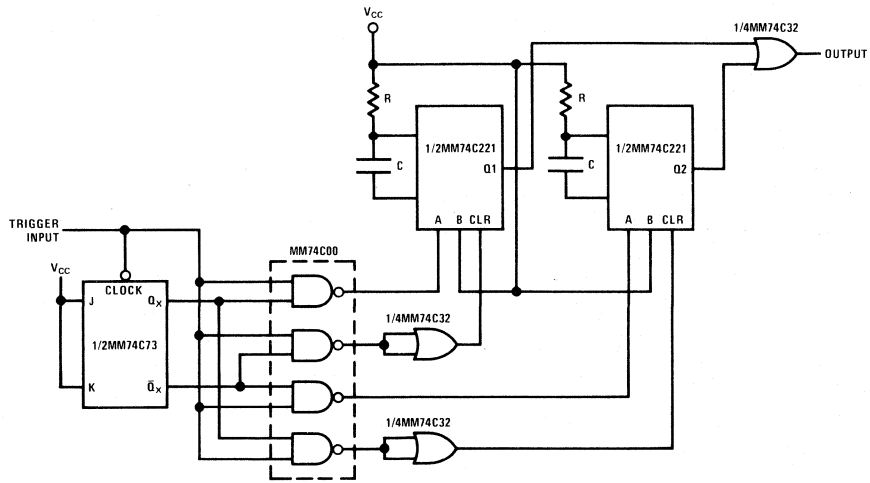
the 50Ω curve in *Figure 12*, R_{EXT} must be greater than 10 kΩ to maintain this accuracy. At V_{CC} = 10V, R_{EXT} must be greater than 5 kΩ as can be seen from the 25Ω curve in *Figure 12*.

Although clearly shown on the MM54C221/MM74C221 data sheet, it is worthwhile, for the sake of clarity, to point out that the parasitic capacitance between pins 7 (15) and 6 (14) is typically 15 pF. This capacitor is in parallel with C_{EXT} and must be taken into account when accuracy is critical.

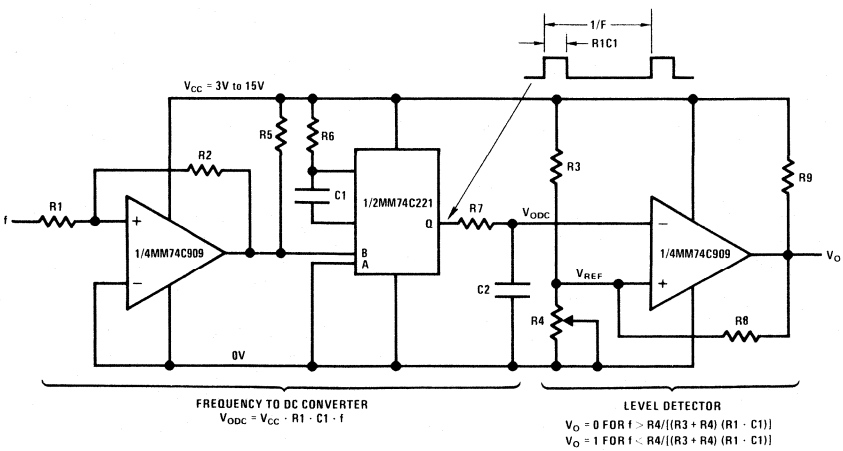
TYPICAL APPLICATIONS



Basic One-Shot Oscillator

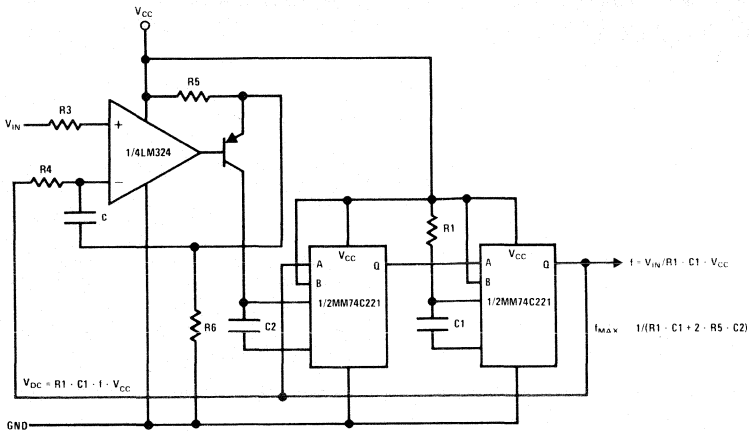


Retriggerable One-Shot

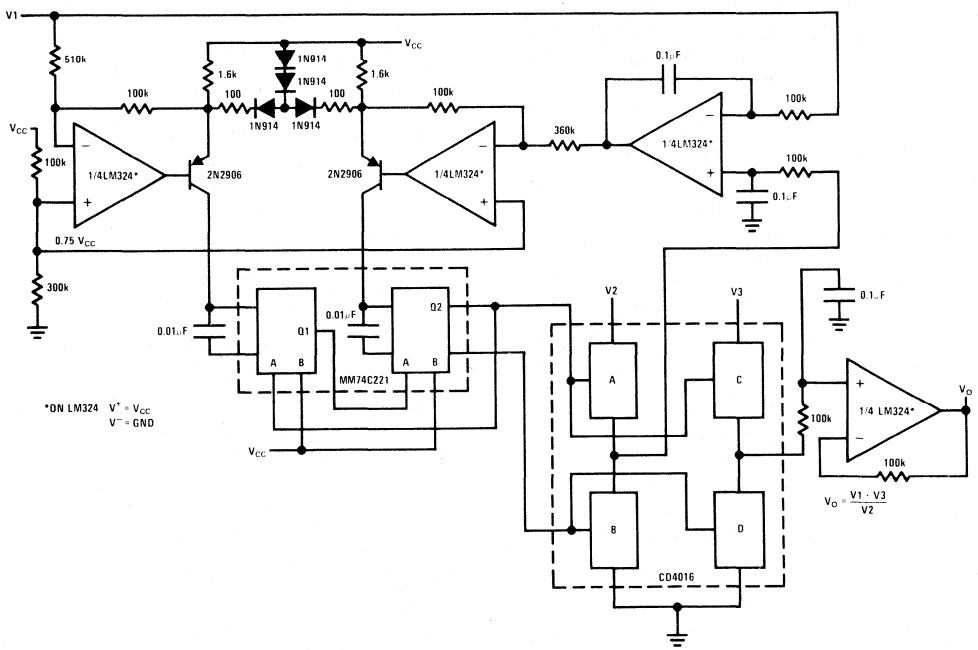


Frequency Magnitude Comparator

TYPICAL APPLICATIONS (Continued)



Linear VCO



Analog Multiplier/Divider

CMOS Schmitt Trigger —a Uniquely Versatile Design Component

National Semiconductor
Application Note 140
Gerald Buurma

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - Thresholds are typically symmetrical to 1/2 V_{CC}
  - Outputs source and sink equal currents
  - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC}-V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above 1/2 V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold is reached.

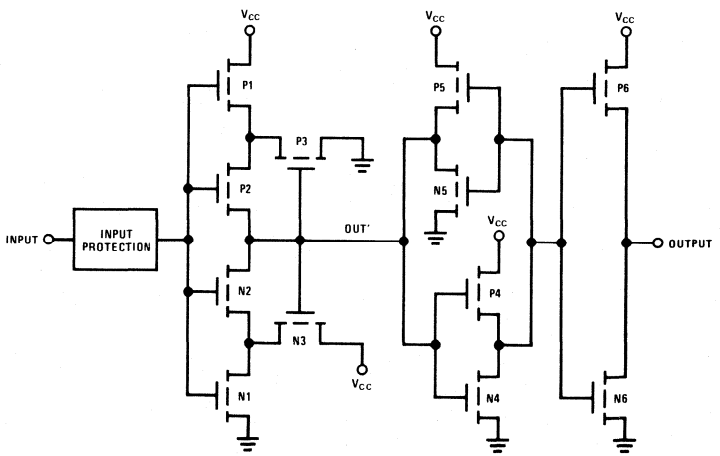


FIGURE 1. CMOS Schmitt Trigger

Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360μA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2*; the guaranteed trip point range is shown in *Figure 3.*

WHAT HYSTERESIS CAN DO FOR YOUR

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is doen to prevent slicing level distortion. If a 4μs wide signal is sent down a transmission line a 4μs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4μs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

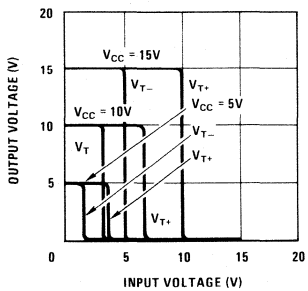


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages.

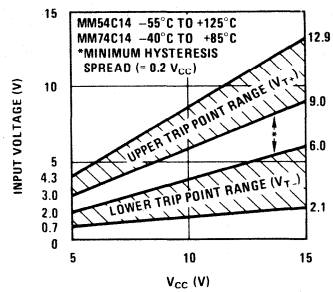


FIGURE 3. Guaranteed Trip Point Range.

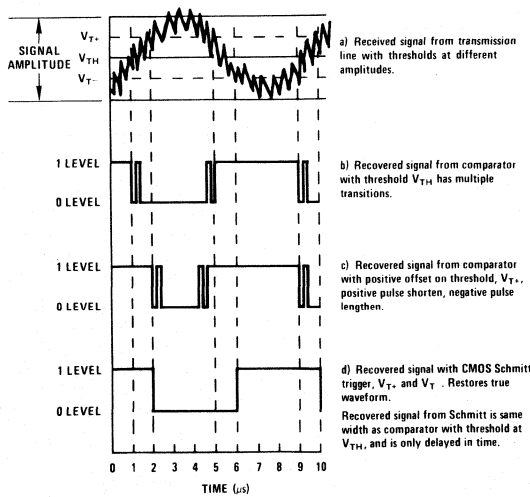
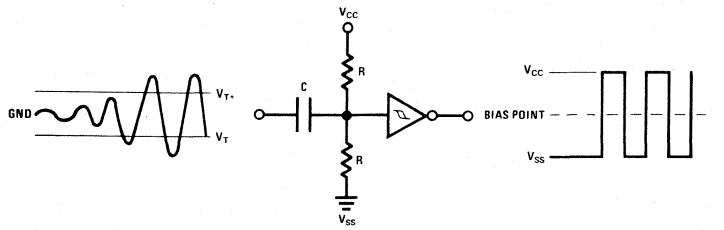
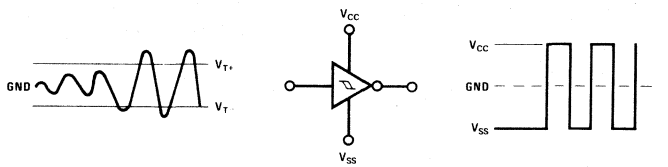


FIGURE 4. CMOS Schmitt Trigger Ignores Noise



a) Capacitor impedance at lowest operating frequency should be much less than R R = 1/2 R.



b) By using split supply (±1.5 to ±7.5) direct interface is achieved.

FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection.

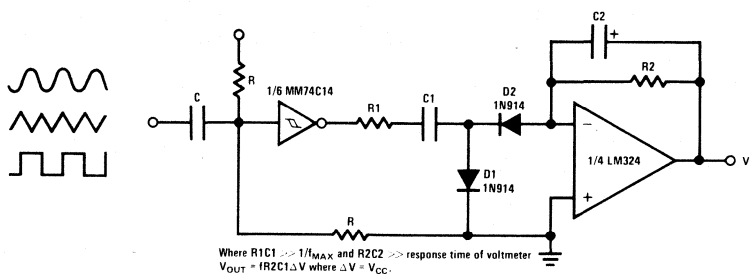


FIGURE 6. Diode Dump Tach Accepts any Input Waveform.

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a $10^{12}\Omega$ typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 >> t_{pd0} + t_{pd1}$.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

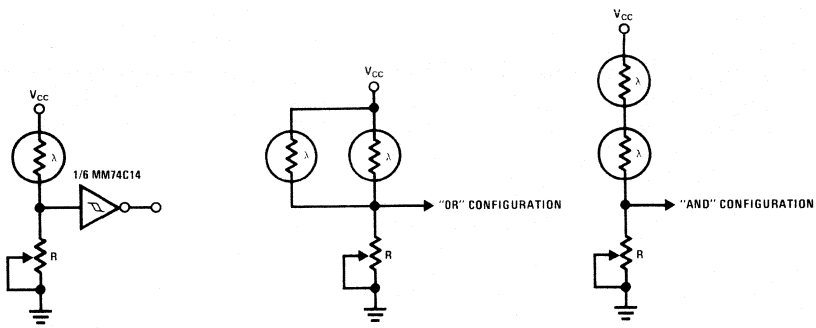


FIGURE 7. Light Activated Switch couldn't be Simpler. The Input Voltage Rises as Light Intensity Increases, when V_{T+} is Reached, the Output will go Low and Remain Low until the Intensity is Reduced Significantly.

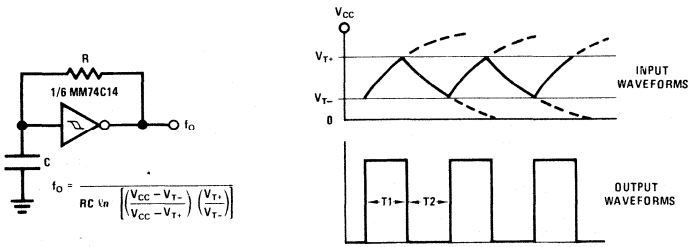


FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into Six Low Power Oscillators. Balanced Input and Output Characteristics give the Output Frequency a Typically 50% Duty Cycle.

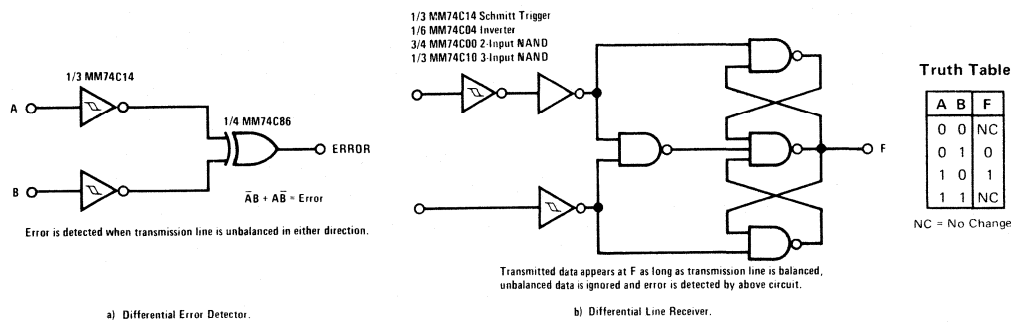


FIGURE 9. Increase Noise Immunity by using the CMOS Schmitt Trigger to Demodulate a Balanced Transmission Line.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} +0.3V and ground −0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_s and speeding up capacitor C_s. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})\ R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to V_{IN} So,

$$\frac{d\ f_O}{d\ V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\ RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

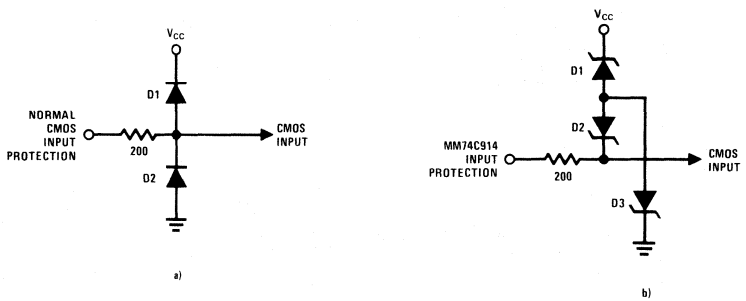


FIGURE 10. Input Protection Diodes, in a) Normally Limit the Input Voltage Swing to 0.3V above V_{CC} and 0.3V below Ground. In b) D2 or D1 is Reverse Biased Allowing Input Swings of 25V above Ground or 25V below V_{CC}.

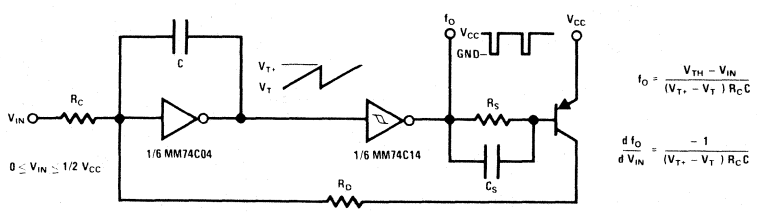


FIGURE 11. Linear CMOS (Voltage Controlled Oscillator)

The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12.* A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{SINK\ INVERTER} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non 5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.

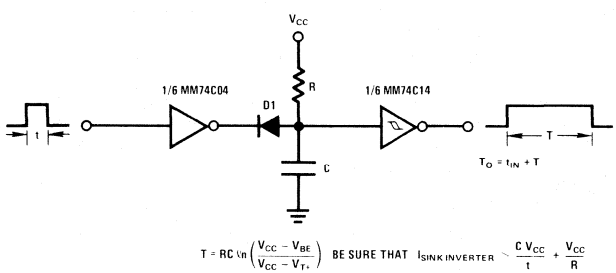


FIGURE 12. Pulse Stretcher. A CMOS Inverter Discharges a Capacitor, a Blocking Diode allows Charging through R only. Schmitt Trigger Output goes Low after the RC Delay.

Designing with MM74C908, MM74C918 Dual High Voltage CMOS Drivers

National Semiconductor
Application Note 177
Jen-yen Huang

INTRODUCTION

By combining the merits of both CMOS and bipolar technologies on a single silicon chip, the MM74C908, MM74C918 provides the following distinguished features as general purpose high voltage drivers.

- Wide supply voltage range (3V to 18V)
- High noise immunity (typ 0.45 V_{CC})
- High input impedance (typ $10^{12}\Omega$)
- Extremely low standby power consumption (typ 750 nW at 15V)
- Low output "ON" resistance (typ 8Ω)
- High output drive capability ($I_{OUT} \geq 250$ mA at $V_{OUT} = V_{CC} - 3V$, and $T_j = 65°C$)
- High output "OFF" voltage (typ 56V at 200 μA)

Among these, the first 4 are typical and unique characteristics of CMOS technology which are fully utilized in this circuit to achieve all the design advantages in a typical CMOS system.

The high output currents and low "ON" resistance are achieved through the use of an NPN Darlington pair at the output stage.

The MM74C908 is housed in an 8-lead epoxy dual-in-line package, which can dissipate at least 1.14W. The higher power version, MM74C918, comes in a 14-lead epoxy dual-in-line package, with power capability up to a minimum of 2.27W.

The circuitry for each of the 2 identical sections is shown in *Figure 1*.

With both inputs sitting at logical "1" level, the output of the inverter is also at logical "1", which prevents the P-channel transistor from being turned "ON"; therefore, the output is in its "OFF" state. Only a small amount of leakage current can flow.

On the other hand, when one or both of the inputs is at logical "0" level, the output of the inverter is also at logical "0", which turns on the P-channel transistor and, hence, the Darlington pair.

POWER CONSIDERATION

To assure junction temperature of 150°C or less, the on-chip power consumption must be limited to within the power handling capability of the packages. In *Figure 2*, the maximum power dissipation on-chip is shown as a function of ambient temperature for both MM74C908 and MM74C918. These curves are generated from (1) at $T_j = T_{j(MAX)} = 150°C$.

$$T_j = T_A + P_D \theta_{jA} \quad (1)$$

where T_j = junction temperature
T_A = ambient temperature
P_D = power dissipation
θ_{jA} = thermal resistance between junction and ambient

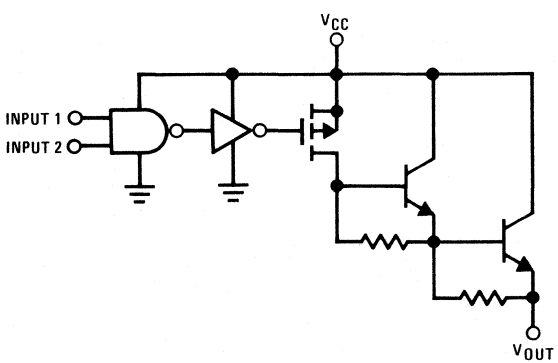


FIGURE 1

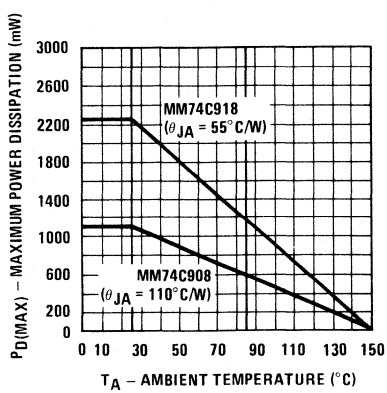


FIGURE 2. Maximum Power Dissipation vs Ambient Temperature

A general application circuit for the MM74C908, MM74C918 is as shown in *Figure 3*.

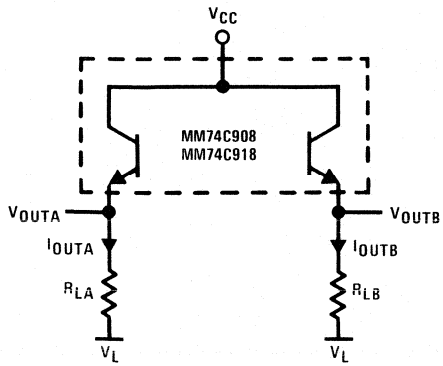


FIGURE 3

For both sections A and B;

$$I_{OUT} = \frac{V_{CC} - V_L}{R_{ON} + R_L} \quad (2)$$

The device "ON" resistance, R_{ON}, is a function of junction temperature, T_j. The worst-case R_{ON} as a function of T_j is given in (3).

$$R_{ON} = 9\ [1 + 0.008\ (T_j - 25)] \quad (3)$$

The total power dissipation in the device also consists of normal CMOS power terms (due to leakage current, internal capacitance, switching etc.) which are insignificant compared to the power dissipated at the output stages. Thus, the output power term defines the allowable limits of operation and is given by:

$$P_D = P_{DA} + P_{DB} = I^2_{OUTA} \cdot R_{ON} + I^2_{OUTB} \cdot R_{ON} \quad (4)$$

Given R_{LA} and R_{LB}, (1), (2), (3), (4) can be used to calculate P_D, T_j, etc. through iteration.

For example, let $V_L = 0V$, $V_{CC} = 10V$, $R_{LA} = 100\Omega$, $R_{LB} = 50\Omega$, $T_A = 25°C$, $\theta_{jA} = 110°C/W$.

Assume:

$R_{ON} = 12.28\Omega$

By (2):

$$I_{OUTA} = \frac{10}{12.28 + 100} = 0.089A$$

$$I_{OUTB} = \frac{10}{12.28 + 50} = 0.161A$$

By (4):

$$P_D = (0.089)^2 \cdot 12.28 + (0.161)^2 \cdot 12.28 = 0.41W$$

By (1):

$T_j = 70.5°C$

And by (3):

$R_{ON} = 12.28\Omega$

DESIGN TECHNIQUE

In a typical design, R_L must be chosen to satisfy the load requirement (e.g., a minimum current to turn on a relay) and at the same time, the power consumed in the driver package must be kept below its maximum power handling capability.

To minimize the design effort, a graphical technique is developed, which combines all the parameters in one plot, which can be used efficiently to obtain an optimal design.

Assume $T_A = 25°C$ and that both sections of the MM74C908 in *Figure 3* are operating under identical conditions. The maximum allowable package dissipation is:

$$P_D = 2\ (V_{CC} - V_{OUT}) \times I_{OUT} = \frac{1}{110}\ (150 - T_A) = 1.14W \quad (6)$$

where $T_j = 150°C$, $\theta_{jA} = 110°C/W$ are used in (1) per the data sheet.

Thus, the maximum power allowed in each section is:

$$P_D = (V_{CC} - V_{OUT}) \times I_{OUT} = 0.57W$$

A constant power curve $P_D = 0.57W$ can then be plotted as shown in *Figure 4*. The circuit must operate below this curve. Any voltage-current combination beyond it (in the shaded region) will not guarantee T_j to be lower than 150°C.

For any given R_L, a load line (7) can be superimposed on *Figure 4*.

$$I_{OUT} = \frac{1}{R_L}\ (V_{CC} - V_L) - \frac{1}{R_L}\ (V_{CC} - V_{OUT}) \quad (7)$$

The slope of this load line is $-1/R_L$ and it intersects with the vertical and horizontal axes at $1/R_L\ (V_{CC} - V_L)$ and $V_{CC} - V_L$ respectively.

Given V_{CC} and V_L, a minimum R_L can be obtained by drawing the load line tangent to the constant power curve. In *Figure 4*, at $V_{CC} - V_L = 5V$ the line intersects I_{OUT} axis at $I_{OUT} = 450$ mA. Thus, $R_{L(MIN)} = 5V/450\ mA = 11.1\Omega$. Any R_L value below this will move the intersecting point up and cause a section of the load line to extend into the shaded region. Therefore, the junction temperature can exceed $T_{j(MAX)} = 150°C$ in the worst case if the circuit operates on such a section of the load line.

Whether this situation will occur or not is determined by both the value of $V_{CC} - V_L$ and the R_{ON} range of the drivers.

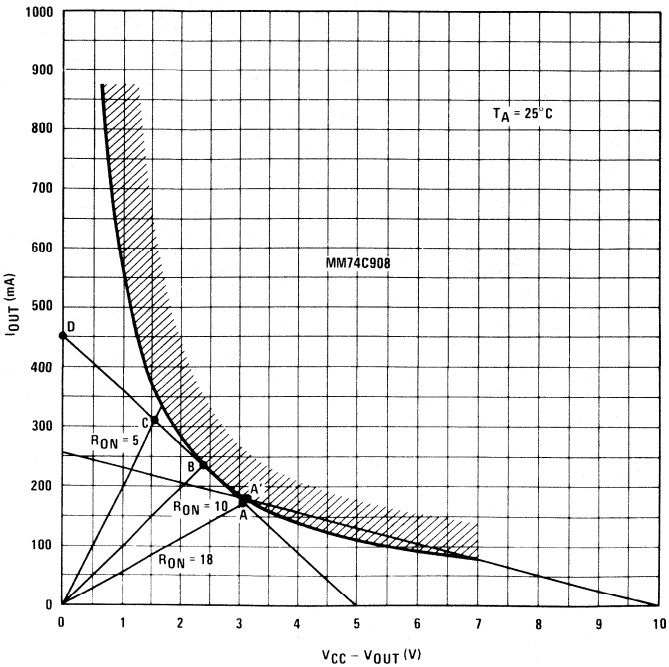


FIGURE 4

By (3), at T_j = 150°C $R_{ON(MAX)}$ = 18Ω, this is a straight line* passing through the origin with a slope of $I_{OUT}/(V_{CC} - V_{OUT})$ = 1/18 mho and intersects the load line at point A. Similarly, point B and C can be found for typical (~10Ω) and minimum (~5Ω) R_{ON} at T_j = 150°C.

For $V_{CC} - V_L$ = 5V, the tangent point falls between A and C. Hence, $R_L \geq$ 11.1Ω calculated above must be satisfied; otherwise, part of the load line within the specified R_{ON} range will extend into the shaded region and therefore, $T_j \geq$ 150°C may occur.

For $V_{CC} - V_L$ = 10V, however, a section of the load line can go beyond the P_D = 0.57W curve without affecting the safe operation of the circuit. By inspection of *Figure 4*, the reason is clear—the load line extends into the shaded region only outside of the specified R_{ON} range (to the right of point A'). Within the R_{ON} range, the load line lies below the P_D = 0.57W curve, thus, a safe operation.

To a first approximation**, the section of the load line between A and C is the operating range for the circuit at $V_{CC} - V_L$ = 5V and R_L = 11.1Ω. Hence, the available current and voltage ranges for this circuit are 310 mA $\geq I_{OUT} \geq$ 172 mA and 3.4V $\geq V_{OUT} \geq$ 1.9V, respectively.

Thus, by simply drawing no more than 3 straight lines, one obtains all of the following immediately:

1. All the necessary design information (e.g., minimum R_L, minimum available I_{OUT} and V_{OUT}, etc.)
2. Operating characteristics of the circuit as a whole, including the effect of different R_{ON} values due to process variations, thus, a better insight into the circuit operation.
3. Most importantly, a guarantee that the circuit will be operating in the safe region, ($T_j \leq$ 150°C).

For different ambient temperatures or for different power considerations, *Figure 4* can be applied by properly scaling the I_{OUT} axis. (Note that $I_{OUT} \propto T_j - T_A$ and $I_{OUT} \propto P_D$).

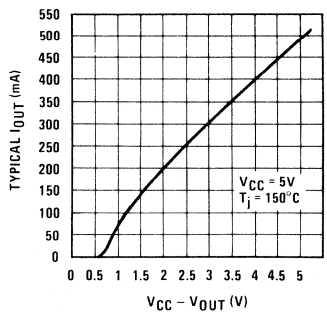


FIGURE 5. Typical I_{OUT} vs Typical V_{OUT}

*Strictly speaking, R_{ON} is a non-linear function of I_{OUT}. A typical R_{ON} characteristic at T_j = 150°C is shown in *Figure 5*. The non-linear characteristic near the origin is due to the fact that the output NPN transistor is not saturated. As soon as saturation is reached (I_{OUT} ~ 150 mA) the curve becomes a straight line which extrapolates back to the origin. For practical design purposes, it is sufficient to consider R_{ON} as a linear function of I_{OUT}.

**Note that as the operating point on the load line moves away from the P_D = 0.57W curve, (away from the tangent point in this case), the actual junction temperature drops. Therefore, at point A, for example, the device is actually running cooler than T_j = 150°C, even in the worst case. Hence, R_{ON} value drops below 18Ω and the actual operating point is slightly different from A.

To further simplify the design, a family of such curves has been generated as shown in *Figure 6*. Each of these curves corresponds to a particular T_A and P_D (per driver) as indicated, and similar to the P_D = 0.57W curve in *Figure 4*, is generated from (6) by using appropriate T_A values. The application of these curves is illustrated as follows:

Example 1

1. In *Figure 3*, assume that the two drivers in the MM74C908 package are to operate under identical conditions. Find minimum R_L at T_A = 25°C, 45°C, 65°C and 85°C for both $V_{CC} - V_L$ = 5V and $V_{CC} - V_L$ = 10V.

   Then plot $R_{L(MIN)}$ vs T_A.

   a) $V_{CC} - V_L$ = 5V

   By constructing the load lines tangent to the curves for T_A = 25°C, 45°C, 65°C and 85°C, $R_{L(MIN)}$ for each case can be obtained through the vertical coordinate for the intersection points as shown in *Figure 6*. These are calculated in Table I.

   Note that the same results (within graphical error) can be obtained analytically by letting $dR_L/dR_{ON} = 0$. It can be shown that

$$R_{L(MIN)} = \frac{(V_{CC} - V_L)^2}{4X \text{ (Max Power Per Driver)}} \quad (8)$$

   b) $V_{CC} - V_L$ = 10V

   The $R_{L(MIN)}$ given in (8) may not be a true minimum if the tangent point does not fall inside the specified R_{ON} region. The actual $R_{L(MIN)}$ can be obtained as shown in *Figure 7*. The calculations and results are given in Table II.

   Note that the $R_{L(MIN)}$ values in Table II are lower than those given by (8). This corresponds to the section on each of the 4 load lines in *Figure 7* which extends beyond the power limit curve at each associated temperature. However, this section on each load line is outside the specified R_{ON} range. Within the R_{ON} range, load lines are below the power limits; therefore, safe operation is guaranteed.

   The $R_{L(MIN)}$ vs T_A plot is as shown in *Figure 8*.

   All the curves generated so far are restricted to $P_D \leq 0.57W$ due to our simplifying assumption that both drivers are operating identically. In *Figure 9* a few more curves are added to account for the general situation in which only the restriction $P_{DA} + P_{DB} \leq 1.14W$ is required, (i.e., P_{DA} can be different from P_{DB}). Application of *Figure 9* is illustrated as follows:

TABLE I.

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	450	375	310	240
$R_{L(MIN)} = \frac{5}{I_{OUT} \text{ @ D1, 2, 3, 4}}$ (Ω)	11.1	13.3	16.1	20.8

TABLE II.

T_A	25°C	45°C	65°C	85°C
I_{OUT} @ D1, 2, 3, 4 (mA)	261	230	197	166
$R_{L(MIN)} = \frac{10}{I_{OUT} \text{ @ D1, 2, 3, 4}}$ (Ω)	38.3	43.5	50.8	60.2

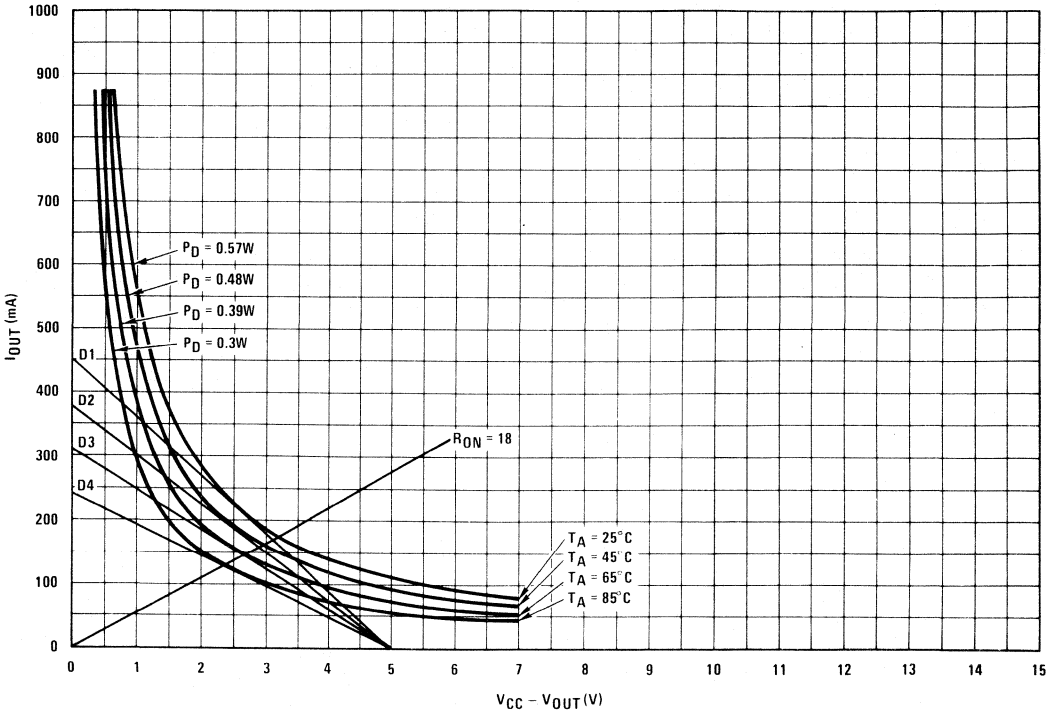


FIGURE 6

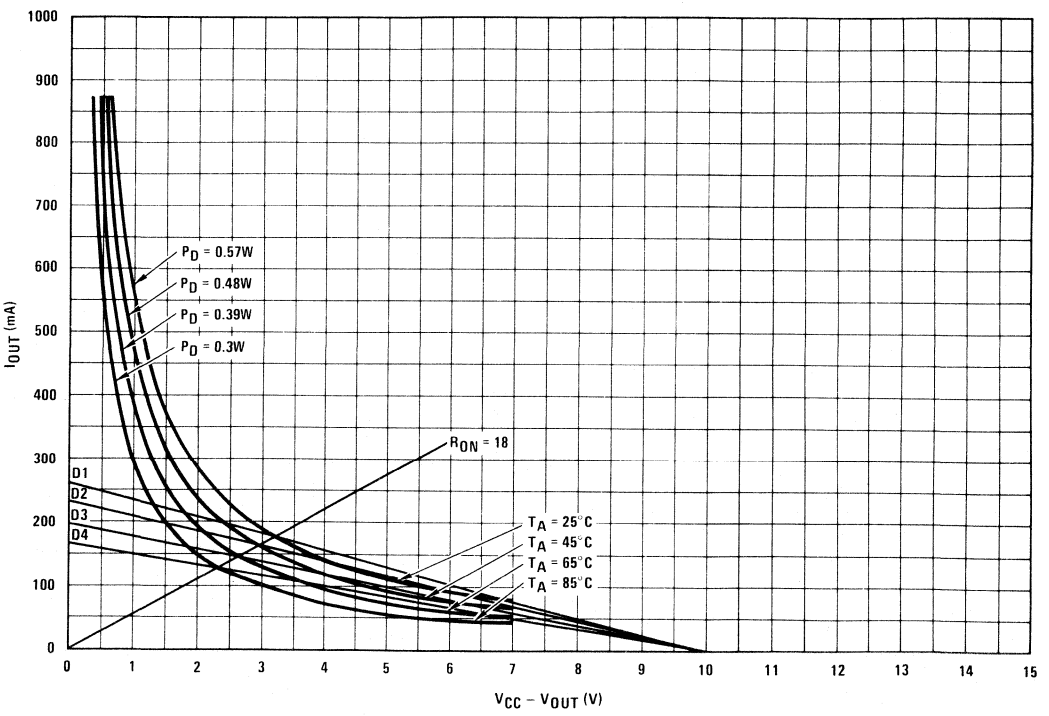


FIGURE 7

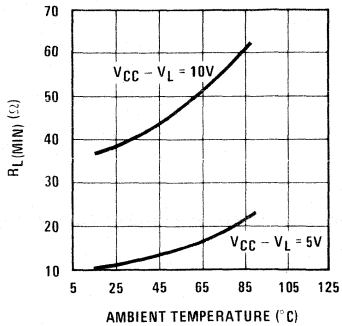


FIGURE 8

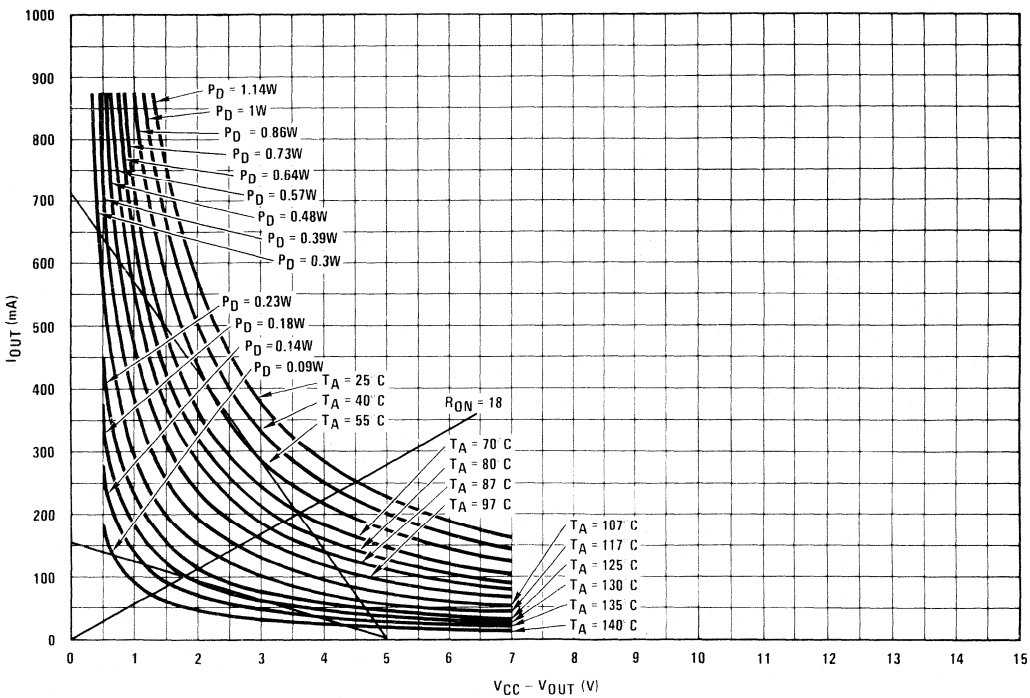


FIGURE 9

Example 2

In *Figure 3*, assume that driver A has to deliver 200 mA to its load while driver B needs only 100 mA. Design R_{LA} and R_{LB} for $V_{CC} - V_L = 5V$.

By inspection of *Figure 4*, units with high R_{ON} values will not be able to deliver 200 mA. However, since section B does not need the same amount of drive, we can reduce the power consumed in this section to compensate for the higher power (> 0.57W) required in section A.

The design procedure follows:

Section A

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 200$ mA.
2. This load line intersects the I_{OUT} axis at $I_{OUT} = 710$ mA and is tangent to $P_{DA} \simeq 0.9W$ curve, thus $R_{LA} \cong 5V/710\ mA = 7.1\Omega$ will guarantee both $P_{DA} \leq 0.9W$ and $I_{OUTA} \geq 200$ mA.

Section B

1. Draw a load line intersecting $R_{ON} = 18\Omega$ line at $I_{OUT} = 100$ mA.
2. Similar to (2) above, it is seen immediately that $R_{LB} \cong 5V/150\ mA = 33.3\Omega$ will guarantee $I_{OUTB} \geq 100$ mA and $P_{DB} \leq 0.18W$.

Since $P_{DA} + P_{DB} \leq 0.9 + 0.18 < 1.14W$

$R_{LA} = 7.1\Omega$
$R_{LB} = 33.3\Omega$

satisfy all the requirements in this problem.

The design in Example 2 illustrated the simple and straight-forward use of the curves and the result meets all the problem requirements. However, it should be noted that there is not much design margin left for tolerance in resistances and other circuit parameters. The reason is obvious—we are pushing at the power limit of the MM74C908 package—and the solutions are simple:

a) Increase V_{CC} supply
b) Use the higher power package MM74C918.

The design for higher V_{CC} is identical to that in Example 2 and will not be repeated here.

For the 14-lead higher power (2.27W) MM74C918, $\theta_{jA} = 55°C/W$, this is exactly half that of the 8-lead MM74C908. Therefore, by scaling the I_{OUT} axis by a factor of 2, the same family of curves in *Figure 9* can be applied directly. This is shown in *Figure 10*. (Note that the slope of the $R_{ON} = 18\Omega$ line has been adjusted to the new scale).

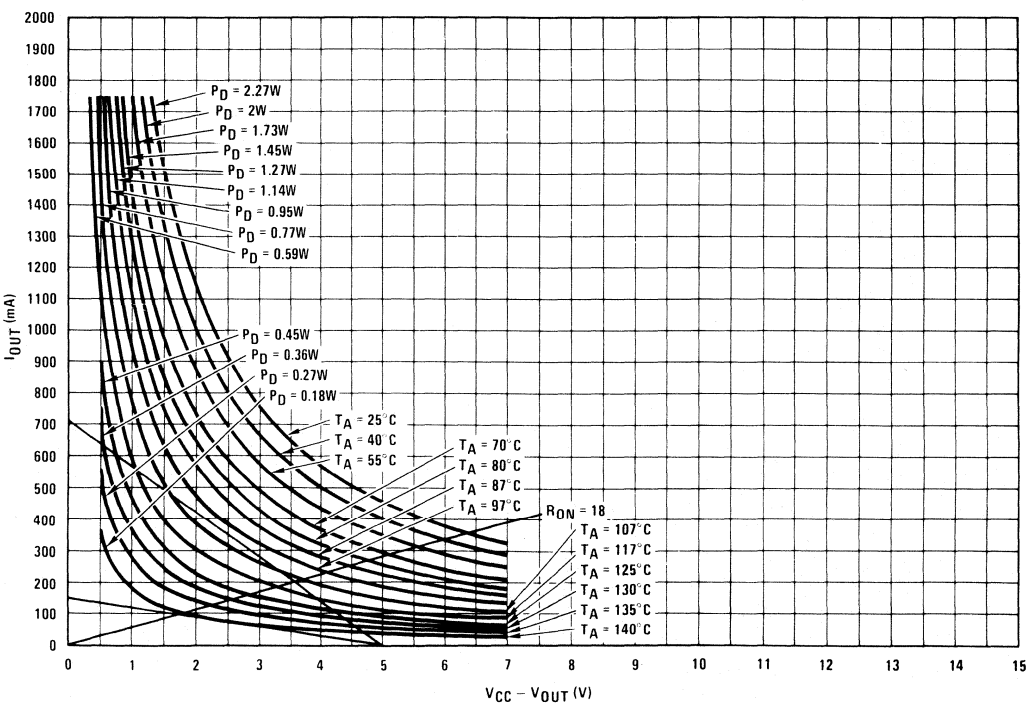


FIGURE 10

By drawing the same load lines, it is found that:

$R_{LA} \cong 5V/710\ mA = 7.1\Omega$
guarantees $P_{DA} \leq 0.9W$

and

$R_{LB} \cong 5V/150\ mA = 33.3\Omega$
guarantees $P_{DB} \leq 0.18W$

$P_{DA} + P_{DB} \leq 1.08W$

which is way below the maximum power 2.27W available. Therefore, both R_{LA} and R_{LB} can be lowered to account for tolerance in the resistors. Consider specifically the following example:

Example 3

Assume driver A, B of the MM74C918 have to deliver 250 mA and 150 mA, respectively, to its load. Design R_{LA} and R_{LB} at $V_{CC} - V_L = 10V$.

Driver A

1. In *Figure 11*, draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 250$ mA.
2. This load line intersects the I_{OUT} axis at 450 mA. Thus, by inspection $R_{LA} \cong 10V/450\ mA \cong 22.2\Omega$ guarantees $P_{DA} \leq 1.14W$.

Driver B

1. Draw the load line intersecting $R_{ON} = 18\Omega$ at $I_{OUT} = 150$ mA.
2. This load line intersects the I_{OUT} axis at 210 mA. Thus, by inspection $R_{LB} \cong 10V/210\ mA = 47.6\Omega$ guarantees $P_{DB} \leq 0.4W$.

Since $P_{DA} + P_{DB} \leq 1.14 + 0.4 = 1.8W$, while the package is capable of delivering 2.27W, both R_{LA} and R_{LB} can be lower than the above values and the circuit still operates safely. By picking the closest standard resistance values:

$R_{LA} = 20\Omega$
$R_{LB} = 43\Omega$

For 5% tolerance in these values,

$19\Omega \leq R_{LA} \leq 21\Omega$
$40.85\Omega \leq R_{LB} \leq 45.15\Omega$

Thus:

$$I_{OUTA(MIN)} \geq \frac{10V}{18\Omega + 21\Omega} = 256.4\ mA > 250\ mA$$

$$I_{OUTB(MIN)} \geq \frac{10V}{18\Omega + 45.15\Omega} = 158.3\ mA > 150\ mA$$

$$P_{DA(MAX)} \leq \left(\frac{10V}{18\Omega + 19\Omega}\right)^2 \cdot 18\Omega = 1.31W$$

$$P_{DB(MAX)} \leq \left(\frac{10V}{18\Omega + 40.85\Omega}\right)^2 \cdot 18\Omega = 9.52W$$

$$P_{DA(MAX)} + P_{DB(MAX)} \leq 1.31 + 0.52 < 2.27W$$

Therefore:

$R_{LA} = 20\Omega$ (1.5W, 5%)
$R_{LB} = 43\Omega$ (1W, 5%)

will guarantee satisfactory performance of the circuit.

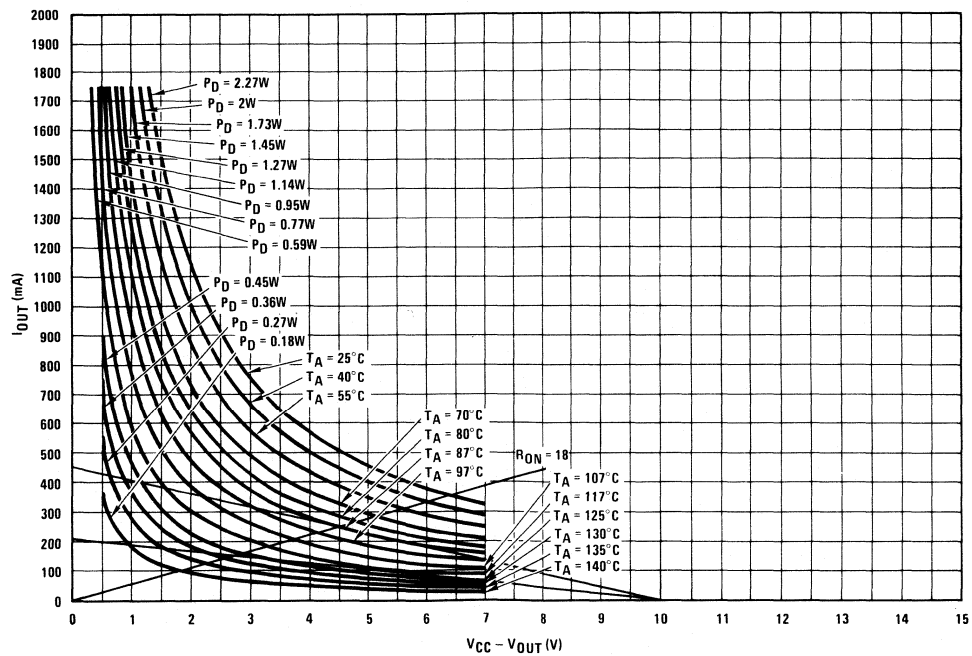


FIGURE 11

APPLICATIONS

Like most other drivers, the MM74C908, MM74C918 can be used to drive relays, lamps, speakers, etc. These are shown in *Figure 12*. (To suppress transient spikes at turn-off, a diode as shown as *Figure 12a* is recommended at the relay coil or any other inductive load.)

However, the MM74C908, MM74C918 offers a unique CMOS feature that is not available in drivers from other logic families—extremely low standby power. At V_{CC} = 15V, power dissipation per package is typically 750 nW when the outputs are not drawing current. Thus, the drivers can be sitting out on line (a telephone line, for example) drawing essentially zero current until activated—an ideal feature for many applications.

The dual feature and the NAND function of the driver design can also be used to advantage as shown in the following applications:

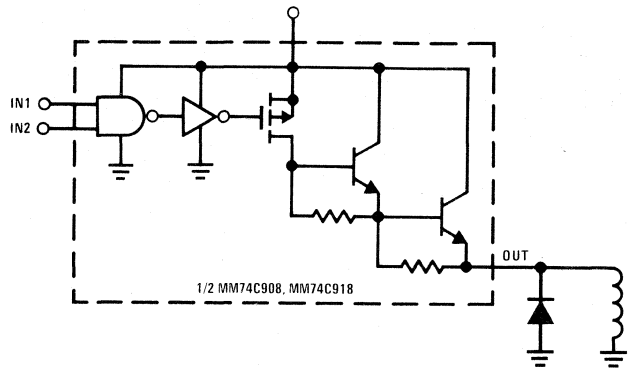


FIGURE 12a. Relay Driver

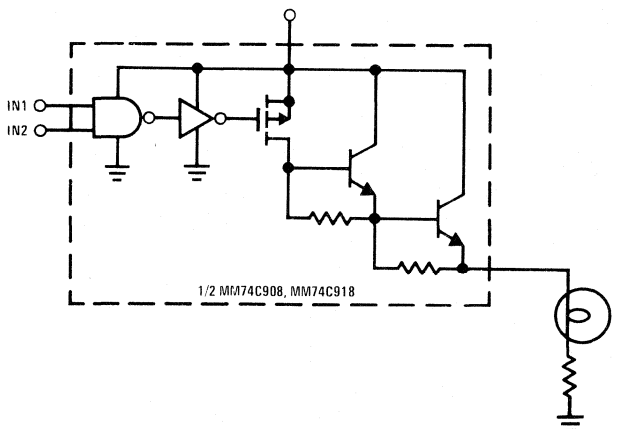


FIGURE 12b. Lamp Driver

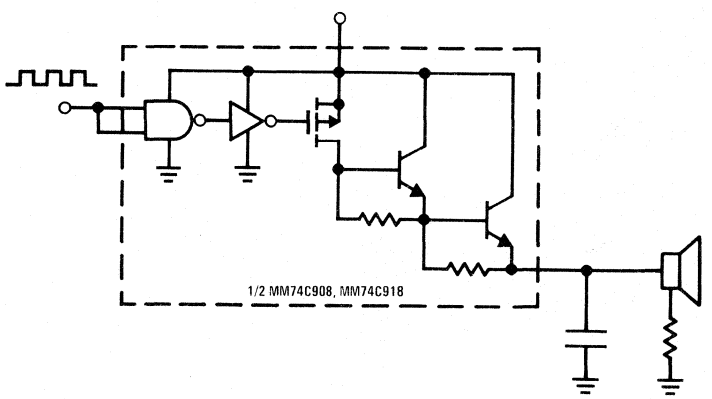


FIGURE 12c. Speaker Driver

In *Figure 13*, the 2 drivers in the package are connected as a Schmitt trigger oscillator, where R1 and R2 are used to generate hysteresis. R3 and C are the inverting feedback timing elements and R4 is the pull-down load for the first driver. Because of its current capability, the circuit can be used to drive an array of LEDs or lamps. If resistor R4 is replaced by an LED (plus a current limiting resistor), the circuit becomes a double flasher with the 2 LEDs flashing out of phase. This is shown in *Figure 14*.

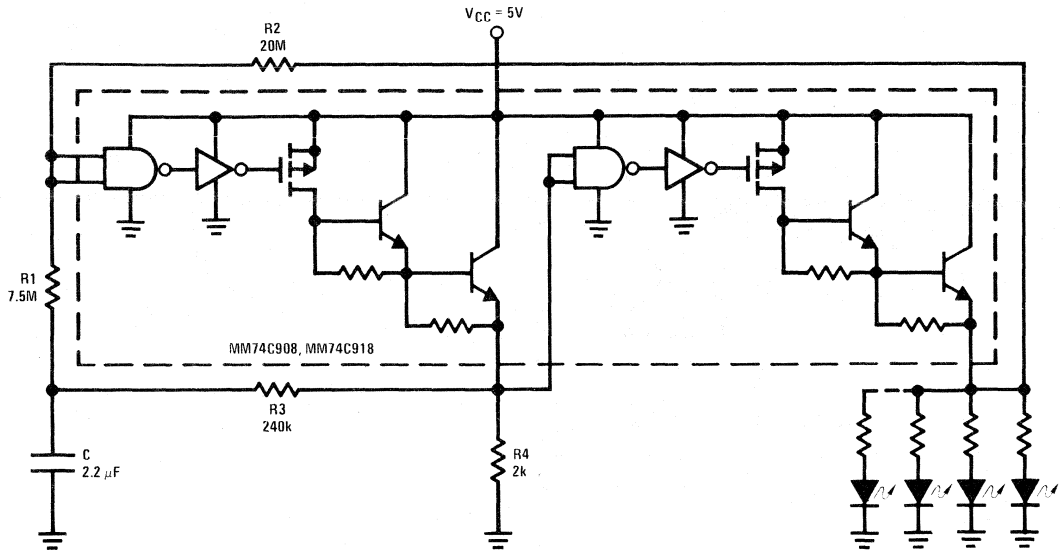


FIGURE 13. High Drive Oscillator/Flasher

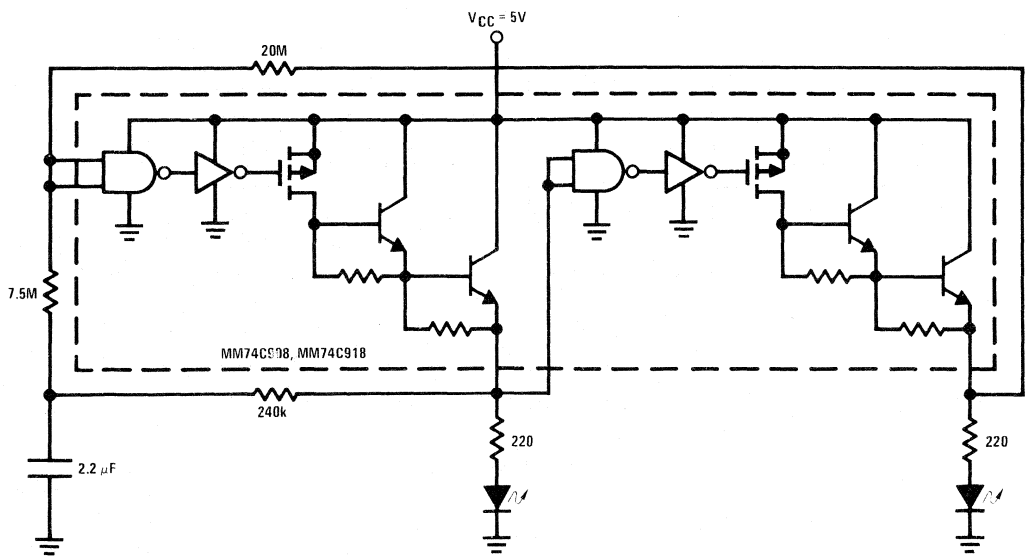


FIGURE 14. Out of Phase Double Flasher

Another oscillator circuit using only 1/2 of the package and 4 passive components is shown in *Figure 15*. Assume V_I is slightly below the input trip point, the driver is "ON" and charging both V_O and V_I until V_I reaches the trip point, V_T, when the driver starts to turn "OFF". V_O can be made much higher than V_I at this instance by adjusting the component values such that $R_fC_f >> (R_{ON}||R_L)C_L$. Since V_O is higher than V_I, V_I is still going up, although the driver is "OFF" and V_O is ramping down. The rising V_I will eventually equal to the falling V_O, and then start discharging. Then, both V_I and V_O discharge until V_I hits the trip point, V_T, again, when the driver is turned "ON", charging up V_O and subsequently V_I to complete a cycle.

This oscillator is ideal for low cost applications like the 1-package siren shown in *Figure 16*, where 1 oscillator is used as a VCO while the other is generating the voltage ramp to vary the frequency at the VCO output.

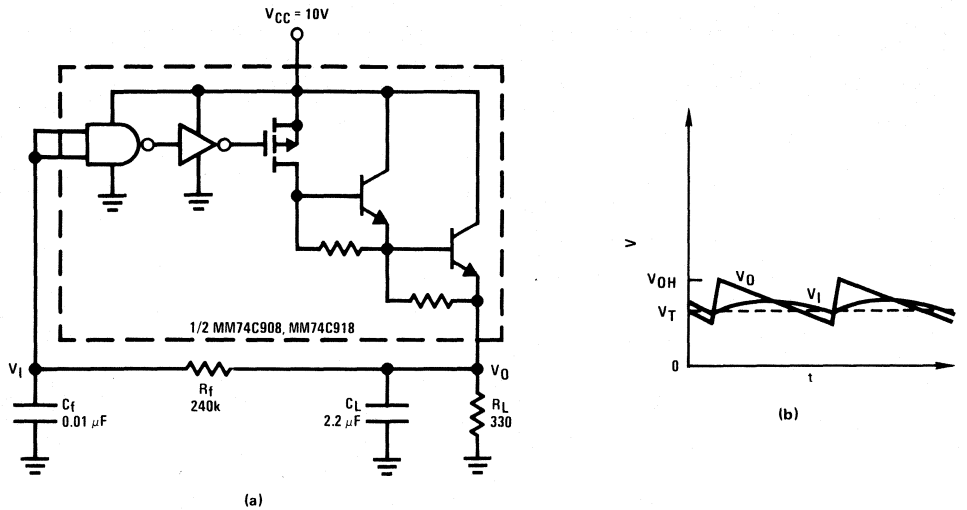


FIGURE 15. Single Driver Oscillator

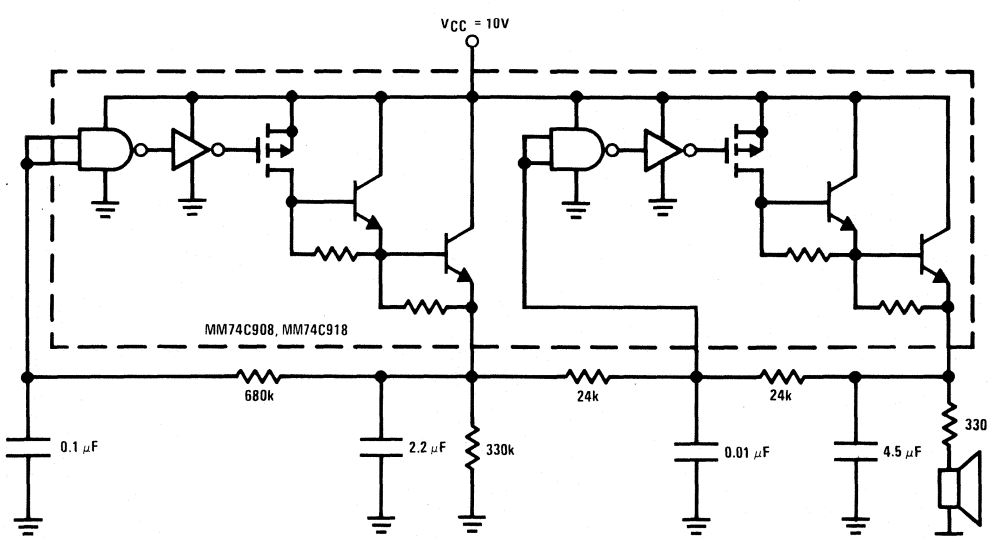


FIGURE 16. Low Cost Siren

The NAND functions at the input can also be used to reduce package count in applications where both high output drive and input NAND features are required. One such example is given in *Figure 17*.

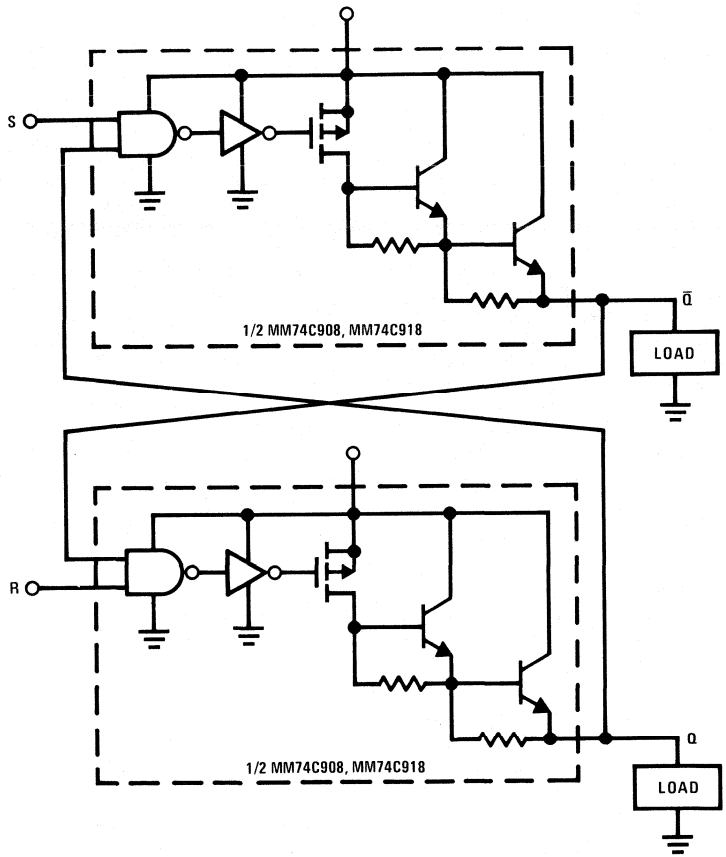


FIGURE 17. High Drive RS Latch

CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200
Jake Buurma

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters – two of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 1/2-digit DPM and ADD3701 3 3/4-digit DPM) while the other two (ADC3511 3 1/2-digit A/D and ADC3711 3 3/4-digit A/D) have addressable BCD outputs. These last two devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 1/2-digit types divide the input into 2,000 counts plus sign, while the 3 3/4-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 1/2-digit converters require 200 ms per conversion; 3 3/4-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the inputs must be floating with respect to the supply return. Without a floating supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

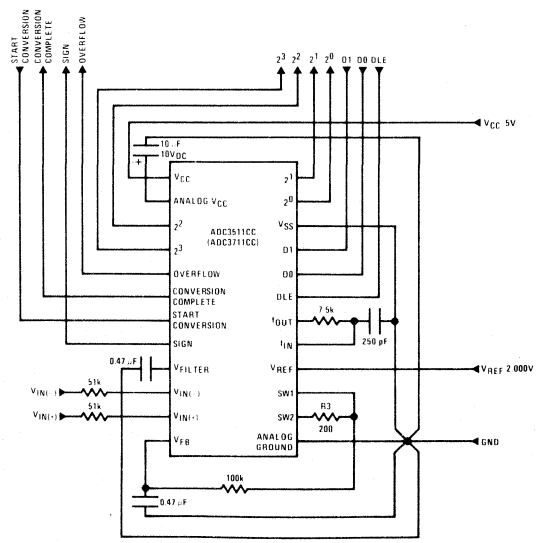


FIGURE 1. Basic A/D Converter

BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

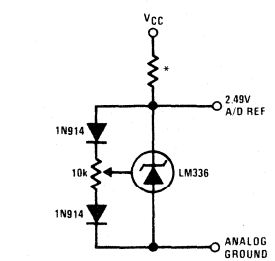
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*. One reference can be used for many A/D's. The value of the upper series resistor R1 depends on the number of converters used.



$$*R1 = \frac{2.49V}{(2N + 1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3 and 4. Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multichannel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The program then calls a subroutine which

goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

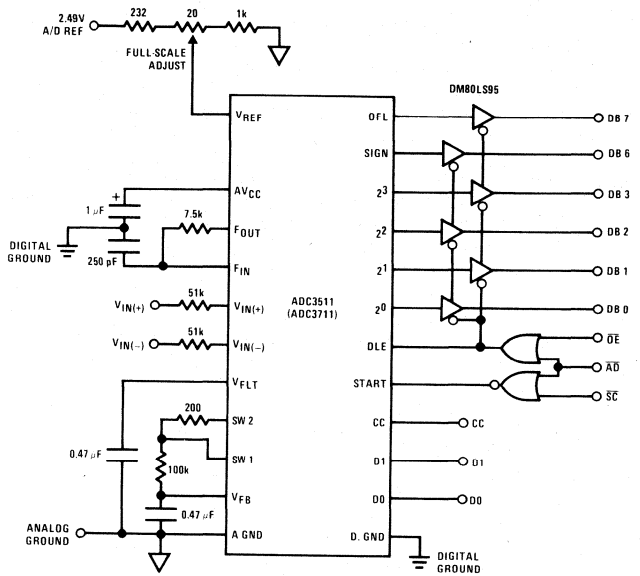


FIGURE 3. Dual Polarity A/D Requires that Inputs are Floating with Respect to the Supply. Input Range is ±1.999V.

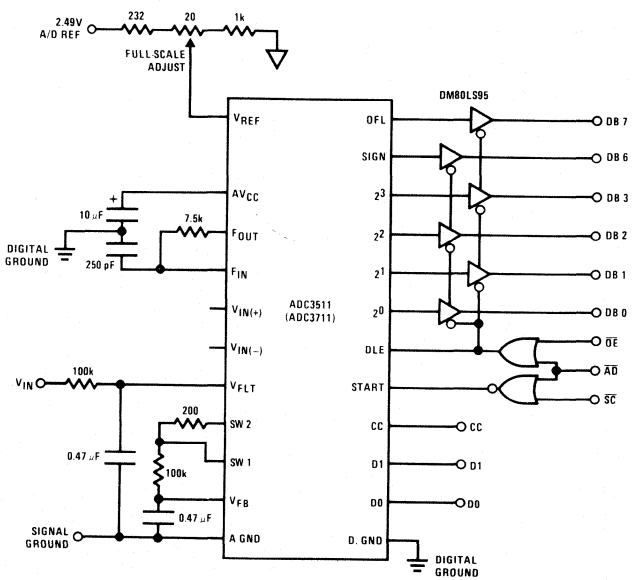


FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range is +1.999V.

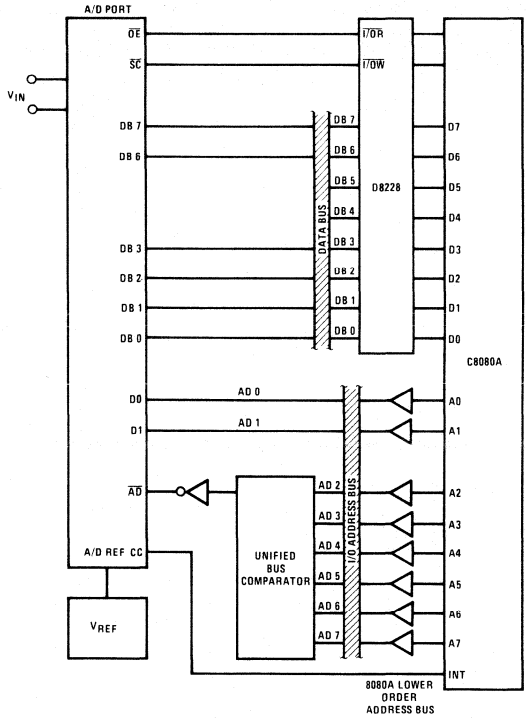


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

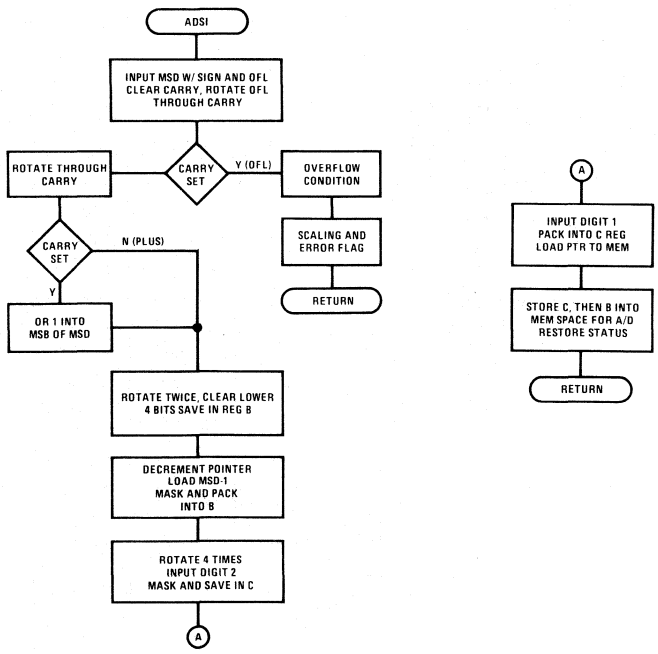


FIGURE 6. Flow Chart for Single Channel A/D Converter

```
LABEL   OPCODE   OPERAND    COMMENT
ADIS:   PUSH     PSW        ; A/D interrupt
                            service
        PUSH     H          ; save
        PUSH     B          ; current status
        IN       ADD 4      ; input A/D digit 4
        IN       ADD 4      ; delay
        ORA                 ; reset carry
        RAL                 ; rotate OFL thru
                            carry
        JC       OFL        ; overflow condition
        RAL                 ; rotate sign thru
                            carry
        JC       PLUS       ; positive input
        ORI      20H        ; OR 1 into MSB,
                            neg input
PLUS:   RAL                 ; shift
        RAL                 ; into position
        ANI      FO         ; mask lower bits
        MOV      BA         ; save in B
        IN       ADD 3      ; input digit 3
        IN       ADD 3      ; delay
        ANI      OF         ; mask higher bits
        OR       B          ; pack into B
        MOV      B, A       ; save in B
        IN       ADD 2      ; input digit 2
```

```
LABEL   OPCODE   OPERAND    COMMENT
        IN       ADD 2      ; delay
        RAL                 ; rotate
        RAL                 ; into
        RAL                 ; upper
        RAL                 ; 4 bits
        ANI      FO         ; mask lower bits
        MOV      C, A       ; save in C
        IN       ADD 1      ; in digit 1
        IN       ADD 1      ; delay
        ANI      OF         ; mask upper bits
        OR       C          ; pack
        MOV      C, A       ; save in C
        LXI      H, ADMS    ; load ptr to A/D
                            Mem, space
        MOV      M, C       ; save C in memory
        INX      H          ; point next
        MOV      M, B       ; save B in memory
        OUT      ADD 1      ; start new conver-
                            sion
        POP      B          ; restore
        POP      H          ; previous
        POP      PSW        ; status
        EI                  ; enable interrupts
        RET                 ; return to main
                            program
```

Routine 1. Single Channel Interrupt Service Routine

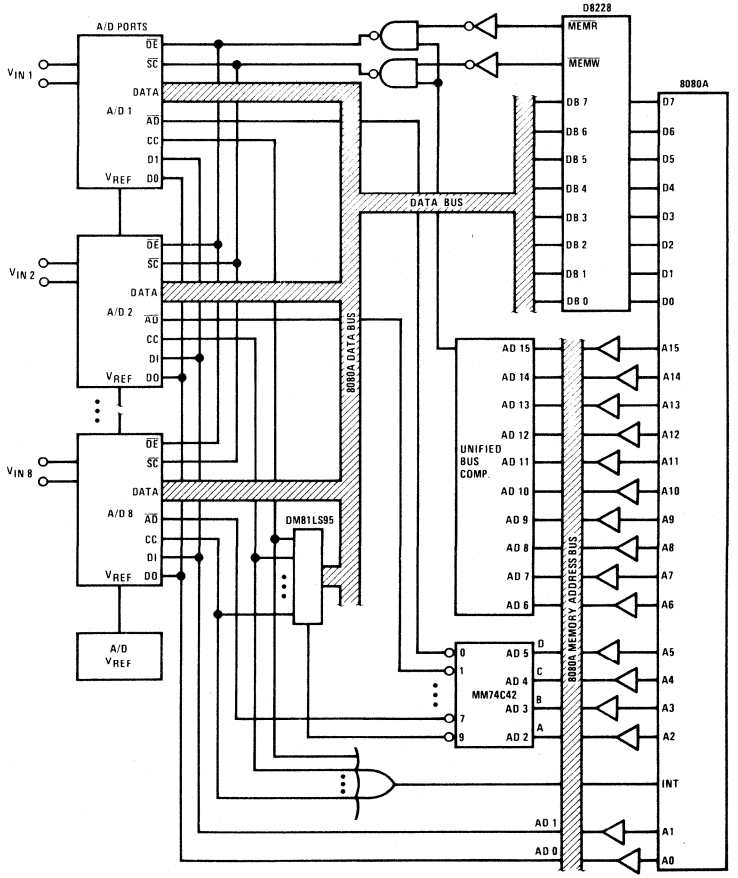


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

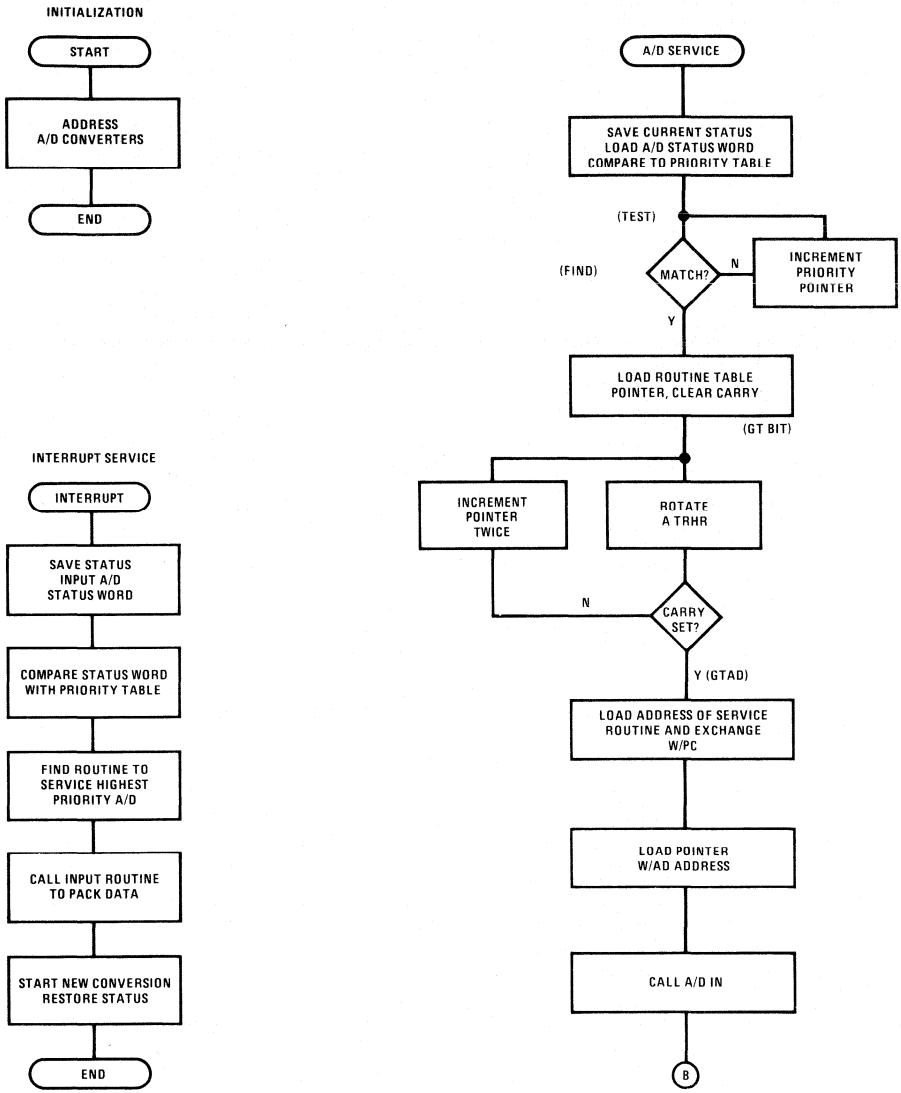


FIGURE 8. Flow Charts of A/D Routines

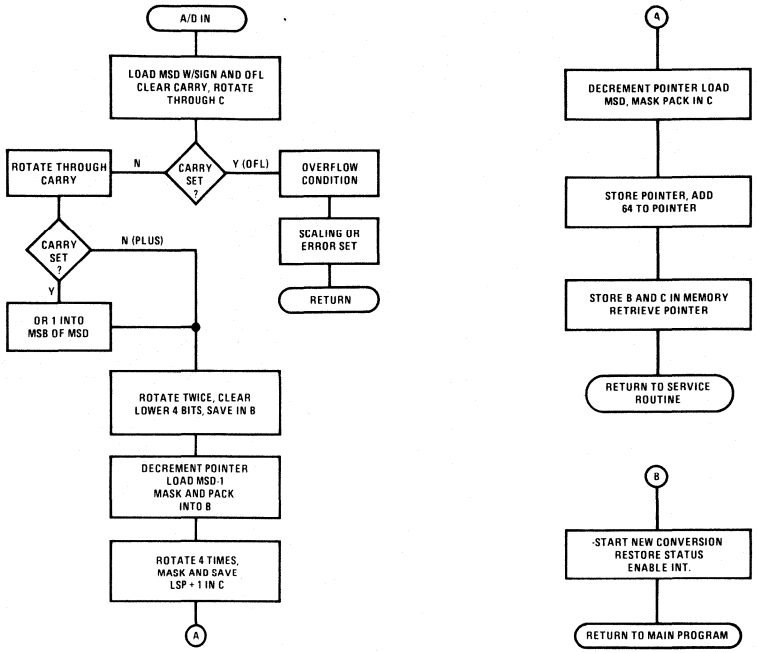


FIGURE 8. Flow Charts of A/D Routines (Continued)

```
LABEL   OPCODE   OPERAND    COMMENT
IAD:    PUSH     PSW        ; interrupt from A/D
        PUSH     H          ; save H & L on
                            stack
        PUSH     B          ; save B & C on
                            stack
        PUSH     D          ; save D & E on
                            stack
        LXI      H, ADWD    ; pickup A/D status
                            word
        MOV      6, M       ; move word into B
        LXI      H, PRTBL   ; pickup priority tbl
                            pointer
TEST:   MOV      A, B       ; place status word
                            in accum.
        ANA      M          ; mask with priority
                            table
        JNZ      FIND       ; match jump to
                            Find
        INX      H          ; point to lower
                            priority
        JMP      TEST       ; try again
FIND:   LXI      H, RTBL    ; pickup routine tbl
                            pointer
        ORA      A          ; reset carry
GTBIT:  RAR                 ; rotate thru carry
        JC       GTAD       ; bit was found
        INX      H          ; point to
        INX      H          ; next routine
        JMP      GTBIT      ; try again
GTAD:   MOV      E, M       ; move first byte
                            into E
        INX      H          ; point to next byte
        MOV      D, M       ; move second byte
                            into D
        XCGH                ; exchange DE, HL
        PCHL                ; jump to input
                            routine
INAD1:  LXI      H, AD1     ; pickup pointer to
                            A/D 1
        CALL     ADIN       ; call common input
                            routine
        MOV      M, A       ; start new conversion
        JMP      DONE       ; all done
INAD2:  LXI      H, AD2     ; pickup pointer to
                            A/D 2
        CALL     ADIN       ; call input routine
        MOV      M, A       ; start new conver-
                            sion
        JMP      DONE       ; all done
        .
        .
        .
DONE:   POP      D          ; restore D
        POP      B          ; restore B
        POP      H          ; restore H
        POP      PSW        ; restore PSW
        EI                  ; enable interrupts
        RET                 ; return to main
                            program
PRTBL:  DB       04H        ; 0000C100 AD3
                            highest priority
        DB       03H        ; 00000011 AD2 &
                            AD1 next priority
        .
        .
        .
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

```
LABEL   OPCODE  OPERAND   COMMENT
PRTBL:  DB      10H       ; 00010000 AD5
                            lowest priority
RTBL:   DW      1000H     ; routine for A/D 1
        DW      100CH     ; routine for A/D 2
        .
        .
        .
        DW      1060H     ; routine for A/D 8
ADIN:   MOV     A, M      ; input MSD plus
                            OFL & SIGN
        MOV     A, M      ; delay
        ORA     A         ; reset carry
        RAL               ; rotate left thru
                            carry, OFL
        JC      OFL       ; jump to overflow
                            if set
        RAL               ; rotate left thru
                            carry, sign
        JC      PLUS      ; jump to plus if set
        OR1     20H       ; OR1 into BCD,
                            MSB for minus
PLUS:   RAL
        RAL
        ANI     FO        ; mask lower order
                            bits
        MOV     B, A      ; save in B
        DCR     H         ; point to MSD-1
        MOV     A, M      ; input MSD-1
        MOV     A, M      ; delay
        ANI     OF        ; mask higher 4 bits
        OR      B         ; pack MSD and MSD-1
        MOV     B, A      ; save in B
        DCR     H         ; point to LSD + 1
        MOV     A, M      ; input LSD + 1
        MOV     A, M      ; delay
        RAL               ; rotate
        RAL               ; into
        RAL               ; upper
        RAL               ; 4 bits
        ANI     FO        ; mask lower bits
        MOV     C, A      ; save in C
        DCR     H         ; point to LSD
        MOV     A, M      ; input LSD
        MOV     A, M      ; delay
        ANI     OF        ; mask upper bits
        OR      C         ; pack
        MOV     C, A      ; save in C
        SHLD    TEMP      ; store HL in temp
        MOV     A, L      ; move L in accum.
        ACI     64        ; generate lower
                            address
        MOV     L, A      ; above memory.
                            mapped
        MOV     A, H      ; converter addresses
        ACI     0         ; include carry
        MOV     H, A      ; to upper bits
        MOV     M, C      ; store C
        INX     H         ; then
        MOV     M, B      ; store B
        LHLD    TEMP      ; retrieve HL
        RET               ; return
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority (Continued)

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

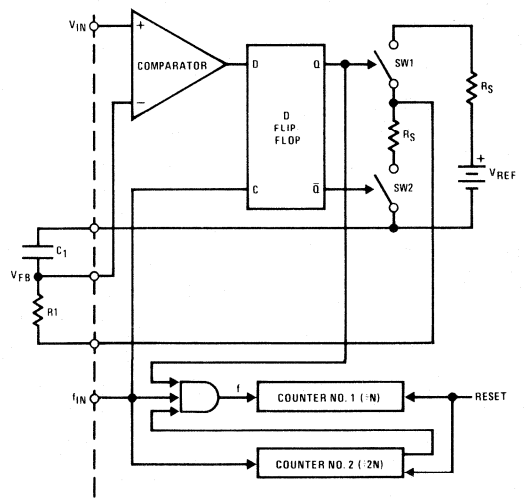
The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.
For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

ELECTRICAL CHARACTERISTICS

ADC3511CC, ADC3711CC $4.75 \leq V_{CC} \leq 5.25V$; $-40^{\circ}C \leq T_A + 85^{\circ}C$, f_C = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	(Note 3)				
		V_{IN} = 0–2V Full-Scale	−0.05	±0.025	0.05	% of Full-Scale
		V_{IN} = 0–200 mV Full-Scale				
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	$T_A = 25^{\circ}C$	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for $T_A = 25^{\circ}C$.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = 1/2 counts and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

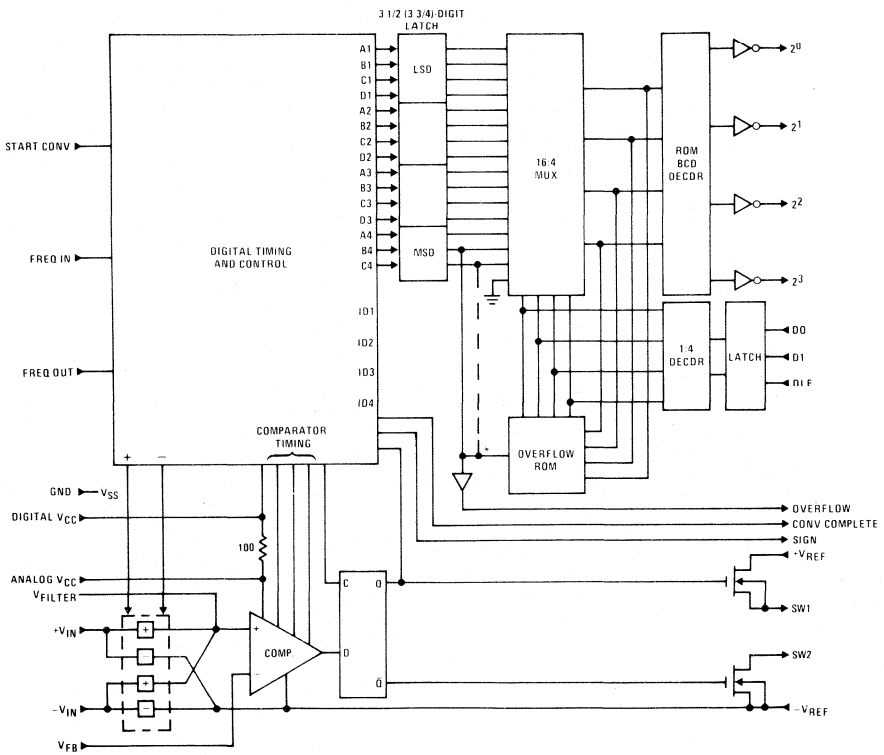


FIGURE A2. ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D) Block Diagram

Digital Weight Scales

National Semiconductor
Carson Chen
March 1978

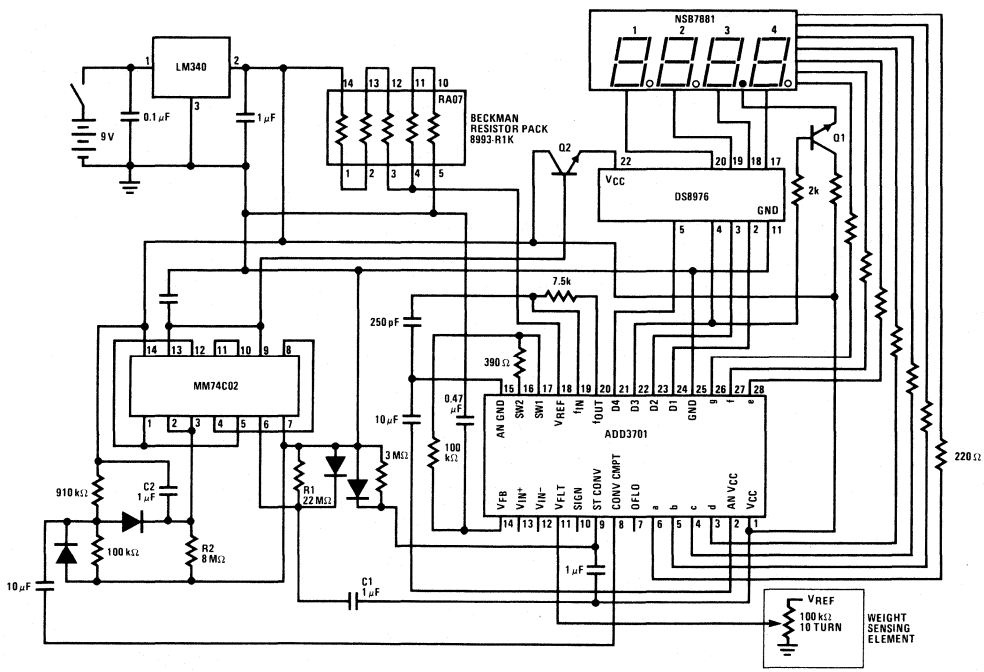
The application of digital systems to detect weight provides for low cost, accurate weight scales.

A developed system using the 3¾-digit DVM IC, ADD3701,* shown in figure 1, allows for conversion of an analog voltage to digital information linearly related to the weight being sensed.

Support circuitry for the DVM IC consists of a voltage regulator, a reference voltage, a weight sensing element, display drivers, and an LED display. Additional circuitry may be implemented for added features.

The weight scale circuit of figure 1 employs a potentiometer as the weight sensing element and functions as a variable voltage divider from ground to V_{REF}, 2 volts. An object placed upon the scale displaces the potentiometer wiper, which is connected to the scale mechanics, an amount proportional to its weight. Conversion of the wiper voltage to digital information is performed, decoded, and interfaced to the numeric display by the ADD3701. The LM340 regulates the V_{CC} supply voltage and the RA07 resistor array is connected as a voltage divider to generate the ADD3701 2V reference voltage. The NSB7881 is driven by the ADD3701 segment drivers and the DS8976 digit drivers.

*See ADD3701 data sheet for details of DVM operation.



Notes:

1. R1, C1 defines POWER ON display blanking interval. R2, C2 defines display ON time.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.
3. Display sequence for Rev A ckt implementation:
   - t = 0 sec • power ON
   - t = 0 → 5 sec • display blanked • system converging
   - t = 5 → 10 sec • conversion complete • display ENABLE
   - t > 10 sec • display blanked • wait for new POWER UP cycle

Figure 1

Q2, the MM74C02 and surrounding circuitry generate the display sequence explained in Note 3 of figure 1.

The ADD3701 3¾-digit DVM displays a maximum of 3999 counts, full scale, having a resolution of 500 μV per LSD.

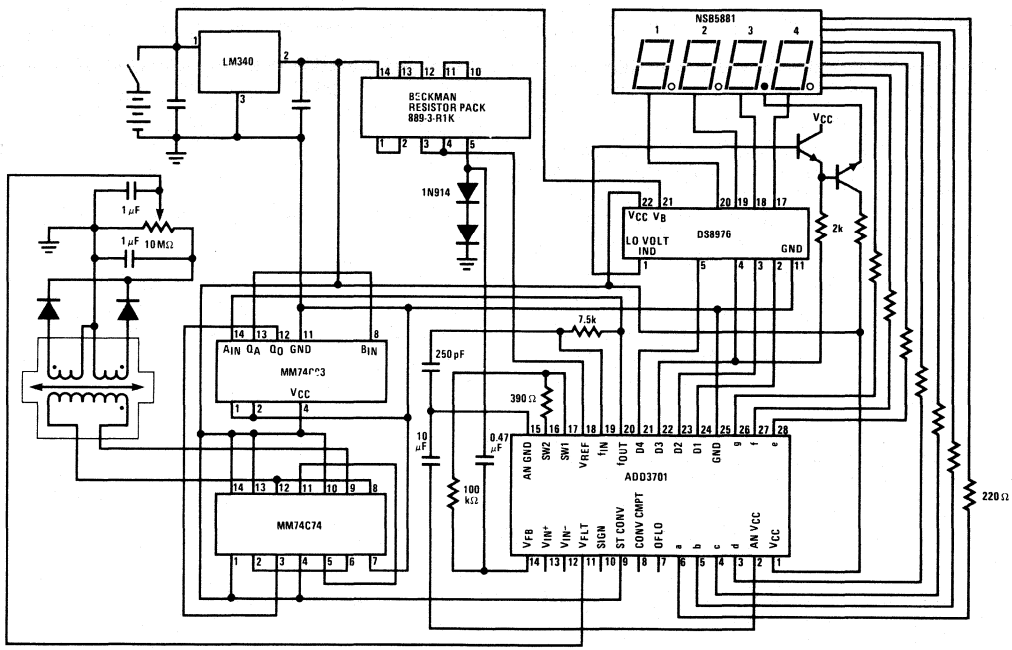
With the decimal point of digit 3 forced "ON" by Q1 the maximum displayed reading of figure 1 would equate to 399.9 units of weight.

Figure 2 is a weight scale sensor similar to that in figure 1, differing only in the weight sensing element and its related support circuitry.

The transformer of figure 2 is rectified to a DC voltage, proportional to a weight displacement, and then converted to its digital equivalent with the ADD3701.

The purpose of setting analog ground two diode drops above digital ground is to help cancel the inherent air coupling offset voltage generated by the transformer.

Figure 2 is also connected to display a maximum of 399.9 units of weight. The accuracy of both systems without the transducer elements is ±1 LSD at 25°C ± 15°C.



Notes:

1. Excitation to the LVDT (i.e., outputs of the MM74C93 and MM74C74) may be altered to compensate for the varying frequency ranges of LVDTs.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Figure 2

DC Noise Immunity of CMOS Logic Gates

National Semiconductor
Vivek Kulkarni
March 1978

INTRODUCTION

The immunity of a CMOS logic gate to noise signals is a function of many variables, such as individual chip differences, fan-in and fan-out, stray inductance and capacitance, supply voltage, location of the noise, shape of the noise signal, and temperature. Moreover, the immunity of a system of gates usually differs from that of any individual gate; thus a generalized analysis of the noise immunity of a logic circuit becomes a very complex process when one takes all the above parameters into consideration.

The complementary structure of the inverter results in a near-ideal input-output characteristic with switching point midway (45%-55%) between the "0" and "1" output logic levels. The result is a high noise immunity (defined as the maximum noise voltage which can appear on the input without switching an inverter from one state to another). National's CMOS circuits have a typical noise immunity of 0.45 V_{CC}. This means that a spurious input which is 45% of the power supply voltage typically will not propagate through the circuit. However, the standard guaranteed value through the industry is 30%.

This note describes the variation of the transfer region (or DC noise immunity) of a multiple-input gate in conjunction with the gate configuration — a consideration important in the system design.

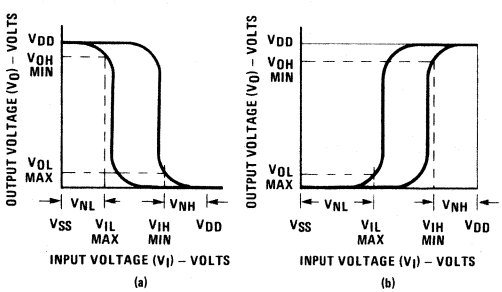


Figure 1. Minimum and Maximum Transfer Characteristics for (a) Inverting Logic Function and (b) Noninverting Logic Function.

Transfer Characteristics

Figure 1 illustrates minimum and maximum transfer characteristics useful for defining noise immunity for an inverter and a non-inverter. Some definitions are as follows:

V_{IH}min = the minimum input voltage high-level input for which the output logic level does not change state.

Then:

$V_{NL} = V_{IL}$max = "low level" noise immunity

$V_{NH} = V_{DD} - V_{IH}$ = "high level" noise immunity

V_{OH}min = minimum high level output voltage for rated V_{NL} [for inverting function as in figure 1(a)].

Table I shows the UB and B series noise immunity and noise margin ratings determined by the Joint Electron Devices Engineering Council (JEDEC). B series ratings are slightly higher than the UB series because of the buffered nature of these gates.

Table I. UB and B Series DC Noise Immunity and Noise Margin ($T_A = 25°C$)

Characteristics	Test Conditions V_O (V)	Test Conditions V_{DD} (V)	Input Voltage (V)
Input Low Voltage V_{IL} max			
B types	0.5/4.5	5	1.5
	1/9	10	3
	1.5/13.5	15	4
UB types	0.5/4.5	5	1
	1/9	10	2
	1.5/13.5	15	2.5
Input High Voltage V_{IH} min			
B types	0.5/4.5	5	3.5
	1/9	10	7
	1.5/13.5	15	11
UB types	0.5/4.5	5	4
	1/9	10	8
	1.5/13.5	15	12.5

Since the MOS transistors are voltage-controlled resistors, the transfer characteristics and consequently the DC noise immunity are determined by the parallel series combination of the transistor impedances in conjunction with the input voltages, the number of inputs, and the gate circuit configuration. This consideration becomes more important for a system designer who has harsh-noise-prone applications.

The value of the standard transistor ON resistance may vary from 10 MΩ down to almost 30 Ω (depending on the dimensions of the MOS-FET and applied voltages). For different input conditions, different combinations of the impedances of the N-channel transistors connected in parallel and the P-channel transistors connected in

series will come into play for a NOR gate. This is illustrated in figure 2. For a NAND gate, similar considerations hold good and give rise to varying transfer characteristics as shown in figure 3.

EXAMPLE OF CD4001

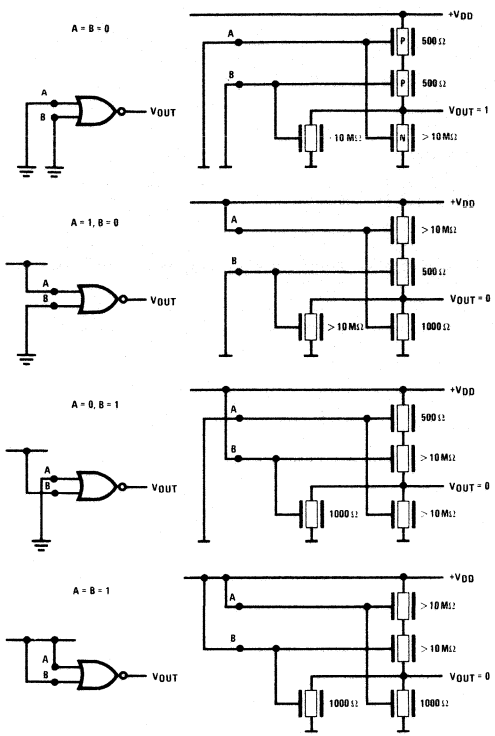


Figure 2. Typical Transistor ON/OFF Resistances for Various Input Combinations for CD4001.

Analysis

The DC transfer characteristics of the CMOS inverter can be calculated from the simplified DC current-voltage characteristics of the N- and P-channel MOS devices.

In the transfer region, where both transistors are in saturation, the following relationships can be used for an inverter.

N-channel drain current will be:

$$I_{dsn} = \frac{K_n}{2}(V_{IN} - V_{TN})^2 \qquad (1)$$

P-channel drain current will be:

$$-I_{dsp} = \frac{K_p}{2}(V_{IN} - V_{DD} - V_{TP})^2 \qquad (2)$$

where:

$$K_n = \frac{\mu_n C_{ox} W_n}{L_n}, \quad K_p = \frac{\mu_p C_{ox} W_p}{L_p}$$

Taking the ratio of (2) and (1):

$$\frac{|I_{dsp}|}{I_{dsn}} = \frac{K_p}{K_n} \cdot \frac{(V_{IN} - V_{DD} - V_{TP})^2}{(V_{IN} - V_{TN})^2}$$

$$\frac{K_p}{K_n} = \frac{|I_{dsp}|}{I_{dsn}} \cdot \frac{(V_{IN} - V_{TN})^2}{(V_{IN} - V_{DD} - V_{TP})^2} \qquad (3)$$

Studies made at National show good correlations between the process monitor pattern and actual device on a wafer for drive currents. Thus the ratio K_p/K_n can be calculated for the actual device if one knows drive currents for the test pattern, widths of N- and P-channel devices and threshold voltages from a given process.

The transition voltage is calculated from basic current equations and from the fact that some current has to flow through P- and N-channel devices. Equating saturation currents and rearranging terms, one can obtain[1]:

$$\text{Transition Voltage} = V_{IN}^* = \frac{V_{TN} + \sqrt{\frac{K_p}{K_n}}(V_{DD} - |V_{TP}|)}{\sqrt{1 + K_p/K_n}} \qquad (4)$$

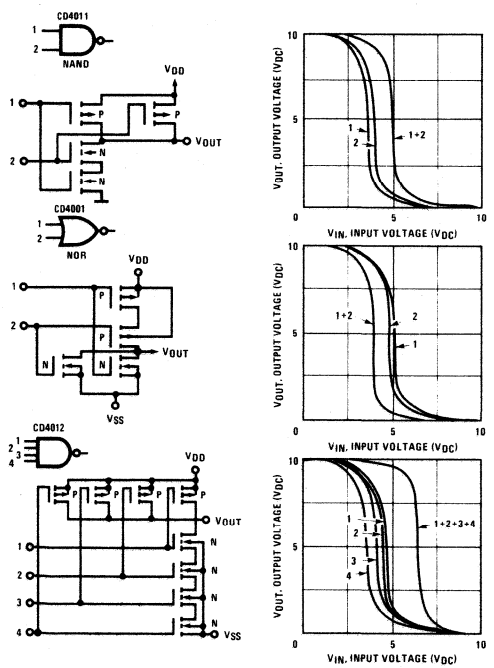


Figure 3. Allowed Voltage Transfer Curve Shifts which Result Due to Various Input Combinations of Multiple Input Gates.

By selecting $|V_{TP}| = V_{TN}$ and $K_p = K_n$, transition voltage can be designed to fall midway between 0V and V_{DD} – an ideal situation for obtaining excellent noise immunity. However, it is not always possible to obtain equal threshold voltages because of process variations. Also, W/L ratio for a P-channel device must be made 2 or 3 times larger than W/L ratio for an N-channel device to take into account mobility variations. The designer should consider these factors when designing for the best noise immunity characteristics.

In equation (4), the value of K_p/K_n substituted is obtained from equation (3). With different gate configurations, effective W_p and W_n values change; also, K_p/K_n ratio changes and a shift in transfer characteristics results.

For the 4-input NOR gate like CD4002, an empirical relation for the low noise margin V_{NL} has been obtained, which is as follows:

$$V_{NL} \approx V_{DD}\left[\frac{1}{1.5 + \frac{N_i}{N_m}} - 0.1\right] \qquad (5)$$

where:

N_i = number of used inputs/gate

N_m = total number of inputs/gate

The input voltage high noise margin V_{NH} can be calculated by:

$$V_{NH} \approx V_{DD}\left[0.9 - \frac{1}{1.5 + \frac{N_i}{N_m}}\right] \qquad (6)$$

Similar equations can be derived for a NAND gate.

From equations (5) and (6), one can see that the low noise margin V_{NL} will *decrease* as a function of the number of controlled inputs, while it will increase for a NAND gate. The input HIGH noise margin will *increase* as a function of the number of controlled inputs for the NOR gate; for the NAND gate it will decrease.

Figure 4 depicts $V_{OUT} = f(V_{IN})$ for different configurations for NOR and NAND gates. The system designer can thus use these facts effectively in his design and obtain the best possible configuration for the desired noise immunity with National's logic family.

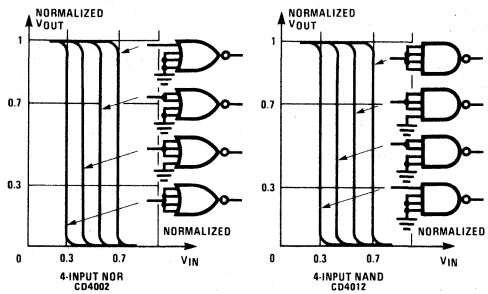


Figure 4. Example of Transfer Voltage Variation for NOR and NAND Gates for Various Input Combinations.

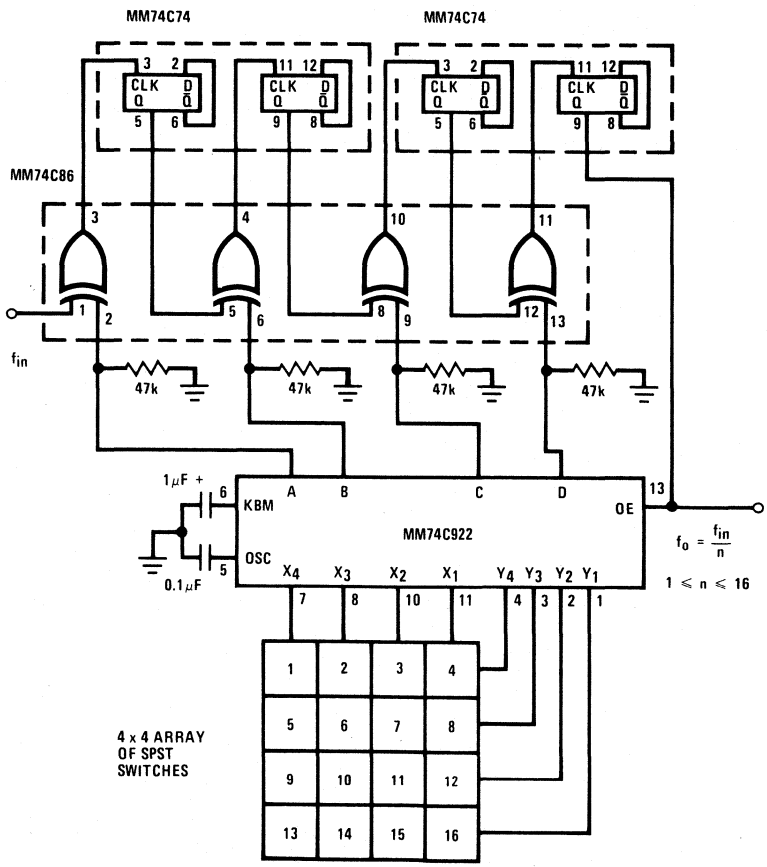
1. Carr, W.N., and Mize, J.P., *MOS/LSI Design and Application*, Texas Instruments Electronic Series, 1972.

Keyboard Programmable Divide-by-N Counter with Symmetrical Output

National Semiconductor
Digital Brief 5
Gerald Buurma

A CMOS key encoder combines with a couple of Dual D flip-flops and an exclusive OR package to form a simple but versatile programmable divider. The input frequency can be divided by any number n between 1 and 16 by simply pressing the appropriate key. The counter output is symmetrical for both odd and even divisors.

This circuit is useful for simple frequency synthesis or as an oscilloscope triggering unit where the displayed signal is applied to the counter input and the external trigger of the oscilloscope is connected to the counter output. The trigger signal is then some submultiple of displayed signal which often results in a more stable trace. Different divisors can be easily keyed in as the input signal varies.



Simply press the key and the input frequency is divided by that number. The output frequency is symmetrical for odd and even divisors. Use it for simple frequency synthesis or as a keyboard controlled oscilloscope triggering unit.

The key encoder scans the key array which is set up so the key labeled "16" is in the matrix position which causes "0" to be encoded, the key labeled "15" causes "1" to be encoded, and so on until we find that the key position labeled "1" causes a binary "15," or all ones, at the output of the encoder. The key arrangement converts a key position so that any number n from 1 to 16 is encoded as 16 - n at the encoder output. For example, if the key labeled 5 is pressed the binary number 1011 = 11 appears at the encoder output. The MM74C922 key encoder scans the keys, detects, debounces, and encodes any entry. An internal register remembers the last key pressed and presents it to the Tri-State® outputs.

The input to the exclusive OR is a "zero" when the respective encoder output is a "zero" or when the feedback signal from the last counter stage forces the encoder outputs into Tri-State. When in Tri-State the pull down resistors feed a "zero" into the exclusive OR inputs.

When the output is an active "one," the clock signal from one flip-flop to the next is inverted by the exclusive ORs. When the output is a "zero" or the encoder is in Tri-State, due to the feedback signal, the clock signal from one flip-flop to the next is the same phase. For every n/2 input time period, the counter output and feedback change state. Whenever the feedback signal changes state, all flip-flops programmed with a "one" by the encoder change their phases; this effectively adds a clock pulse to that stage of the counter. The addition of clock pulses to the 2^0, 2^1, 2^2 or 2^3 stages allows us to divide by any number between 1 and 16. Since the feedback changes state every n/2 input time period, the output frequency is symmetrical for any divisor.

The unit operates over the standard CMOS supply range of 3 to 15 volts and has a typical upper frequency limit of one megacycle with a 10 volt supply.

REFERENCE

1. M. V. Subba Rao, "Programmable Divide by n Counter Provides Symmetrical Outputs for all Divisors," *Electronic Design*, no. 2, January 19, 1976, p. 82.

MM54C/MM74C Voltage Translation/Buffering

National Semiconductor
Memory Brief 18
John Jorgensen
Thomas P. Redfern

INTRODUCTION

A new series of MM54C/MM74C buffers has been designed to interface systems operating at different voltage levels. In addition to performing voltage translation, the MM54C901/MM74C901 through MM54C904/MM74C904 hex buffers can drive two standard TTL loads at V_{CC} = 5V. This is an increase of ten times over the two LpTTL loads that the standard MM54C/MM74C gate can drive. These new devices greatly increase the flexibility of the MM54C/MM74C family when interfacing to other logic systems.

PMOS TO CMOS INTERFACE

Since most PMOS outputs normally can pull more negative than ground, the conventional CMOS input diode clamp from input to ground poses problems. The least of these is increased power consumption. Even though the output would be clamped at one diode drop (−0.6V), all the current that flows comes from the PMOS negative supply. For TTL compatible PMOS this is −12V. A PMOS output designed to drive one TTL load will typically sink 5 mA. The total power per TTL output is then 5 mA x 12V = 60 mW. The second problem is more serious. Currents of 5 mA or greater from a CMOS input clamp diode can cause four-layer diode action on the CMOS device. This, at best, will totally disrupt normal circuit operation and, at worst, will cause catastrophic failure.

To overcome this problem the MM74C903 and MM74C904 have been designed with a clamp diode from inputs to V_{CC} only. This single diode provides adequate static discharge protection and, at the same time, allows voltages of up to −17V on any input. Since there is essentially no current without the diode, both the high power dissipation and latch up problems are eliminated.

To demonstrate the above characteristics, *Figures 1, 2, and 3* show typical TTL compatible PMOS circuits driving standard CMOS with two clamp diodes, TTL compatible PMOS driving MM74C903/MM74C904, and the TTL compatible PMOS to CMOS system interface, respectively.

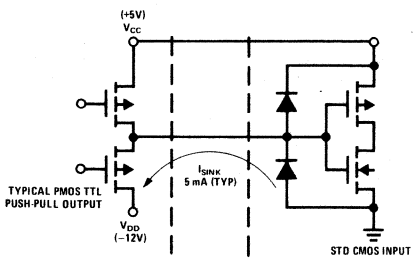


FIGURE 1.

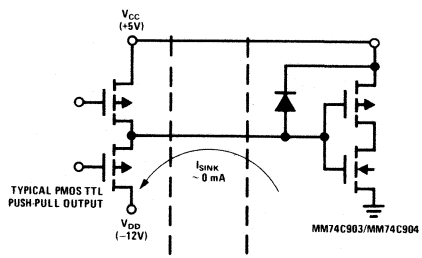


FIGURE 2.

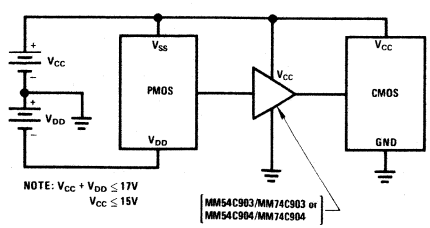


FIGURE 3. PMOS to CMOS or TTL Interface

CMOS TO CMOS OR TTL INTERFACE

When a CMOS system which is operating at V_{CC} = 10V must provide signals to a CMOS system whose V_{CC} = 5V, a problem similar to that found in PMOS-to-CMOS interface occurs. That is, current would flow through the upper input diode of the device operating at the lower V_{CC}. This current could be in excess of 10 mA on a typical 74C device, as shown in *Figure 4.* Again, this will cause increased power as well as possible four layer diode action.

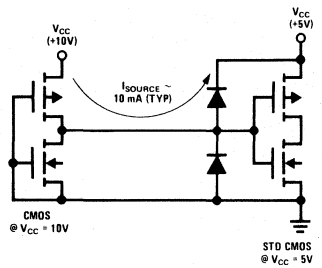


FIGURE 4.

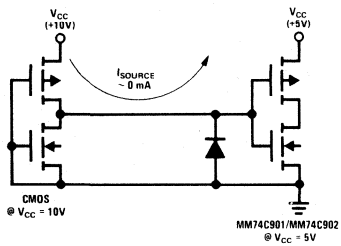


FIGURE 5.

Using the MM74C901 or MM74C902 will eliminate this problem. This occurs simply because these parts are designed with the upper diode removed, as shown in *Figure 5.* With this diode removed the current being sourced goes from about 10 mA to the leakage current of the reverse biased input diode.

Since the MM74C901 and MM74C902 are capable of driving two standard TTL loads with only normal input levels, the output can be used to directly drive TTL. With the example shown, the inputs of the MM74C901 are in excess of 5V. Therefore, they can drive more than two TTL loads. In this case the device would drive four loads with V_{IN} = 10V. If the MM74C902 were used, the output drive would not increase with increased input voltage. This is because the gate of the output n-channel device is always being driven by an internal inverter whose output equals that of V_{CC} of the device.

The example used was for systems of V_{CC} = 10V on one system and V_{CC} = 5V on the second, but the MM74C901 and MM74C902 are capable of using any combination of supplies up to 15V and greater than 3V, as long as V_{CC1} is greater than or equal to V_{CC2} and grounds are common. *Figure 6* diagrams this configuration.

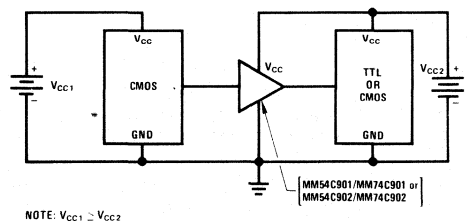


FIGURE 6. CMOS to TTL or CMOS at a Lower V_{CC}

The inputs on these devices are adequately protected with the single diode, but, as with all MOS devices, normal care in handling should be observed.

Radiation Hardened CMOS

National Semiconductor
Application Note 208
A. London
D. Matteucci
R. Wang

For many years, military, aerospace and satellite programs have depended on bipolar transistor and integrated circuit technology in the fabrication of airborne systems. Development of bipolar technology is an outgrowth, in part, of avionics and space applications needs. Despite their relatively high immunity or resistance to high levels of both constant and burst radiation in the form of gamma rays, x-rays, cosmic rays, and so on, bipolar devices have one drawback: high power consumption, which adds to the payload of spacecraft and missiles.

In recent years, development of sophisticated space, satellite and military systems, and mission requirements has fostered an active search for a radiation hardened circuit technology that consumes less power and offers a higher degree of circuit integration on a single silicon chip. Development of metal oxide semiconductor (MOS) devices, particularly the complementary MOS (CMOS) type, seemed to promise just such an alternative. But standard CMOS devices, even those qualified to MIL-STD-38510 or JAN standards, are sensitive to relatively low radiation levels. To date, mass producible radiation hardened or resistant CMOS devices have been able to withstand only 10^5 rads (Si), while many space, satellite and missile systems require circuitry resistance levels at least ten times higher, about 10^6 rads (Si), at a minimum. Now, the problem appears to be solved. A complete line of one megarad (10^6) CMOS logic products using a mass producible radiation hardening fabrication process has been developed, the result of a two-year research effort. Devices ranging in complexity from simple gates to large scale integrated (LSI) random access memories have been hardened to radiation doses of more than 10^6 rads of constant level gamma radiation (table 1). There are 47 circuits presently available with at least 21 more to be qualified by the end of 1978. To achieve this level of radiation resistance in a mass production CMOS process, major modifications were made in the basic commercial process, relating to gate oxidation, substrate and P-tub surface concentrations, and metallization.

Table 1. Examples of Radiation Hardened CMOS Devices, Hard to 10^6 Rads (Si)

1.	CD4001	Quad 2-Input NOR
2.	CD4002	Dual 4-Input NOR
3.	CD4006	18-Stage S/R
4.	CD4007	Dual Pair Plus Inverter
5.	CD4008B	4-Bit Adder
6.	CD4009	Hex Buffer
7.	CD4010	Hex Buffer
8.	CD4011	Quad 2-Input NAND
9.	CD4012	Dual 4-Input NAND
10.	CD4013B	Dual "D" Flip-Flop
11.	CD4014	8-Stage S/R
12.	CD4015	Dual 4-Bit Register
13.	CD4016	Quad Switch
14.	CD4017B	Decade Counter/Divider
15.	CD4019B	Quad AND/OR Select
16.	CD4020	14-Stage Counter
17.	CD4021	8-Stage S/R
18.	CD4022B	Octal Counter/Divider
19.	CD4023	Triple 3-Input NAND
20.	CD4024	7-Stage Binary Counter
21.	CD4025	Triple 3-Input NOR
22.	CD4027B	Dual "J-K" Flip-Flop
23.	CD4028B	BCD to Decimal Decoder
24.	CD4029B	Up/Down Counter
25.	CD4030	Quad Exclusive-OR
26.	CD4031B	64-Bit Shift Register
27.	CD4040	14-Stage Counter
28.	CD4041	True/Complement Buffer
29.	CD4044	Quad NAND R/S Latch
30.	CD4049	Hex Buffer
31.	CD4050B	Hex Buffer
32.	CD4051B	Analog Multiplexer/Demultiplexer
33.	CD4052B	Analog Multiplexer/Demultiplexer
34.	CD4053B	Analog Multiplexer/Demultiplexer
35.	CD4066B	Quad Switch
36.	CD4070B	Quad Exclusive-OR
37.	CD4076B	Quad "D" Flip-Flop
38.	CD4093	2-Input NAND Schmitt Trigger
39.	MM54C86	Quad Exclusive-OR
40.	MM54C173	Quad "D" Flip-Flop
41.	MM54C200	256-Bit RAM
42.	MM54C901	Hex Buffer
43.	MM54C902	
44.	MM54C903	
45.	MM54C904	
46.	MM54C906	
47.	MM54C907	

Bipolar vs CMOS

The inherently higher radiation resistance of bipolar over CMOS devices results from a basic difference in their structures. Bipolar devices are vertical structures. The basic elements — emitter, collector, and base — are laid down vertically, layer upon layer, by diffusion. Current flows through the bulk silicon, some distance below the silicon-silicon dioxide interface. Thus, there is some inherent protection from the interface effects of ionizing radiation in bipolar devices.

CMOS devices are surface effect devices. The equivalent operating elements, gate, source and drain, are at the surface, and the flow of current occurs horizontally across the device, very close to the silicon-silicon dioxide interface. Changes in interface parameters created by gamma or x-radiation will have a first order effect on MOS transistor performance, in contrast to a second order effect on a bipolar device. Thus the basic physics of CMOS transistor structures need to be addressed to minimize ionizing radiation effects without substantially impacting performance.

CMOS Transistor Structure

Complementary MOS, or CMOS, combines two types of MOS devices, P-channel and N-channel structures, as a functioning unit. The lower power dissipation and high stability resulting from this complementary combination is particularly attractive in the design of portable, battery powered, electronic units, or for applications where a battery provides standby power.

MOS structures, both N- and P-types, perform in two modes, enhancement and depletion. In a P-channel enhancement mode MOS device, for example, the gate controls the current flow between the source and drain. In this device, when a negative voltage is applied to the gate with respect to the source, a field is set up across the gate dielectric, producing a positively charged conductive path, a channel, between the source and the drain. This is known as an enhancement mode device because zero gate to source voltage turns off the device. In the alternative mode, depletion, current flows despite the gate voltage being zero, because sufficient field is still present within the gate to induce a conductive path between the device source and drain regions. The N-channel MOS transistor is similar to the P-channel alternative, except that positive voltage applied to the gate with respect to source induces a negatively charged conductive path between source and drain to turn the device on.

Conventional CMOS logic circuits are produced with only enhancement mode N- and P-channel devices. The process is designed to give turn on (threshold) voltage values for both types of devices which insure proper circuit performance. Figure 1 illustrates the cross section of a CMOS structure connected in a simple inverter configuration. To form the standard metal gate CMOS structure, a lightly doped P-tub is formed by diffusion into an N-type substrate with the tub becoming the substrate for the N-channel transistor. The N+ and P+ impurities are diffused into

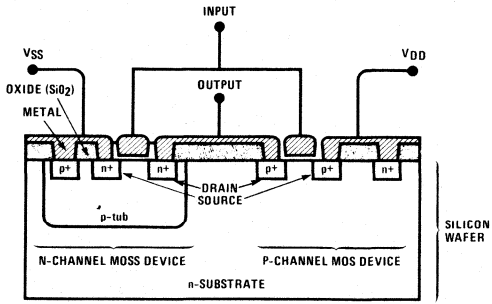


Figure 1. Cross Section of a CMOS Transistor Structure Connected in a Simple Inverter Configuration

the P-tub and N-substrate to become the N- and P-channel transistors, source and drain regions, respectively. These diffusions also serve as contacting regions to the positively biased N-substrate and the normally grounded P-tub regions (V_{DD} and V_{SS} respectively).

A gate oxide is grown such that a thin film of dielectric oxide material bridges the source/drain regions over the entire circuit. Finally, contact apertures are etched to the source/drain regions and an aluminum film evaporated and etched to form gate electrodes, contacts to device terminals, and interconnection conductor lines.

Effects of Ionizing Radiation

A CMOS transistor's radiation resistance is primarily determined by formation of the gate structures in both P-channel and N-channel devices. The gate structures are used to turn the MOS devices on or off; that is, to start or stop a flow of current from the source to the drain. Ionizing radiation induces unwanted positive charge into the gate oxide structure, resulting in lowering the threshold voltage of actual circuit devices and parasitic field oxide devices by values of as much as 30V or more. In establishing a radiation hardened CMOS process, it is necessary to incorporate processing steps which minimize these radiation induced shifts in critical locations of the IC structure.

The impact of radiation induced oxide charge on operating CMOS devices is to decrease both the N-channel threshold voltage, V_{TN}, and the P-channel threshold voltage, V_{TP}. The most serious problem occurs when sufficient reduction in V_{TN} occurs to cause the N-channel device to go from enhancement to depletion mode operation. This results in exces-

sive power supply current drain and loss of circuit functionality. The most severe stress on an N-channel device occurs when its gate is positively biased during irradiation. This causes positive charge in the oxide to be driven closer to the Si-SiO_2 interface where it is more effective in causing the P-type substrate surface to become inverted to N-type.

In normal operation, positive bias does not appear between the gate and substrate of P-channel devices since the substrate is already at the most positive circuit potential, V_{DD}. The most severe effect on P-channel devices during irradiation often occurs with zero gate to substrate bias. This stress creates Si-SiO_2 interface states which are capable of holding a positive charge with negative voltage applied to the gate. This increases the absolute value of V_{TP}, but is a much less deleterious effect on the circuit than the V_{TN} shift.

CMOS Process Modification

Gate Oxidation: To minimize both the radiation induced positive oxide charge and formation of Si-SiO_2 interface states, a dry rather than wet oxidation step is used. The gate oxide is thermally grown in a pure oxygen ambient, rather than in a water ambient, as is the case in some metal gate fabrication processes. Moreover, the gate oxide is thermally grown at 1000°C, followed by a nitrogen anneal at 850°C. This cycle has been empirically found to produce oxides having a high degree of resistance to ionizing radiation effects as well as excellent pre-radiation MOS characteristics.* Why this is so is not known exactly, and is still being studied. The need for thermally growing gate oxides at 1000°C in dry oxygen for optimal radiation hardness is one of the more intriguing aspects of this experimentally deduced cycle.

Metallization: A by-product of the E-beam aluminum evaporation process commonly used in commercial IC fabrication is soft x-radiation. This radiation produces the same type of positive charge in the gate oxide and interface states which a radiation hardened oxide should resist. Although these harmful effects in the gate oxide can be removed by a high temperature anneal cycle, subsequent exposure of the oxide to ionizing radiation results in a drastically less radiation resistant structure. Use of a non-E-beam metallization technique circumvents the problem of high threshold shifts due to irradiation under zero and negative gate bias associated with soft x-ray damage. For this reason, induction heated evaporation of aluminum is used to fabricate radiation hardened CMOS products.

Substrate and P-tub Surface Concentration: The impact of ionizing radiation on V_{TN} and V_{TP} values in a CMOS device is resolved through process modification. In anticipation of these threshold voltage shifts, radiation hardened CMOS devices are designed with the initial value of V_{TN} as high as possible and V_{TP} as close to zero as possible without sacrificing pre-radiation circuit performance. Both the substrate resistivity and the P-tub surface concentration have been modified with the initial value of V_{TN} being increased to 1.8 volts from the standard value of 1.3 volts and V_{TP} being changed from the standard −1.7 volts to −1.3 volts.

Performance Characteristics

Figures 2 and 3 illustrate the variation of post radiation V_{TN} and V_{TP} with dose. The distribution of the V_{TN} and V_{TP} data is found normal both before and after irradiation. The solid line shows the mean value of V_{TN} (or V_{TP}), and the dashed lines indicate the one standard deviation, σ, value on either side of the mean. This value, for both N- and P-channel devices, remains fairly constant with dose from the unirradiated case through 10^6 rad (Si). The values shown remain well above the 300mV V_{TN} lower limit, which, if penetrated, would lead toward N-channel depletion mode behavior and risk of losing circuit functionality and excessive supply current drain.

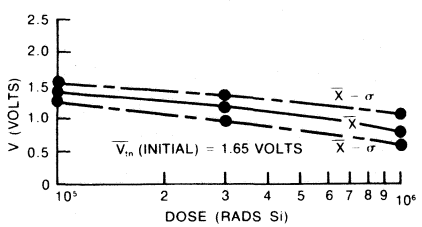


Figure 2. V_{TN} vs Dose

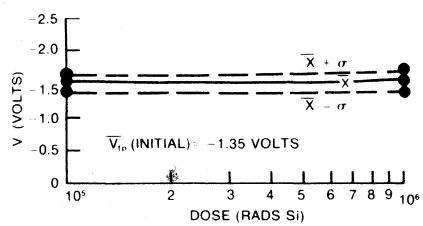


Figure 3. V_{TP} vs Dose

*W.R. Dawes, Jr., G.F. Derbenwich and B.L. Gregory, "Process Technology for Radiation Hardened CMOS Integrated Circuits," *IEEE Journal of Solid State Circuits*, Sc-11, No. 4, p. 459, August 1976.

Figure 4 illustrates the supply quiescent current, I_{SS}, variation as a function of dose. Since I_{SS} is a function of die size, curves have been plotted for three levels of integration, SSI, MSI and LSI. In all cases, the leakage level at 10^6 rad (Si) does not increase by more than an order of magnitude from the initial value. The end point at 10^6 rad (Si) for LSI of 30μA is far below the high temperature (125°C) specification of 600μA. The same conclusion can be drawn for MSI and SSI.

Figure 5 illustrates circuit propagation delay, t_{PD}, as a function of dose. The plot, similar to figure 4, is divided into three categories (LSI, MSI, SSI). The propagation delay value at 10^6 rads (Si) for all three categories increased roughly 20-25% from the initial value, well within desirable operating tolerances. In figures 2 through 5, the biasing conditions during irradiation were: V_{DD} = 10V, V_{IN} = 10V, and V_{SS} = 0V.

Hardness Assurance and Reliability

A sampling plan has been established to ensure radiation hardness to 10^5 and 10^6 rads, since ionizing radiation degrades IC performance and cannot be used for 100% screening. In addition, an intensive program to evaluate the reliability characteristics of radiation hardened CMOS circuits is underway. 476 devices of the CD4001 AD/RH, CD4011 AD/RH, and MM54C200D/RH types have been tested and have operated for over 800,000 hours without a failure. This corresponds to a failure rate less than or equal to 0.125%/1000 hours at 125°C with a 60% confidence level.

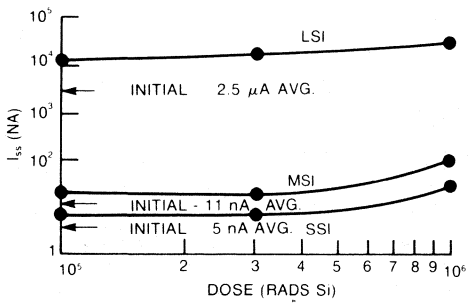


Figure 4. I_{SS} vs Dose

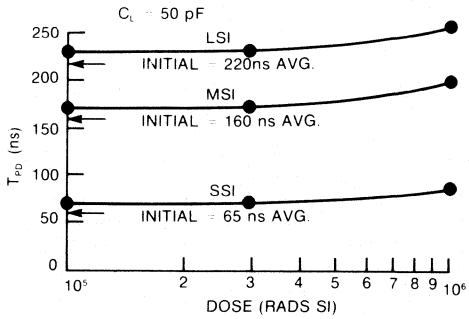


Figure 5. t_{PD} vs Dose

Ordering Information & Physical Dimensions

Ordering Information

MM74C Series

Order Number	Package	Temperature Range
MM74CXXN	Molded DIP (N)	−40°C to +85°C
MM74CXXJ	Cavity DIP (J)	−40°C to +85°C
MM54CXXJ	Cavity DIP (J)	−55°C to +125°C
MM54CXXD	Cavity DIP (D)	−55°C to +125°C
MM54CXXW	Cavity Flat Pack (W)	−55°C to +125°C
MM80CXXN	Molded DIP (N)	−40°C to +85°C
MM80CXXJ	Cavity DIP (J)	−40°C to +85°C
MM70CXXJ	Cavity DIP (J)	−55°C to +125°C
MM70CXXD	Cavity DIP (D)	−55°C to +125°C
MM70CXXW	Cavity Flat Pack (W)	−55°C to +125°C

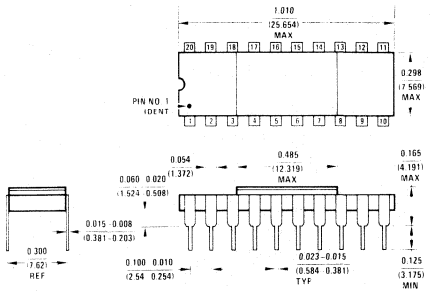
CD4000 Series

Order Number	RCA Equivalent Designation	Package	Temperature Range
CD40XXCN	CD40XXAE	Molded DIP (N)	−40°C to +85°C
CD40XXCJ	CD40XXAY	Cavity DIP (J)	−40°C to +85°C
CD40XXMJ	CD40XXAF	Cavity DIP (J)	−55°C to +125°C
CD40XXMD	CD40XXAD	Cavity DIP (D)	−55°C to +125°C
CD40XXMW	CD40XXAK	Cavity Flat Pack (W)	−55°C to +125°C
CD40XXBCN	CD40XXBE	Molded DIP (N)	−40°C to +85°C
CD40XXBCJ	CD40XXBY	Cavity DIP (J)	−40°C to +85°C
CD40XXBMJ	CD40XXBF	Cavity DIP (J)	−55°C to +125°C
CD40XXBMD	CD40XXBD	Cavity DIP (D)	−55°C to +125°C
CD40XXBMW	CD40XX3K	Cavity Flat Pack (W)	−55°C to +125°C
*CD45XXCN	CD45XX3E	Molded DIP (N)	−40°C to +85°C
*CD45XXCJ	CD45XXBY	Cavity DIP (J)	−40°C to +85°C
*CD45XXMJ	CD45XXBF	Cavity DIP (J)	−55°C to +125°C
*CD45XXMD	CD45XXBD	Cavity DIP (D)	−55°C to +125°C
*CD45XXMW	CD45XXBK	Cavity Flat Pack (W)	−55°C to +125°C

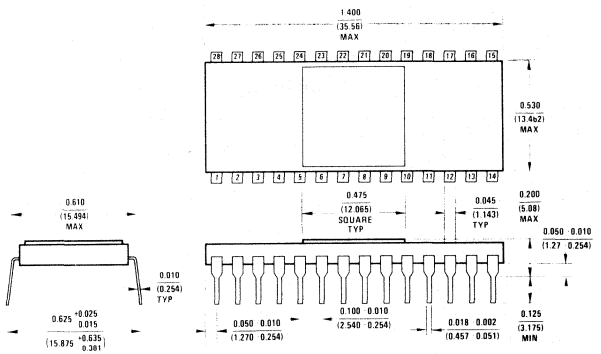
*Equivalent to Motorola MC145XX Series.

CMOS Packages

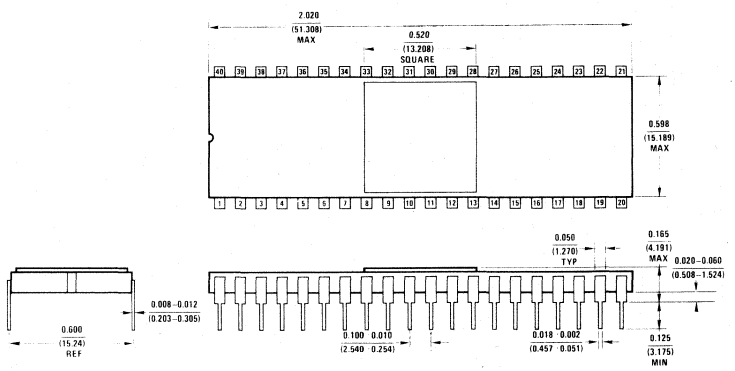
All dimensions expressed as $\frac{\text{inches}}{\text{millimeters}}$



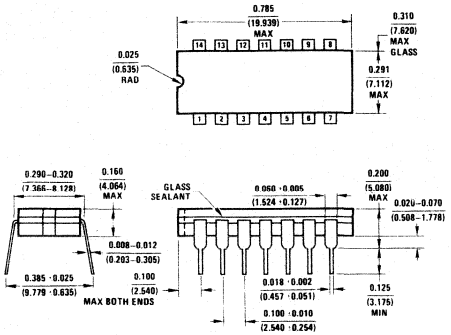
20-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D20A



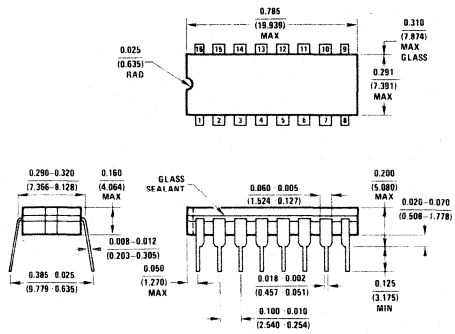
28-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D28A



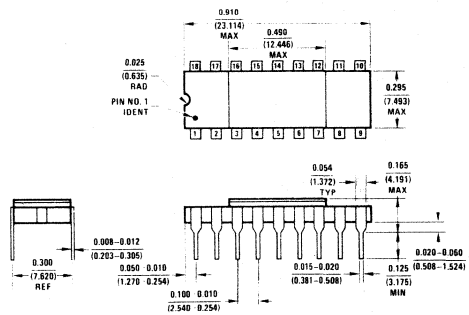
40-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D40C



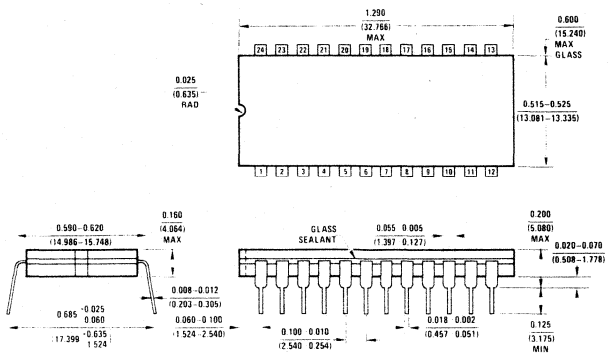
14-Lead Hermetic Dual-In-Line Package (J)
NS Package Number J14A



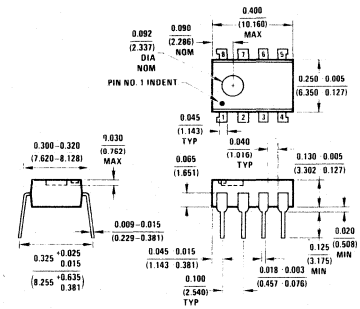
16-Lead Hermetic Dual-In-Line Package (J)
NS Package Number J16A



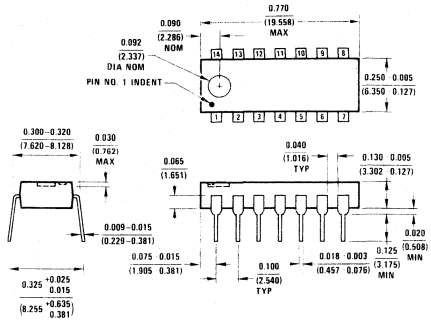
18-Lead Hermetic Dual-In-Line Package (D)
NS Package Number D18A



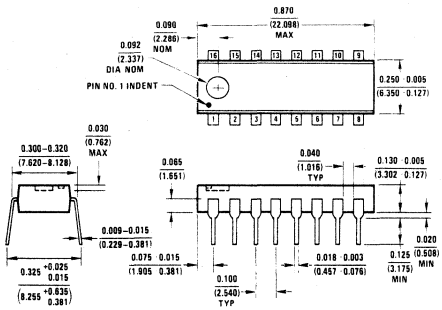
24-Lead Hermetic Dual-In-Line Package (J)
NS Package Number J24A



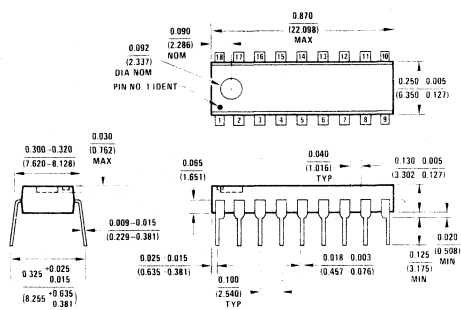
8-Lead Molded Mini Dual-In-Line Package (N)
NS Package Number N08A



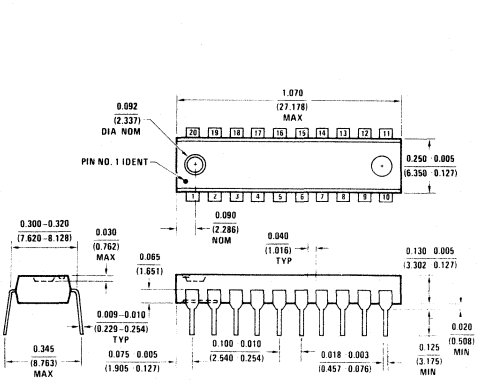
14-Lead Molded Dual-In-Line Package (N)
NS Package Number N14A



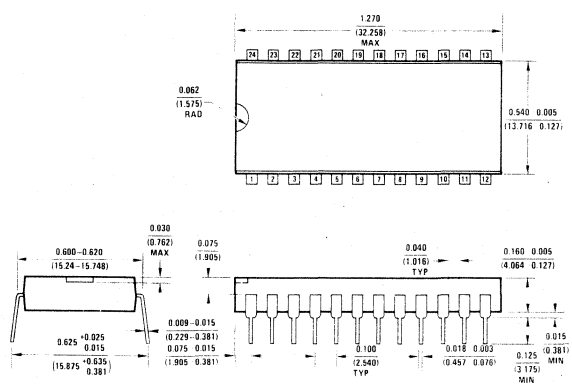
16-Lead Molded Dual-In-Line Package (N)
NS Package Number N16A



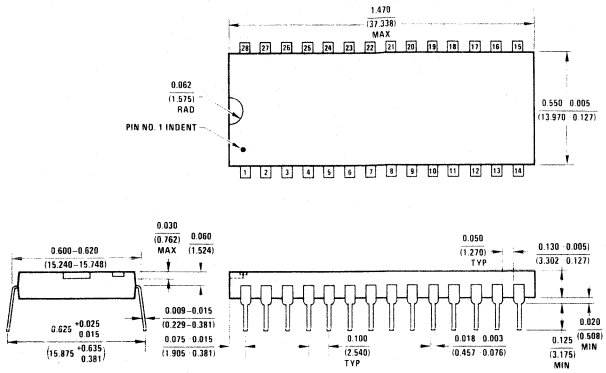
18-Lead Molded Dual-In-Line Package (N)
NS Package Number N18A



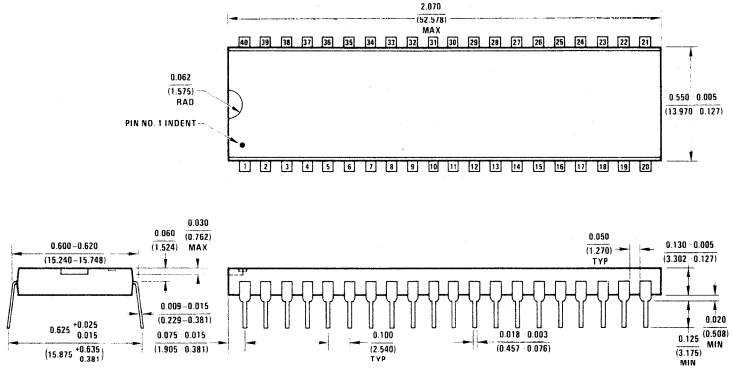
20-Lead Molded Dual-In-Line Package (N)
NS Package Number N20A



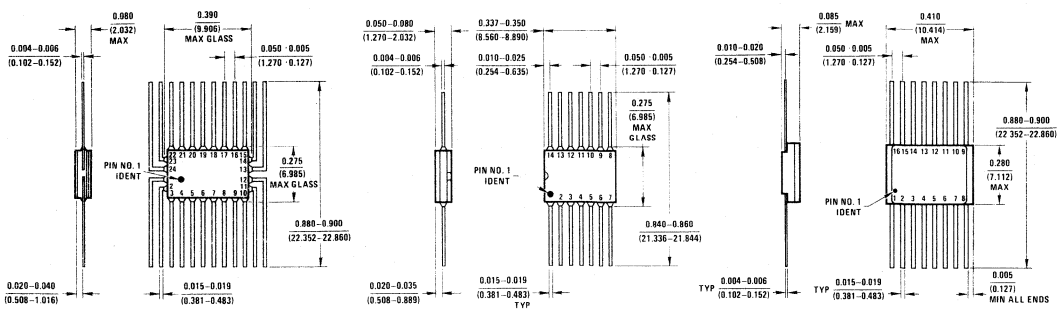
24-Lead Molded Dual-In-Line Package (N)
NS Package Number N24A



28-Lead Molded Dual-In-Line Package (N)
NS Package Number N28A



40-Lead Molded Dual-In-Line Package (N)
NS Package Number N40A



24-Lead Hermetic Flat Package (F)
NS Package Number F24A

14-Lead Hermetic Flat Package (W)
NS Package Number W14A

16-Lead Hermetic Flat Package (W)
NS Package Number W16A

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